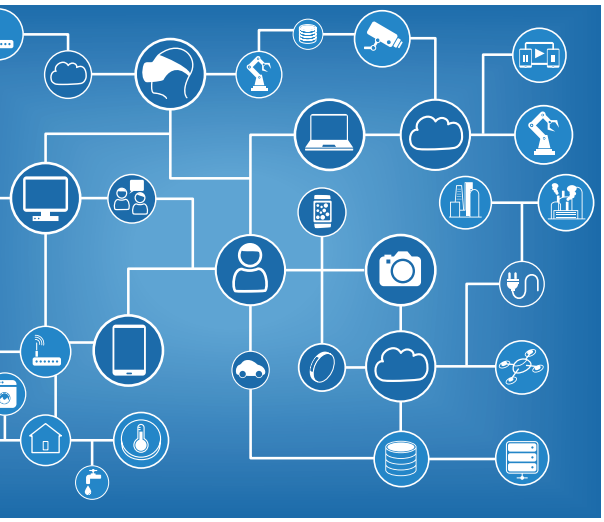
DESIGN AUTOMATION CONFERENCE

CONFERENCE PROGRAM & EXHIBITS GUIDE



JUNE 7-11, 2015
MOSCONE CENTER, SAN FRANCISCO, CA

SPONSORED BY: SIGDA, EDA CONSORTIUM, CEDA IEEE Council on Electronic Design Automation

IN TECHNICAL COOPERATION WITH: SSCS

#52DAC

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GENERAL CHAIR'S WELCOME

Dear Colleagues,

Welcome to the 52nd Design Automation Conference, once again in San Francisco: the cultural, commercial and financial center of Northern California. And for this week, San Francisco is the design automation capital of the world!

Led by the DAC executive committee, countless volunteers who help pull together the conference have excelled once again, bringing you a program filled with incredible research and industry presentations. Our 175+ vendors, an integral part of the conference ecosystem and great contributors to our success, will showcase recent technology advances in design automation, foundry solutions, embedded systems and software, and IP.

DAC is unique in bringing together industry and university researchers, designers, developers, vendors and training partners. There is no better conference for learning and networking, activities which of course aren't limited to the technical sessions. Join us for networking every day at 6:00pm: Monday and Tuesday for the first time on the show floor, and Wednesday on the Moscone Esplanade.

Our industry is doing well and achieved record revenue last year, according to an April 2014 EDAC report. It has also been a year of good news for DAC. We received record submissions for a slew of conference areas, including the research, designer and IP tracks, as well as for tutorials and collocated events. We're continuing our investment in embedded systems and software content, which as in recent years will make up a third of the program. We had more than 1,000 "I love DAC" registrations in the first week alone and more than 30,000 views of our weekly blog over the last nine months.

Here are some forthcoming #DAC52 highlights by the numbers:

- 4 amazing Keynote Sessions and 1 Visionary Moore's Law Talk
- 8 interesting SKY (short keynote) Talks
- 9 Tutorials, 9 Workshops, and 6 Colocated Conferences
- 2 Management Day Sessions
- 24 Special Sessions and Panels
- 27 Research Paper Sessions
- 21 Designer and IP Track Sessions, and a special poster networking session on Tuesday at 4:30pm.
- 6 training sessions on Thursday by Doulos

Make sure to check out the DAC pavilion program and make your way there for the twice daily SKY talks—we moved them to the exhibit floor to make it easier to attend and are featuring some very interesting speakers you don't want to miss.

With our mobile app we are making DAC more fun this year with a game called DAC Attack. You can find details online or just ask ask anyone with an official DAC shirt how to play and compete for several cool prizes including an Apple Watch.

Enjoy the #52DAC!

Anne Cirkel
General Chair, 52nd DAC

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CONFERENCE SPONSORS

ACM/SIGDA

The ACM Special Interest Group on Design Automation has a long history of supporting conferences and the EDA profession. In addition to sponsoring DAC, SIGDA sponsors ICCAD, DATE, and ASP-DAC, plus approximately 15 smaller symposia and workshops. SIGDA provides a broad array of additional resources to our members, to students and professors, and to the EDA profession in general. SIGDA organizes the University Booth and Ph.D. Forum at DAC, and the CADathlon at ICCAD, and also funds various scholarships and awards. Other benefits provided to SIGDA members include the SIGDA's E-Newsletter containing information on upcoming conferences and funding opportunities, SIGDA News highlighting most relevant events in EDA and semiconductor industry, and the "What is...?" column that brings to the attention of EDA professionals the most recent topics of interest in design automation. For further information on SIGDA's programs and resources, see www.sigda.org.

IEEE/COUNCIL ON ELECTRONIC DESIGN AUTOMATION

The IEEE is the world's leading professional association for the advancement of technology, with 430,000 members across 160 countries. The IEEE Council on Electronic Design Automation (CEDA) provides a single focal point for all EDA activities across six major IEEE societies (Circuits & Systems, Computer, Electron Devices, Solid State Circuits, Antennas & Propagation, and Microwave Theory & Techniques). The Council sponsors or co-sponsors over a dozen key EDA conferences, including the Design Automation Conference (DAC), and the International Conference on Computer Aided Design (ICCAD), Design Automation and Test in Europe (DATE) and the Asia South Pacific Design Automation Conference (ASPDAC).
The Council also publishes the IEEE Transactions on CAD, as well as the IEEE Embedded Systems Letters, and sponsors active technical committees like the DATC and CANDE. Since its founding, the Council has expanded its support of emerging areas within EDA such as nanoscale systems, sponsored new initiatives including the Distinguished Speaker Series and is increasing recognition of members of the EDA profession via awards such as the A. Richard Newton Award, Phil Kaufmann Award, and Early Career Award. The Council welcomes new volunteers and local chapters. For more information on CEDA, visit: www.ieee-ceda.org.

EDA CONSORTIUM

The EDA Consortium (EDAC) is the international association of companies that provide tools and services enabling engineers to create the world's electronic products. EDAC addresses issues that are common to its members and the community they serve. Recent accomplishments include simplification of international EDA export regulation, coordinating software anti-piracy efforts, a quarterly Market Statistics Service (MSS) report, and publication of an industry Operating Systems Roadmap. Companies that become EDAC members are eligible for a 10% discount on DAC Exhibit Booth and Suite Space. Contact the EDA Consortium today about sponsorship and membership opportunities. For more information on the EDA Consortium, visit: www.edac.org.

IMPORTANT INFORMATION

EXHIBIT HOURS

LOCATION: SOUTH HALL

Monday, June 8	10:00am - 7:00pm
Tuesday, June 9	10:00am - 7:00pm
Wednesday, June 10	10:00am - 6:00pm

REGISTRATION HOURS

LOCATION: SOUTH LOBBY

Thursday, June 4	12:00 – 6:00pm
Friday, June 5 - Sunday, June 7	8:00am – 6:00pm
Monday, June 8 - Thursday, June 11	7:00am – 7:00pm

Sponsored By: ANSYS

ONLINE PROCEEDINGS

DAC Proceedings and tutorials will be delivered electronically online via a username and password.

To access: http://proceedings.dac.com
Username = Email address
Password = Registration ID (on your badge)

Please refer to your registration receipt to be reminded of what package and associated files you are eligible to view.

DAC MOBLE APP

ANDROID APP ON Google play

Available on the App Store

INFORMATION DESK

The Information Desk is located in the South Lobby of the Moscone Center.

STAY CONNECTED

WIRELESS INTERNET

Moscone Center offers complimentary wireless internet in the lobbies and meeting rooms only. This is a limited service of 256K, to upgrade a fee will be charged by Moscone.

"BIRDS-OF-A-FEATHER" MEETINGS

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal, non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather" (BOF). All BOF meetings are held at the Moscone Center, Tuesday, June 9 from 7:00 - 8:30pm.

To arrange a BOF meeting, please contact Lisa@DAC.com. An LCD projector and screen will be provided.

FIRST AID ROOM

First Aid Room is located across from Room 106.

A nurse will be on duty at all times while meetings and exhibits are open.

Non-emergency: 415-974-4092
Emergency: 511

Help may be reached 24 hours a day from any house phone within the Moscone Center at extension 511.

DAC BUSING

Again this year, DAC is providing bus transportation from San Jose to the South Lobby of the Moscone Center.

The buses will run Monday, June 8 - Wednesday, June 10. Parking at SEMI, the bus pick-up location, will be free. Pick-up and departure times are listed below.

SEMI
3081 Zanker Road
San Jose, CA 95113

Pick-up times from San Jose to the Moscone Center:
7:30am, 7:45am, 9:00am

Departure times from the Moscone Center to San Jose:
6:30pm, 7:15pm

JOIN YOUR FRIENDS & COLLEAGUES!
DAC NETWORKING OPPORTUNITIES

WELCOME RECEPTION

Sunday, June 7, 5:30 - 7:00pm
Intercontinental Hotel -
Grand Ballroom BC

Sponsored by:

Austin – CONVENTION & VISITORS BUREAU –

NETWORKING RECEPTION

Designer/IP Track
Poster Session
Tuesday, June 9, 4:30 - 6:00pm
Exhibit Floor

Sponsored by:

Mentor Graphics

ChipEstimate.com

NETWORKING RECEPTION

Wednesday, June 10, 6:00 - 7:00pm
Esplanade Foyer

Sponsored by:

COCKTAILS & CONVERSATIONS

Networking Reception on the Show Floor

Two Nights!

- **Monday, June 8, 6:00 - 7:00pm**
- **Tuesday, June 9, 6:00 - 7:00pm**

Exhibit Floor

Sponsored by:

AMIQ

25 Celebrating concept engineering

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NETWORKING RECEPTION

Thursday, June 11, 5:30 - 6:30pm
Esplanade Foyer

KEYNOTE PRESENTATIONS

GOOGLE SMART LENS: IC DESIGN AND BEYOND

Brian Otis - *Director, Google, Inc., Mountain View, CA*

- Monday, June 8
  9:20 - 10:00am
  Room: Gateway Ballroom

MOORE'S LAW AT FIFTY: NO END IN SIGHT

Vivek Singh - *Intel Fellow, Intel Corp., Hillsboro, OR*

- Tuesday, June 9
  9:00 - 9:15am
  Room: Gateway Ballroom

THE DESIGN OF INNOVATION THAT DRIVES TOMORROW

Jeffrey Owens - *Chief Technology Officer and Executive Vice President, Delphi Automotive, Troy, MI*

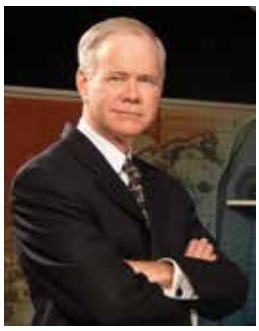
- Tuesday, June 9
  9:15 - 10:00am
  Room: Gateway Ballroom

CYBER THREATS TO CONNECTED CARS: STAYING SAFE REQUIRES MORE THAN FOLLOWING THE RULES OF THE ROAD

- Wednesday, June 10
  9:00 - 10:00am
  Room: Gateway Ballroom

Jeffrey Massimilla
- Chief Product Cybersecurity Officer, Vehicle and Vehicle Services Cybersecurity General Motors Company, Warren, MI

Craig Smith
- Founder, Theia Labs / OpenGarages.org / IATC, Seattle, WA



John McElroy
- President, Blue Sky Productions, Farmington Hills, MI

ELECTRONICS FOR THE HUMAN BODY

John Rogers *- Professor, Univ. of Illinois at Urbana-Champaign, IL*

- Thursday, June 11
  9:15 - 10:00am
  Room: Gateway Ballroom

SKY TALKS

WOMEN, LEADERSHIP AND TECHNOLOGY: WHY TECHNOLOGY NEEDS MORE WOMEN

Telle Whitney - *Anita Borg Institute, Palo Alto, CA*

- Monday, June 8
  1:00 - 1:30pm
  DAC Pavilion, Booth 311

IOT SECURITY: SOLUTIONS AND CHALLENGES AHEAD

Charles Hudson Jr. - *Comcast Corporation, Philadelphia, PA*

- Monday, June 8
  3:30 - 4:00pm
  DAC Pavilion, Booth 311

VIRTUAL TO THE (NEAR) END – USING VIRTUAL PLATFORMS FOR CONTINUOUS INTEGRATION

Jakob Engblom - *Wind River Systems, Inc., Kista, Sweden*

- Tuesday, June 9
  1:00 - 1:30pm
  DAC Pavilion, Booth 311

THE PERFECT STORM: TRENDS IN FUNCTIONAL VERIFICATION

Harry D. Foster - *Mentor Graphics Corp., Wilsonville, OR*

- Tuesday, June 9
  3:30 - 4:00pm
  DAC Pavilion, Booth 311

BUILDING INFINITE SERVICE OPPORTUNITIES WITH IOT

Ali Sebt - *Renesas Electronics America, Santa Clara, CA*

- Wednesday, June 10
  1:00 - 1:30pm
  DAC Pavilion, Booth 311

CHIPS FOR AUTOMOTIVE – IC ROBUSTNESS VERIFICATION IN THE BRAVE NEW WORLD OF ISO 26262

Maik Herzog - *Infineon Technologies AG, Munich, Germany*

- Wednesday, June 10
  3:30 - 4:00pm
  DAC Pavilion, Booth 311

FPGA'S AND INCREASING SECURITY REQUIREMENTS

Sean Atsatt - *Altera Corp., San Jose, CA*

- Thursday, June 11
  1:00 - 1:30pm
  Room: 303

"ON THE MATTER OF TRUST"

Kerry Bernstein - *Defense Advanced Research Projects Agency, Arlington, VA*

- Thursday, June 11
  3:30 - 4:00pm
  Room: 303

IN MEMORY

GAETANO BORRIELLO 1958-2015

This year we lost a visionary leader in the fields of design automation, ubiquitous computing and technology for developing countries.

Gaetano was Jerre D. Noe Professor of Computer Science & Engineering at the University of Washington, where he taught for 27 years.

Born in Naples, Italy, Gaetano immigrated to Brooklyn, N.Y., with his family when he was 9. He never lost his fluent Italian and loved visiting family in Italy. He earned a bachelor of science from the Polytechnic Institute of New York in 1979, and a master's degree from Stanford in 1981. He was a member of the research staff at the Xerox Palo Alto Research Center from 1981 to 1984 during the heyday of VLSI research. He earned his Ph.D. from the University of California, Berkeley, in 1988, and then joined the University of Washington.

Gaetano's research career started in the area of integrated circuit design, focusing on automatic synthesis of hardware and software components of embedded systems, with an emphasis on interfaces and the analysis and verification of timing constraints. He was also active in research on architectures and tools for reconfigurable hardware.

In the late 90's Gaetano's interests turned to the applications of ubiquitous and embedded computing, and he led the DARPA-sponsored project Portolano as an expedition into this nascent research area. He and his students became known for many forward-looking projects including location-aware computing, sensor-rich computing and wearable computing. In 2001, he was chosen as the founding director of Intel's Seattle Research Lab, which he directed for three years before returning full-time to the University of Washington. The Seattle Lab flourished under his leadership to become one of the premiere research labs on embedded computing.

Gaetano then focused on employing embedded computing to solve problems in the developing world. While on sabbatical at Google, he and his students invented the Open Data Kit, a collection of open-source mobile data collection tools that have been used around the world to address issues in public health, human rights and the environment. Today, when the International Red Cross, Kiva, the Carter Center, the US Agency for International Development, the World Health Organization, Google, the Centers for Disease Control, New York City, the Jane Goodall Institute, or many others around the globe think of data collection, they think of ODK.

Gaetano was a force in both education and research, known for his dedication to students and his leadership in exploring new research areas. He received the University of Washington Distinguished Teaching Award in 1995 and University of Washington Marsha L. Landolt Distinguished Graduate Mentor Award in 2014. He was a Fellow of ACM and IEEE as well as a Fulbright Scholar.

He will be remembered by students and colleagues as warm, caring and generous with his time. As Jane Goodall wrote to his family, "[We] recall his kindness, thoughtfulness and desire to be of service, as well as his humble nature and the unassuming way in which he was developing the next generation of computer scientists and engineers so they too can use their knowledge to improve the lives of others. What a great loss indeed he is to our world."

UW Computer Science & Engineering has established the Gaetano Borriello Endowed Fellowship for Change, which will support University of Washington students exploring technology to improve the lives of underserved populations. You can support this Fellowship here: tinyurl.com/GaetanoBorriello.

WORKSHOPS

WORKSHOP 1: LOW-POWER IMAGE RECOGNITION CHALLENGE (LPIRC)

Time: 9:00am - 4:30pm || Room: 310
Track: Embedded Systems || Topic Area: Low-Power Circuits and Systems

ORGANIZERS:
Yung-Hsiang Lu - *Purdue Univ., West Lafayette, IN*
Alex Berg - *Univ. of North Carolina, Chapel Hill, NC*

Many mobile systems (smartphones, electronic glass, autonomous robots) can capture images. These systems use batteries and energy conservation is essential. This challenge aims to discover the best technology in both image recognition and energy conservation. Winners will be evaluated based on both high recognition accuracy and low power usage.

This workshop is a programming contest. Registration is available for attendees to observe the participants.

There is no workshop presentation. The winners will be announced on Monday, June 8 at 4:30pm in the DAC Pavilion Booth #311.

WORKSHOP 2: DESIGN AUTOMATION FOR BEYOND-CMOS TECHNOLOGIES

Time: 8:30am - 5:30pm || Room: 301
Track: Silicon Design || Topic Area: Emerging Technologies

ORGANIZERS:
Rasit Topaloglu - *IBM Corp., Poughkeepsie, NY*
Shaloo Rakheja - *New York Univ. New York, NY*

Traditional scaling has been continuing but without implied guarantees that we can manufacture devices at finer and finer pitches. It is possible that we may need to switch to new materials and beyond-CMOS devices, which may require drastically different EDA support. Hence, it is a great opportunity to bring researchers working on such devices with design automation community and discuss if new EDA models or tools are needed.

This workshop features invited talks by leading researchers on each topic. An accompanying panel allows interactive Q&A. Furthermore, posters are presented to discuss early work.

SPEAKERS:
Philip Wong - *Stanford Univ., Stanford, CA*
Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*
An Chen - *GLOBALFOUNDRIES, Santa Clara, CA*
Lu Li - *Univ. of Michigan, Ann Arbor, MI*
Sasikanth Manipatruni - *Intel Corp., Portland, OR*
Vijay Narayanan - *Pennsylvania State Univ., State College, PA*
Michael Niemier - *Univ. of Notre Dame, IN*
Praveen Raghavan - *IMEC, Heverlee, Belgium*
Sayeef Salahuddin - *Univ. of California, Berkeley, CA*
Shaloo Rakheja -*New York Univ., New York, NY*

WORKSHOP 3: SEAK 2015: DAC WORKSHOP ON SUITE OF EMBEDDED APPLICATIONS AND KERNELS

Time: 9:00am - 5:30pm || Room: 300
Track: Embedded Systems || Topic Area: Embedded System Architecture and Design

ORGANIZERS:
Adolfy Hoisie - *Pacific Northwest National Lab, Richland, WA*
Darren Kerbyson - *Pacific Northwest National Lab, Richland, WA*
Antonino Tumeo - *Pacific Northwest National Lab, Richland, WA*
Joseph Manzano - *Pacific Northwest National Lab, Richland, WA*
Joseph Cross - *Defense Advanced Research Projects Agency, Arlington, WA*
Nathan Tallent - *Pacific Northwest National Lab, Richland, WA*

This workshop is a venue for the DARPA SEAK project to interact with the broader embedded community. SEAK is defining a new, public suite of constraining problems to evaluate end-to-end embedded systems for application areas of interest. SEAK also expects to provide yearly or bi-yearly rankings of the most appropriate embedded systems for those areas.

Evaluating, benchmarking and classifying embedded systems are challenging tasks. Embedded systems are designed to fit within certain constraints dictated by their target application areas. Aspects such as power consumption, real time awareness, reliability, accuracy of the computation, cost, device and physical size are all metrics under which an embedded system can be classified and that have a direct influence on the overall system performance. All these contrasting metrics define how well an embedded system can address its target application. An additional challenge derives from the fact that modern embedded systems are composed of a multitude of heterogeneous processing elements and components. They include general-purpose processors, digital signal processors, graphic processors, application specific accelerators, reconfigurable logic and more. These components can be either off-the-shelf or custom designed. Embedded systems often present disparate types of memory hierarchies. Also the software toolchain, which includes compilers, synthesizers and optimization tools, may have significant impacts on the metrics.

This workshop aims at involving the benchmarking, simulation and modeling community to devise novel systematic approaches to evaluate, characterize, and classify embedded systems, with a particular focus on the power/performance tradeoffs. It objective is to provide a novel and vital forum where to discuss methodologies and approaches to evaluate embedded systems, including appropriate metrics, benchmarks applications, microbenchmarks, power/performance instrumentation.

SPEAKERS:
Gary Ray - *Boeing, Seattle, WA*
John Hodapp - *Night Vision and Electronic Sensors Directorate, Fort Belvoir, VA*
Jeffrey Smith - *BAE Systems, Inc. , Hooksett, NH*
Luca Carloni - *Columbia Univ., Columbia, NY*
James Bonick - *Night Vision and Electronic Sensors Directorate, Fort Belvoir, VA*

WORKSHOP 4: SYSTEM-TO-SILICON PERFORMANCE MODELING AND ANALYSIS

Time: 9:00am - 5:00pm || Room: 302
Track: Embedded Systems || Topic Area: Embedded System Architecture and Design

ORGANIZERS:
Adam Morawiec - *ECSI, Belmont, France*
Laurent Maillet-Contoz - *STMicroelectronics, Grenoble, France*
Kim Grüttner - *OFFIS – Institute for Information Technology, Oldenburg, Germany*
Gjalt de Jong - *ArchWorks, Diegem, Belgium*

SESSION ORGANIZERS:
Andreas Herkersdorf -*TU München, Germany*
Jürgen Becker -*KIT Karlsruhe, Germany*
Domenik Helms -*OFFIS, Germany*
Christoph Sohrmann -*Fraunhofer Institute for Integrated Circuits IIS, Germany*
Roland Jancke -*Fraunhofer Institute for Integrated Circuits IIS, Germany*

The integration of heterogeneous electronic systems composed of SW and HW requires not only a proper handling of system functionality, but also an appropriate expression and analysis of various extra-functional properties: timing, energy consumption, thermal behavior, reliability, cost and others as well as performance aspects related to caching, non-determinism, probabilistic effects.

The workshop addresses cross-domain aspects related to the design and verification framework covering methodology, interoperable tools, flows, interfaces and standards that enable formalization, specification, annotation and refinement of functional and extra-functional properties of a system. Special emphasis will be given to formalization and expression of power, temperature, reliability, degradation and aging.

Several research and industry efforts address (parts of) the problem. However, there is a need for community-wide cooperation to establish a holistic vision on extra-functional property treatment, and to agree on research and development directions and further on validation of applicable solutions and standardization. This event will support collaboration between main actors from system and microelectronics industry, EDA and research.

The workshop is inviting submissions of short abstracts industrial and scientific work in progress and practical solution and experiences.

Main Topics

- Formalization,specification and modeling of extra-functional properties (e.g. using UML, SysML, MARTE, …) and multi-physics specification of timing, power, temperature, reliability and aging properties from system level, transactional level, to implementation
- Domain-specific languages and formalisms; system-level design languages (e.g. C++, SystemC, SystemVerilog, …) and extensions to express extra-functional properties
- Tracing of extra-functional properties during simulation and run-time
- Model of computation extensions for non-determinism, probability analysis, caching, timing, power, temperature, reliability, ...
- System performance and design space exploration using abstract modelling and analysis (e.g. virtual prototyping, …)
- Multi-physics simulation challenges: speed vs. accuracy, fidelity
- Power and performance estimation, analysis and measurement techniques
- Temperature measurement, abstraction, modeling and analysis techniques
- Power and temperature aware scheduling & real-time analysis
- System level reliability and aging models
- Reliability from transistor to RTL level: e.g. NBTI models including basic physical properties
- Design for Aging and Reliability
- Performance objectives validation, including metrics (across abstraction levels) and formal checking of extra-functional properties (e.g. using contract-based design techniques)
- Evolution and extensions of standards like UPF, IP-XACT to express extra-functional properties
- Industrial case-studies, state-of-the-art EDA tools including identification of challenges and gaps

WORKSHOP 5: COMPUTING IN HETEROGENEOUS, AUTONOMOUS 'N' GOAL-ORIENTED ENVIRONMENTS

Time: 9:00am - 5:00pm || Room: 303
Track: Embedded Systems || Topic Area: Emerging Technologies

ORGANIZERS:
Marco Santambrogio, Alessandro Nacci - *Politecnico di Milano, Italy*
Hank Hoffmann - *Univ. of Chicago, IL*

As the push for parallelism continues to increase the number of cores on a chip, system design has become incredibly complex; optimizing for performance and power efficiency is now nearly impossible for the application programmer. To assist the programmer, a variety of techniques for optimizing performance and power at runtime have been developed, but many employ the use of speculative threads or performance counters. These approaches result in stolen cycles, or the use of an extra core, and such expensive penalties can greatly reduce the potential gains.

Within this context imagine a revolutionary computing system that can observe its own execution and optimize its behavior around a user's or application's needs. Imagine a programming capability by which users can specify their desired goals rather than how to perform a task, along with constraints in terms of an energy budget, a time constraint, or simply a preference for an approximate answer over an exact answer.

Imagine further a computing system that performs better according to a user's preferred goal the longer it runs an application. Such an architecture will enable, for example, a handheld radio or a cell phone that can run cooler the longer the connection time.
Or, a system that can perform reliably and continuously in a range of environments by tolerating hard and transient failures through self healing.

Self-aware computer systems are the key technology to succeed in doing this. They will be able to configure, heal, optimize, improve interaction and protect themselves without the need for human intervention, exploiting abilities that allow them to automatically find the best way to accomplish a given goal with the resources at hand. Within this context, imagine a revolutionary computing system that can observe its own execution and optimize its behavior around the external environment, user's and application's needs.
The Self-Aware computing research leverages the new balance of resources to improve performance, utilization, reliability and programmability.

Within this context, the proposed workshop is intended to present innovative works describing:

- Self-aware Operating Systems
- Autonomous self-aware computer architecture
- Adaptive algorithm and distributed self-training algorithms
- Biologically inspired systems

SPEAKERS:
Steven Hofmeyr - *Lawrence Berkeley National Lab, Berkeley, CA*
Gianluca Carlo Durelli - *Politecnico di Milano, Italy*
Wayne Luk - *Imperial College London, United Kingdom*
John Kubiatowicz - *Univ. of California, Berkeley, CA*
Nikil Dutt - *Univ. of California, Irvine, CA*
Georgi Gaydadjiev - *Maxeler Technologies, London, United Kingdom*
Matteo Ferroni - *Politecnico di Milano, Italy*

WORKSHOP 6: DESIGN AUTOMATION FOR HPC, CLOUDS, AND SERVER-CLASS SOCS

Time: 8:30am - 5:00pm || Room: 304 || Track: EDA || Topic Area: System-on-Chip Design

ORGANIZERS:
John Shalf - *Lawrence Berkeley National Lab, Berkeley, CA*
James Ang - *Sandia National Laboratories, Albequerque, NM*
David Donofrio - *Lawrence Berkeley National Lab, Berkeley, CA*

The current mainstream HPC and Cloud has relied upon Commercial off-the-Shelf (COTS) commodity building blocks to enable cost-effective design by sharing costs across a larger computing ecosystem. Modern HPC nodes use commodity chipsets and processor chips integrated together on custom motherboards. An alternative model for commodity HPC, high performance embedded, mobile and Cloud technology is emerging where the chip acts as the "silicon motherboard" that interconnects commodity Intellectual Property (IP) circuit building blocks to create a complete integrated System-on-a-Chip (SoC). This silicon-motherboard approach is still very much COTS, but the commodities are licensable IP for pre-verified circuit designs (the Lego-blocks for SoC designs) rather than the chips. By leveraging the enormous commodity IP market for design tools, processors, memory controllers, and I/O circuit designs, a chip designer can focus their effort and NRE costs on engineering a handful of essential features that are not covered by the commodity ecosystem. This presents a new design paradigm and architecture for large-scale computing including both Clouds and HPC systems.

Traditionally SoC design methods have focused on low-power consumer electronics or high performance embedded applications. But now SoC design methods are moving into high-end computing due to the emergence of embedded IP offering capable double-precision floating point, 64-bit address capability, and options for high performance I/O and memory interfaces. System on Chip (SoC) integration is able to further reduce power, increase integration density, and improve reliability. It also enables designers to minimize off-chip I/O by integrating application required peripheral functions, such as network interfaces and memory controllers by integrating application optimized components onto a single chip. However, existing CAD, EDA and HDL tools are primarily oriented towards consumer electronics devices, and gaps remain in the technologies for automating synthesis of components suitable for highly scalable HPC and Cloud systems.

This workshop will explore the CAD, EDA and HDL tools for Server-Class SoCs that are suitable for server-class applications that range from high-performance embedded/mobile to clouds and supercomputers. The focus of the workshop will be on tools that enable designers to rapidly prototype, simulate, and synthesize, with a much faster turn-around than we have come accustomed to for commodity server and high performance embedded/mobile chip designs (many designs targeted at an 18 month design cycle for the hyper-competitive consumer market).

This workshop builds upon the highly successful "System-on-Chip Design for HPC" workshop that took place in August of 2014 in Denver Colorado. It is fortuitous to colocate with the Design Automation Conference (DAC) in order to maximally leverage the community of experts in Computer Automated Design (CAD) tools to tackle this challenging problem of reinventing High performance embedded, server, and data center technologies for the new century.

SPEAKERS:
Scott Houghton - *Advanced Micro Devices, Inc., Austin, TX*
Shekhar Borkar - *Intel Corp., Santa Clara, CA*
Mike Holmes - *Sandia National Laboratories, Albuquerque, NM*
Noel Wheeler - *Univ. of Maryland, Catonsville, MD*
Rob Aitken - *ARM Ltd., Austin, TX*
Chris Rowen - *Cadence Design Systems, Inc., Santa Clara, CA*
Krste Asanovic - *Univ. of California, Berkeley, CA*
David Donofrio - *Lawrence Berkeley National Lab, Berkeley, CA*

WORKSHOP 7: REQUIREMENTS DRIVEN VERIFICATION (FOR STANDARDS COMPLIANCE)

Time: 2:00 - 5:00pm || Room: 305 || Track: Automotive || Topic Area: Test and Verification

ORGANIZER:
Mike Bartley - *Test and Verification Solutions, Bristol, United Kingdom*

Requirements-driven verification is based on ensuring that feature-level requirements are adequately verified by tracing such requirements through to verification tasks. It is similar to Coverage-driven verification from the sense that it is metric-driven but differs significantly because the metrics derive from requirements rather than verification goals. Those verification goals may come a wide variety of activities and tools (such as reviews, simulation, formal verification, the lab, etc.) but can all be traced back to one or more requirements.

Requirements-driven verification is required for compliance with the increasing number of standards that control development of hardware and software for domains such as automotive (ISO26262) and avionics (DO254). The workshop will cover what the development standards mandate in development and how it can be delivered through requirements-driven verification methodology.

- Requirements engineering
- Requirements at a hierarchical level
- Requirements of good quality
- Requirements mapping
- No loss incorrect translation or loss of context through the Requirements tree.
- Requirements need to be proven to be implemented and working

The workshop will use an automotive example to cover the three main issues regarding standards compliance and how they are covered through a requirements-driven verification methodology making the most use of the strengths and weaknesses of available tools and techniques.

1. Requirements elicitation and passing through a Quality gateway
- Where and how do we elicit the requirements, what format and quality are they?
- Ensure we recognize the scope from which to elicit the requirements and any influencers outside the scope.
- Identify hazards, safety goals and how to mitigate the hazards.
- How can we harmonize the requirements so that multiple sources have the same look and feel.
- How do we split requirements to ensure a pragmatic approach to Requirements engineering that will work with the product?
- How do we check for quality? Boiler plates, manual inspection,model rule checker pros and cons of these methods
- What do we gain by ensuring a quality gateway is passed (automation, better comprehension, better customer interface, early analysis of impact and conflicts)?

2. Translation of data down the Requirements tree safely
- Multiple documents and model types mean multiple transformations of data?
- Ways to ensure data stays where it is and can be read by multiple tools, including model to model transformation
- Reuse and Variability (orthogonal problems)
- The need to reduce data transformations and increase reuse
- Ensure that the hierarchy is followed down the requirements engineering tree (otherwise there is a need to revert to configuration files
and look up tables)

3. Demonstrating that each requirement is proven to work "proof of implementation"
- How do we link requirements into their 'proofs' (test results, formal proofs, coverage, documents, manual inspection etc.)?
- How variability extends into the verification domain.
- Reusability in testbenches vs. maintainability: how to follow the requirements variation model.
- Ensuring a complete set of requirements and minimizing testbenches, tests and proofs.
- Eliminate over-engineering by ensuring that you are only verifying and maintaining what is needed.
- Auditable documentation: what is acceptable and what metadata is needed?
- Change and configuration management: what needs to be recorded and how long does it needed to be maintained?

SPEAKER:
Dave Kelf - *OneSpin Solutions GmbH, Munich, Germany*

WORKSHOP 8: ENTERPRISE-LEVEL IP MANAGEMENT FOR THE DAC SEMICONDUCTOR PROFESSIONAL

Time: 9:00am - 3:00pm || Room: 308 || Track: IP || Topic Area: Business

ORGANIZER:
Warren Savage - *IPextreme, Campbell, CA*

This workshop addresses a burgeoning problem for semiconductor companies - managing the vast amount of IP that is being produced and consumed by their design teams. Over the last 20 years, we have seen the transition from almost no IP reuse to some modern SoC's owing nearly 90% of their functionality to reused or purchased IP.

The workshop will provide the audience with awareness of various best practices used across the semiconductor industry, recognizing that there is no "one-size-fits-all" approach and that each company needs to develop methodologies and processes that are tuned to their organization's unique needs.

There are six primary modules to the workshop:

1. Levels of Design Reuse. In this section we will cover the various levels of IP reuse and how one goes about deciding which level of reuse is appropriate.
2. IP Business Models. There are numerous business models in practice around the licensing of semiconductor IP. We will review the most common ones along with the typical legal terms used in IP license agreements.
3. Common IP Reuse Issues.Many companies struggle with implementing IP reuse, and in this section we will go deep, not only into some of the most common problems, but also how they can be addressed at a technical, organizational, and business level.
4. Creating a Reuse-aware Culture. In this section, we will show examples of how some companies are setting up incentive programs and other vehicles to encourage engineers to regularly employ IP reuse and incorporate more and more IP into their designs.
5. Keeping Track of Everything.The widespread use of IP today has created a gigantic data problem. Information from dozens of suppliers, hundreds of chips, and thousands files needs to be organized in a coherent and consistent fashion. In this section, we will discuss the various techniques that companies are using to get ahead of this tsunami of information.
6. Incorporating User Feed back Loops into Your Processes. Every healthy ecosystem needs to have in place the facility for people to share information and awareness of activities so that the system can be improved. In this section, we will share a few best practices associated with communication and continuous improvement of IP-related processes.

This will be a highly interactive workshop throughout which attendees will have an opportunity to ask questions and share their experiences. Each attendee will receive a workshop booklet containing the training materials presented, as well as a scorecard that can be taken away and used following the workshop to assess their own company's capabilities for IP reuse.

Who Should Attend?

- Design engineers developing IP or using IP
- Design managers and architects
- Design executives
- Legal, Finance, and Purchasing people specializing in IP transactions

Also of Interest:
Attendees may find it useful to attend the included afternoon session that complements this workshop and provides all attendees with a hands-on use of IPextreme's Xena IP management software in an interactive group training format.

SPEAKERS:
Warren Savage - *IPextreme, Campbell, CA*
Robert Beanland - *Atrenta Inc., San Jose, CA*

WORKSHOP 9: INTERDISCIPLINARY ACADEMIA INDUSTRY COLLABORATION MODELS AND PARTNERSHIPS

Time: 9:00am - 5:00pm || Room: 309
Track: Embedded Systems || Topic Area: General Interest

ORGANIZERS:
Michael Huebner - *Ruhr Univ. Bochum, Germany*
Patrick Haspel - *Cadence Design Systems, Inc., San Jose, CA*

Design Automation as well as circuit design and implementation did NOT get easier recently! Even in challenging economic situations industry has to find ways to partner closely with academia to ensure continued leading edge research and education. Solutions created under very restrictive constraints often have a high degree of momentum and networking. The workshop will discuss different approaches in which universities and industry can work closely together to overcome those challenges with a focus on the networking aspect.

This workshop will discuss how to tackle the continued increase of complexity in modern EDA/IP environments in academia challenges of today's
academic environments.

1. Funding for research and education (industry funded collaborations)

2. Access to state of the art technology (semiconductor, EDA, IP,…)

3. IP issues of collaboration results

4. Education/Recruiting: Demand definition

The purpose of the workshop is to discuss, understand and learn from each other how collaboration models and partnerships have to be setup so that they can help in tackling those challenges.

SPEAKERS:
Diana Goehringer - *Ruhr Univ. Bochum, Germany*
Jason Wong - *Xilinx, Inc., San, Jose, CA*
Matthew Swabey - *Purdue Univ., West Lafayette, IN*
Patrick Haspel - *Cadence Design Systems, Inc., San Jose, CA*
Ralf Sommer - *Technische Universität Ilmenau, Germany*
Sadanad Gulwadi - *ARM, Inc, San Francisco, CA*

OPENING SESSION & AWARDS PRESENTATION

Room: Gateway Ballroom || Time: 8:45 - 9:20am

MARIE R. PISTILLI WOMEN IN EDA ACHIEVEMENT AWARD

For her significant contributions in helping women advance in the field of EDA technology.
Margaret Martonosi, Princeton Univ.

P.O. PISTILLI UNDERGRADUATE SCHOLARSHIPS FOR ADVANCEMENT IN COMPUTER SCIENCE AND ELECTRICAL ENGINEERING

The objective of the P.O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under-represented groups (women, African-American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship and a volunteer committee continues to administer the program for DAC. DAC normally funds a $4000 scholarship, renewable up to five years, to graduating high school seniors.

The 2015 Recipients are:

Antonio Anguliar
Attending: California Polytechnic State University in San Luis Obispo

Moie Uesugi
Attending: Brown University

EDAC - IEEE/CEDA PHIL KAUFMAN AWARD RE-PRESENTATION

Honoring an individual who has had demonstrable impact on the field of electronic design through contributions in Electronic Design Automation (EDA).
Dr. Lucio Lanza, Lanza Tech Ventures, for providing innovative EDA and IP companies with exceptional vision, mentoring, and financial support.

IEEE CEDA OUTSTANDING SERVICE AWARD

Soha Hassoun, *Tufts Univ.*
For outstanding service to the EDA community as DAC General Chair in 2014.

IEEE CEDA OUTSTANDING SERVICE AWARD

Jörg Henkel, *Karlsruhe Institute of Technology (KIT)*
For outstanding service to the EDA community as ICCAD General Chair in 2013.

IEEE FELLOW

Jörg Henkel, *Karlsruhe Institute of Technology (KIT)*
For contributions to hardware/software codesign of embedded computing systems

IEEE FELLOW

Steven P. Levitan, *Univ. of Pittsburgh*
For contributions to mixed-technology micro-systems education

IEEE FELLOW

Michael Orshansky, *Univ. of Texas at Austin*
For contributions to VLSI design for manufacturability

IEEE FELLOW

Yuan Xie, *Univ.of California at Santa Barbara*
For contributions to design automation and architecture of three-dimensional integrated circuits

IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS DONALD O. PEDERSON BEST PAPER AWARD

Kai Hu, Feiqiao Yu, Tsung-Yi Ho, Krishnendu Chakrabarty, "Testing of Flow-Based Microfluidic Biochips: Fault Modeling, Test Generation, and Experimental Demonstration," Vol. 33, Issue 10, pp. 1463 - 1475, October 2014.

A. RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION

Sponsored by the IEEE Council on EDA and the ACM Special Interest Group on Design Automation.

For pioneering contributions in the discovery and use of silicon physical unclonable functions (PUFs) for the design and operation of secure integrated circuits and systems.
Blaise Gassend, Dwaine Clarke, Marten van Dijk, and Srinivas Devadas, "Silicon Physical Random Functions," Proc. of the 9th ACM Conference on Computer and Communications Security, pp 148 – 160, November 2002

Blaise Gassend, Google

Dwaine Clarke, Univ. of the West Indies

Marten van Dijk, Univ. of Connecticut

Srinivas Devadas, Massachusetts Inst. of Tech.

2015 ACM TODAES BEST PAPER AWARD

A fast and scalable multidimensional multiple-choice knapsack heuristic

Hamid Shojaei, Univ. of Wisconsin, Twan Basten, Eindhoven University of Technology, Marc Geilen, Eindhoven University of Technology, and Azadeh Davoodi, Univ. of Wisconsin
Volume 18, Issue 4, Article 51, October 2013

ACM SIGDA OUTSTANDING NEW FACULTY AWARD

In recognition of a junior faculty member who demonstrates outstanding potential as an educator and/or researcher in the field of electronic design automation.
Muhammad Shafique - Karlsruhe Institute of Technology

ACM SIGDA OUTSTANDING PHD DISSERTATION AWARD

In recognition of an outstanding Ph.D. dissertation that makes the most substantial contribution to the theory and/or application in the field of electronic design automation.

Wenchao Li - "Specification Mining: New Formalisms, Algorithms and Applications"
Advisor: Sanjit Seshia, University of California, Berkeley

ACM FELLOWS

To recognize and honor outstanding ACM members for their achievements in computer science and information technology and for their significant contributions to the mission of the ACM. In particular, we recognize the ACM Fellows involved in design automation research, including the areas of test, security, energy-efficient systems, embedded systems, and SAT solvers.

Srinivas Devadas, *MIT*
For contributions to secure and energy-efficient hardware

Nikil Dutt, *University of California, Irvine*
For contributions to embedded architecture exploration, and service to electronic design automation and embedded systems

Shard Malik, *Princeton University*
For contributions to efficient and capable SAT solvers, and accurate embedded software models

Subhasish Mitra, *Stanford University*
For contributions to the design and testing of robust computing systems

Vijay Narayanan, *Pennsylvania State University*
For contributions to power estimation and optimization in the design of power-aware systems

Parthasarathy Ranganathan, *Google*
For contributions to the areas of energy efficiency and server architectures

Alberto Sangiovanni-Vincentelli, *University of California, Berkeley*
For contributions to electronic design automation

KEYNOTE PRESENTATION

GOOGLE SMART LENS: IC DESIGN AND BEYOND

Brian Otis - *Director, Google, Inc., Mountain View, CA*

9:20 - 10:00am || Room: Gateway Ballroom
Track: Silicon Design || Topic Area: Low-Power Circuits and Systems

Summary: We have amazingly sparse access to information about our own bodies. Indeed, the healthier we are, the less data we collect. Technologies to continually monitor critical biomarkers are still in their infancy, but continuing advances in chip design and biocompatible system integration will help define the next generation of these devices. Against the backdrop of the Google Smart Contact Lens platform, I'll share thoughts on the scarcity of power, extreme miniaturization, and end-to-end connected systems that span the design space from transistors to the cloud. Along the way, I'll cover chip design techniques for body-worn systems and wireless sensors and present examples of constantly-connected devices for improving healthcare.

These areas present tough unsolved problems at the interface between the IC and the outside world that cannot be solved by transistor technology scaling alone. The interface between silicon and the human body is highly variable, erratic, and messy. This unpredictability impacts sensor performance, RF/electromagnetic performance, system reliability, tolerability and comfort, etc.

Several future applications will demand thin-film realization and biocompatibility of complex systems. Novel power sources, low power IC design techniques, microscale user interface technologies, and new system integration techniques will be a few of the enabling technologies for these emerging systems.

Biography: Dr. Brian Otis is a Director at Google and a Research Associate Professor at the University of Washington, Seattle. He received a B.S. in electrical engineering from the University of Washington, Seattle, and a M.S. and Ph.D. degree in electrical engineering from the University of California, Berkeley.

He joined the faculty of the University of Washington in 2005 where he founded a chip design research lab that develops tiny, low power wireless chips for a variety of applications (neural recording, implantable devices, wearable on-body wireless sensors, environmental monitoring, etc).

He has previously held positions at Intel Corporation and Agilent Technologies and has been with Google Inc since 2012. He is a founder of Google's smart contact lens project and leads the Microsystems group at Google Life Sciences. He has served as a member of the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC) and Associate Editor of the Journal of Solid State Circuits (JSSC).

His research interests include low power SoC design, exploring limitations of power and size of wireless systems, and the realization of novel biomedical devices.

1 - IP TRACK: LOW POWER IP

Sponsored by: ChipEstimate.com

Time: 10:30 - 11:30am || Room: 101
Track: IP || Topic Area: Designer and IP Track

CHAIR:
Farzad Zarrinfar - *Mentor Graphics Corp., Fremont, CA*

Many of today's SoCs, ASICs, and ASSPs contain multiple digital, analog, and subsystem IPs. In the majority of cases for such ICs, the dynamic power and static power play key roles in the differentiation and viability of complex chips. In this session, implementation techniques, selection tradeoffs, and optimization for ultra-low power IC will be presented. This is greatly beneficial for designers in applications such as: IOT, automotive, imaging, wireless, networking, portable multimedia, medical, gaming, video, and MEM applications. This session will conclude with a panel discussion featuring low power IP experts.

*** Indicates Best Paper Candidate**

1.1 Taking Advantage of the Dark Silicon Opportunity (10:30)
Drew Wingard - *Sonics, Inc., Milpitas, CA*

1.2 Low Power IP* (11:00)
Luis Paris - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*

1.3 Power Regression Flow for Soft IPs (11:30)
Ritesh Agrawal - *Freescale Semiconductor, Inc., Noida, India*
Saurabh Shrimal - *Calypto Design Systems, Inc., Noida, India*
Ankur Krishna, Kshitij Bajaj, Chanpreet Singh - *Freescale Semiconductor, Inc., Noida, India*

1.4 Techniques for Power and IR Drop Optimization in Sensor Digital IP* (12:00)
Aditya Mukherjee - *Microsoft Corporation, Mountain View, CA*

Q & A Poster Session
Tuesday, June 9 - 4:30 - 6:00pm - Exhibit Floor

2 - IP TRACK: MINIMIZING SOC POWER CONSUMPTION WITH POWER EFFICIENT IPS AND ASSOCIATED TECHNIQUES

Sponsored by: ChipEstimate.com

Time: 11:30am - 12:00pm || Room: 101
Track: IP || Topic Area: Low-Power Circuits and Systems

MODERATOR:
Dave Bursky - *PRN Engineering Services, San Jose, CA*
ORGANIZER:
Farzad Zarrinfar - *Mentor Graphics Corp., Fremont, CA*

In this panel, implementation techniques and tradeoffs for designing ultra Low-power SOCs, ASSPs, and ASICs will be presented. These techniques are critical for battery-powered devices, and other devices that are sensitive to thermal management as well as reduction of packaging cost. IP suppliers and EDA vendors now offer low-power IPs as well as optimization tools.

Topics such as FinFet and FDSOI devices will be compared with planar CMOS, power harvesting, and using UPF for low power implementation. Designers also apply reduced voltage or Dynamic Voltage & Frequency Scaling (DVFS), power shutdown, and retention logic. Typical low-power designs could have over 30 different power modes and power domains. Dual-rail memory IPs operate in full power, partial power, or shutoff modes. Designs include isolation cells, level shifters, and retention cells with multiple modules in each power domain.

Optimization of these advance techniques for various applications such as portable Gaming, IOT, Automotive, Wireless, Networking, Portable Multimedia, wearable computing. low power techniques are paramount for gaining and keeping market share.

PANELISTS:
Lluis Paris - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*
Aditya Mukherjee - *Microsoft Corporation, Mountain View, CA*
Shankar Krishnamoorthy - *Mentor Graphics Corp., Fremont, CA*
Saurabh Shrimal - *Calypto Design Systems, Inc., Noida, India*
Drew Wingard - *Sonics, Inc., Milpitas, CA*

3 - DESIGNER TRACK: NEW CHIPS ON THE BLOCK

Sponsored by: Mentor Graphics

Time: 10:30am - 12:00pm || Room: 105
Track: EDA || Topic Area: Designer and IP Track

CHAIR:
William Wallace - *Texas Instruments, Inc., Richardson, TX*

Following on from the success of "New Chips on the Block" last year. We're continuing again with this attendee favorite. We have an exciting line up of talks from Biotech to Sensors to an application of the OpenPOWER initiative. We expect to have some great talks and insights into the architectural and design approaches required for these diverse chip implementations.

3.1 The Demise of the Age of Antibiotics and the Rise of the CMOS Biochip (10:30)
Mark Miller - *InSilixa, Inc., Sunnyvale, CA*

3.2 Design Challenges for Sensor Hubs in Smartphones/ Wearable Devices (11:00)
Timothy Saxe - *QuickLogic Corp., San Jose, CA*

3.3 Across Company Lines: How CAPI is Driving OpenPOWER Partnerships and Innovation (11:30)
Bruce Wile - *IBM Corp., Poughkeepsie, NY*

4 - IP TRACK: IP IMPLEMENTATION

Time: 1:30 - 2:30pm || Room: 101
Track: IP || Topic Area: Designer and IP Track

Sponsored by: ChipEstimate.com

CHAIR:
Brenda Westcott - *ARM, Inc., San Jose, CA*

IP implementation can mean many different things - all depending on where you are in the design process and what you are trying to build. Selection, verification, and implementation come to mind first, but there are so many other factors to consider now because of the sheer complexity of next-generation SoC designs. This session will explore some of those new challenge considerations and examine the different methodologies and advanced techniques used for IP implementation with real industry examples.

This session includes an interactive panel of noted industry professionals with deep knowledge of IP implementation and optimization for complex SoC design.

4.1 Efficient Synthesis Constraint Methodology for Multiprotocol High Speed Serdes (1:30)
Raghuram TNV, Aravind Vijayakumar, Vivek A, Satyakam Sudershan, Nageswara Rao Kunchapu, Sathish Kumar Ganesan - *Cadence Design Systems, Inc., Bangalore, India*

4.2 Analog IP Reuse: A Methodology to Map Analog IPs to Different Foundries (1:45)
Dan J. Woodard - *IQ-Analog Corporation, San Diego, CA*
Sriram Rajamanohar - *ClioSoft, Inc., Fremont, CA*

4.3 Effective Analysis and Optimization of On-Chip POP Package Co-Design, for DDR Interfaces* (2:00)
Chakrapal Kalwa - *Broadcom Corp., Santa Clara, CA*
Uttara Sampath - *Broadcom Corp., San Jose, CA*
Mohit Kumar - *Broadcom Corp., Santa Clara, CA*
Sam Karikalan, David Chang, James Turner, Sathish Kumar Radhakrishnan - *Broadcom Corp., Irvine, CA*

4.4 The Ultimate Usage of SystemC to Build the HW & SW for Upcoming ULP Wi-Fi IP Solutions (2:15)
Marleen J. Boonen - *Methods2Business BV, Eindhoven, The Netherlands*
Daniel Kesler, Dejan M. Dumic, Miroslav Drobac, Vlada Kalinic, Nemanja Kondic, Tivadar Mako, Lenard Mesaros, Ivan Mokanj, Ratko V. Raicki - *Methods2Business BV, Novi Sad, Serbia*

*** Indicates Best Paper Candidate**

Q & A Poster Session
Tuesday, June 9 - 4:30 - 6:00pm - Exhibit Floor

5 - IP TRACK: UM, HOW DO WE KNOW THE DESIGN WILL WORK? THE IP IMPLEMENTATION PANEL

Time: 2:30 - 3:00pm || Room: 101
Track: IP || Topic Area: General Interest

Sponsored by: ChipEstimate.com

MODERATOR:
Ed Sperling - *Semiconductor Engineering, Los Gatos, CA*
ORGANIZER:
Brenda Westcott - *ARM, Inc., Fremont, CA*

Typical implementation challenges that companies are facing today include IP selection, the verification process, and technology integration – all crucial phases to an IP-based design. But consider some equally crucial challenges. For instance chip size; billion transistor chips affect tool capacity, runtime, memory and yield. And what about these formerly separate, but now acutely connected issues such as overall timing, signoff, variability, test, binning, performance, and yield mesh? These issues in combination can greatly complicate the design, implementation and manufacturing process. This panel of industry experts will discuss the pitfalls of these difficult challenges and explore some potential solutions. They will share from their own unique perspectives various techniques and methodologies used to achieve successful IP-based SoC design implementation.

PANELISTS:
Darren Jones - *Xilinx, Inc., San Jose, CA*
Lawrence Loh - *Cadence Design Systems, Inc., San Jose, CA*
Sean Smith - *Soft Machines, Santa Clara, CA*

6 - DESIGNER TRACK: DIARY OF A WIMPY KID: REAL DESIGNERS HAVE STRONG METHODOLOGY

Time: 1:30 - 3:00pm || Room: 105
Track: EDA || Topic Area: Physical Design

Sponsored by: Mentor Graphics®

CHAIR:
Badhri Uppiliappan - *Analog Devices, Inc., Wilmington, MA*

CO-CHAIR:
Jovanka Ceric-Vujkovic - *Synopsys, Inc., Mountain View, CA*

Smart system architects, experienced designers and robust EDA tools are necessary ingredients for a first-pass working silicon, but are they sufficient? All the robust tools cannot do any good unless you manage the input data and control the tools to produce the right output; otherwise you get the proverbial 'Garbage In, Garbage Out.'

In this session, you will hear the leading edge physical designers share their experience of fine-tuning their methodologies for mixed-signal, near-threshold and high performance designs, and how they analyzed their designs to bring feedback to improve the quality and reliability.

6.1 Fully Automated Interface Elements Insertion for Digital and Analog Mixed Signal Verification in Multi Power Domain Designs (1:30)
Bharath K. Poluri, Atul Lele, Aswani K. Golla, Lakshmanan Balasubramanian, **Sudhakar Surendran** - *Texas Instruments India Pvt. Ltd., Bangalore, India*

6.2 Circuit Design Method for MOS Analog-Design Reuse (1:45)
Akira Suzuki, Yukichi Todoroki, Kazuhiro Miura, **Nobuto Ono** - *Jedat, Inc., Tokyo, Japan*

6.3 A Methodology to Analyze Edge-to-Edge Jitter for High Speed DDR Interfaces with PDN Noise* (2:00)
Clara Lim - *Xilinx, Inc., San Jose, CA*
Anant Narain - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., Noida, India*
Nithin Kumar - *Avago Technologies, Bangalore, India*

6.4 Automation in Derivation of Number of Synchronization Stages and MTBF Computation at SoC Level (2:15)
Sakshi Gupta, Rangarajan Ramanujam, Atul Nauriyal, Nidhi Agnihotri - *STMicroelectronics, Greater Noida, India*
Vaibhav Singh - *STMicroelectronics, Santa Clara, CA*

6.5 Design Methodology for Operating in Near-Threshold-Computing (NTC) Region* (2:30)
Ravinder Rachala - *Advanced Micro Devices, Inc., Austin, TX*

6.6 Self-Heating Analysis Flow with Electro-Thermal Transient Simulation (2:45)
Yonghwan Kim - *Samsung Electronics Co., Ltd., Seoul, Republic of Korea*
Joohee Choung, Wook Kim, Kyungtae Do - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

*** Indicates Best Paper Candidate**

Q & A Poster Session
Tuesday, June 9 - 4:30 - 6:00pm - Exhibit Floor

SKY TALK: WOMEN, LEADERSHIP AND TECHNOLOGY: WHY TECHNOLOGY NEEDS MORE WOMEN

Time: 1:00 - 1:30pm || Room: Booth 311 || Track: EDA || Topic Area: Business

CHAIR:
Donatella Scuito - *Politecnico di Milano, Italy*

Technology innovation is at the heart of the world's positive future, and there is no question that innovation and business success benefit when women and men are together at the table creating technology. Today, women make up about 25% of the technical workforce and earn 18% of computer science degrees. Dr. Whitney will draw on her experience in this area to frame the discussion of where women are today in technology, and present strategies that work both for women to succeed and for organizations that are committed to creating inclusive environments where women thrive.

SPEAKER:
Telle Whitney - *Anita Borg Institute, Palo Alto, CA*

SKY TALK: IOT SECURITY: SOLUTIONS AND CHALLENGES AHEAD

Time: 3:30 - 4:00pm || Room: Booth 311 || Track: Security || Topic Area: Security

CHAIR:
Mark Tehranipoor - *Univ. of Connecticut, Storrs, CT*

Large and small enterprises have long focused on security issues in their network, and those come from bugs, phishing, and viruses. However, they will soon be faced with a new and more formidable foe in Internet of Things. Cisco has predicted that by 2020, there will be more than 50 billions of IoT devices connected to network. Authentication, traceability, tamper resistance, and encryption are few example challenges to address.

SPEAKER:
Charles Hudson Jr. - *Comcast Corporation, Philadelphia, PA*

7 - IP TRACK: SUBSYSTEM IP & IP INTEGRATION

Sponsored by: ChipEstimate.com

Time: 4:30 - 5:30pm || Room: 101
Track: IP || Topic Area: Designer and IP Track

CHAIR:
Clark Chen - *Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan*

As SoC design complexity increases dramatically with every added feature, IP adoption is a proven path to reduce time to market, but integrating IPs from various sources brings its own challenges for both IP providers and SoC designers. In this session, we shall explore solutions including IP platforms, subsystem optimization, and system-level verification.

Immediately following this paper session there will be a panel discussion with representatives from companies providing subsystem IP and IP integration tools who will discuss their experiences and perspectives on the topic of subsystem IP and IP integration.

7.1 DfA: Design for Analytics (4:30)
Graham Pink, Andrew B. Hopkins, David Rose, **Rupert Baines** - *UltraSoC Technologies Ltd., Cambridge, United Kingdom*

7.2 IoT Processor IP Platform (4:45)
Kands Manickam - *IPextreme, Campbell, CA*

7.3 Accelerating ISO 26262 Automotive Functional Safety Certification Using Protected SoC Fabric IP (5:00)
Thomas M. Murphy - *Arteris, Inc., Aptos, CA*
Monica Tang - *Arteris, Inc., Campbell, CA*

7.4 Design in the Eye of the Hurricane - Building Optimal Vision Processing Subsystems* (5:15)
Chris Rowen, Greg Efland, Shrinivas Gadkari, Vadim Kustov, Dan Nicolaescu, Himanshu Sanghavi, Sandip Parikh - *Cadence Design Systems, Inc., San Jose, CA*

*** Indicates Best Paper Candidate**

Q & A Poster Session
Tuesday, June 9 - 4:30 - 6:00pm - Exhibit Floor

8 - IP TRACK: INTEGRATION CHALLENGES OF 3RD PARTY IP - WORTH THE RISK?

Sponsored by: ChipEstimate.com

Time: 5:30 - 6:00pm || Room: 101
Track: IP || Topic Area: General Interest

MODERATOR:
Ann Mutschler - *Semiconductor Engineering, San Jose, CA*
ORGANIZER:
Clark Chen - *Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan*

Modern SoC design challenges include growing design complexity, more advanced or specialty technologies, and shorter product cycles.

The use of 3rd party IP is a proven and effective way to increase quality and lower design risk. On the other hand, the integration of IPs from multiple sources creates new design challenges.

The integration challenges are quite diverse: verification, floorplanning, power management, timing budgeting and closure, routability, pin coloring, fixed poly orientation, design kits formats, etc.

PANELISTS:
Navraj Nandra - *Synopsys, Inc., Mountain View, CA*
Thomas Wong - *Cadence Design Systems, Inc., San Jose, CA*
Albert Li - *Global Unichip Corp., San Jose, CA*
Leah Schuth - *ARM Ltd., San Jose, CA*

9 - DESIGNER TRACK: EMBEDDED SYSTEM DESIGN - MODELS AND OPTIMIZATION

Sponsored by: Mentor Graphics

Time: 4:30 - 6:00pm || Room: 105
Track: Embedded Systems || Topic Area: Embedded System Architecture and Design

CHAIR:
Alicia Strang - *Cadence Design Systems, Inc., Irvine, CA*
CO-CHAIR:
Michael Solka - *Coherent Logix, Austin, TX*

Models are key to managing complexity of today's embedded system design efforts. This session showcases the value of models applicable to multiple facets of embedded systems -- from streaming interfaces to arbitration schemes to firmware, and more. Furthermore, it highlights roles of innovative design methodologies in optimizing product cost and performance.

9.1 An Abstract Formal Model for Verification of Complex Arbitration Schemes (4:30)
Iain Singleton - *Imagination Technologies Ltd., Newcastle Upon Tyne, United Kingdom*
Ashish Darbari - *Imagination Technologies Ltd., Kings, United Kingdom*

9.2 Modeling Streaming Interfaces with Adaptive Accuracy Using TLM2* (4:45)
Murali Krishnan - *Qualcomm India Pvt. Ltd., Chennai, India*
Amitabh Menon - *Qualcomm, Inc., San Jose, CA*

9.3 Model-Based Development of Firmware for Hardware Management Services (5:00)
Tali Rabetti - *IBM Research - Haifa, Israel*
Johannes Koesters - *IBM Corp., Boeblingen, Germany*
Alex Goryachev, Gil Shurek - *IBM Research - Haifa, Israel*
Derk Rembold - *IBM Systems and Technology Group, Mainz, Germany*

9.4 Unified Register Model for SystemVerilog and C (5:15)
Alexander Pivovarov - *Qualcomm, Inc., Markham, ON, Canada*
Amir Nilipour - *Synopsys, Inc., San Diego, CA*
Mansour Amirfathi - *Synopsys, Inc., Mountain View, CA*

9.5 Optimize Product Cost and Performance with System-level 3D Chip, Package, Board Co-Design (5:30)
James Church, **Humair Mandavia** - *Zuken, Milpitas, CA*

9.6 Architectural Exploration Platform for Solid State Drive Designs* (5:45)
Yohei Hasegawa, Akira Kuroda, Hidenori Matsuzaki, Shigehiro Asano - *Toshiba Corp., Kawasaki, Japan*

*** Indicates Best Paper Candidate**

Q & A Poster Session
Tuesday, June 9 - 4:30 - 6:00pm - Exhibit Floor

TUTORIALS

Each Tutorial below is presented multiple times to allow you to cover multiple topics.
Special registration required.

TUTORIAL 1: PATTERNING BEYOND MULTIPLE PATTERNING

Time: 10:30am - 12:00pm & 4:30 - 6:00pm || Room: 301
Track: EDA || Topic Area: Design for Manufacturability

ORGANIZER:
Puneet Gupta - *Univ. of California, Los Angeles, CA*

Multi-patterning is the process of record for many sub 10nm process technologies. The drive to higher densities has required the use of double and triple patterning for several levels. This reduces the profitability of the new processes especially for low volume products in which the mask set is a large percentage of the total cost. For that reason there has been a strong incentive to develop technologies like EUV or DSA to reduce the total number of masks needed in a new technology node while enhancing resolution.

This tutorial explains how introduction of such lithography technologies going to impact layout and circuit design. Choices of lithography would impact physical design and have a significant impact at system level.

This tutorial will focus on transition from 193i multi-patterning technologies to EUV lithography and DSA. Factors that would determine the enablement of these technologies would be highlighted and possible solutions would be shared. For instance, in case of EUV, mask defectivity is one of the biggest challenges to adoption. We will discuss how defective masks can be used and how design layouts can be robustified to these defects. In case of DSA, we will focus on contact patterning and discuss how choice of complementary lithography (e.g., EUV or double patterning) influences DSA compliance of layouts.

SPEAKERS:
Puneet Gupta - *Univ. of California, Los Angeles, CA*
Arindam Malik - *IMEC, Leuven, Belgium*
Andres Torres - *Mentor Graphics Corp., Wilsonville, OR*

TUTORIAL 2: 2.5D/3D MEMORY & LOGIC INTEGRATION: TOOLS, METHODOLOGIES, REQUIREMENT AND INFRASTRUCTURE

Time: 10:30am - 12:00pm & 4:30 - 6:00pm || Room: 302
Track: EDA || Topic Area: General Interest

ORGANIZER:
Farhang Yazdani - *BroadPak Corp., San Jose, CA*

Prospects of 2.5D/3D integration technology to break the memory and logic wall has prompted the memory makers to develop lower power and higher bandwidth devices. These devices are formed by stacking DRAMs in 3D configuration using Through Silicon Via (TSV). Due to large number of micro bumps, silicon interposer is typically used as carrier of choice to integrate these devices with multiple logic dies. Successful integration of these devices with logic dies on interposer, package and Board requires innovative low power logic design techniques, co-design methodology, advanced EDA tools, manufacturing requirement and supply chain infrastructure. Due to thermal requirement, low power logic design plays a critical role in producing a cost effective and reliable 2.5D/3D system.

This session provides the fundamental knowledge, individual skill sets and the most recent state of the art technologies used for 2.5D/3D integration. In particular we present low cost silicon interposer, low power logic design techniques and EDA tools and methodologies to perform system co-design.

SPEAKERS:
Farhang Yazdani - *BroadPak Corp., San Jose, CA*
John Park - *Mentor Graphics Corp., Longmont, CO*
Rajiv V. Joshi - *IBM T.J. Watson Research Center, Yorktown Heights, NY*

TUTORIAL 3: LINUX PORTING, BRING UP AND DRIVER DEVELOPMENT

Time: 10:30am - 12:00pm & 4:30 - 6:00pm || Room: 303
Track: Embedded Systems || Topic Area: Embedded Software

ORGANIZER:
Larry Lapides - *Imperas Software Ltd., Oxford, United Kingdom*

Key Topics:
- Linux for embedded systems, including SMP Linux (Altera)
- Driver development for Linux, both static and dynamic (Loadable Kernel Modules, or LKMs) drivers (Posedge Software)
- Testing of Linux and drivers (Imperas)

Linux has become the general purpose operating system of choice for embedded systems, and is almost always supported for high end SoCs developed by the semiconductor vendors. Most vendors use the open source Linux distribution, then build a custom distribution representing the device tree supported for the specific SoC, and including the necessary drivers for the peripherals on the SoC, as well as supporting other customizations and unique features. The operating system is complicated further with multicore processors and symmetric multiprocessor (SMP) Linux. Just because everyone supports Linux, does not make porting and bring up an easy task. To put it another way: Just because you get to the Linux prompt doesn't mean everything is working.

This tutorial will be presented in three sections. In the first section (Altera), the various components of the Linux distribution will be covered, including the basic Linux kernel, device trees and other customizations, SMP variations and drivers, both static and dynamic. Boot loaders, including U-boot, will also be discussed. The methodology used for bring up of the Linux kernel on hardware will be presented.

Driver development is the focus of the second section of the tutorial (Posedge). An overview of development of both static and dynamic drivers (Loadable Kernel Modules, or LKMs) will be covered. A virtual platform environment will be used to highlight key points in the development methodology, including co-debug of driver software and peripheral hardware models.

The final section (Imperas) will discuss the development of a robust test environment using the virtual platform technology. The virtual platform provides a complementary approach to porting and bring up on hardware. The benefits of controllability, observability and repeatability for virtual platform use will be covered. Specific OS-aware tools will also be highlighted, plus other tools such as non-intrusive memory monitors and the use of software assertions and code and functional coverage techniques for the operating system and drivers.

SPEAKERS:
Matthew Gerlach - *Altera Corp., San Jose, CA*
Henry Von Bank - *Posedge Software, Inc., Rogers, MN*
Simon Davidmann - *Imperas Software Ltd., Oxford, United Kingdom*

TUTORIAL 4: ELECTRIC VEHICLES - WHAT'S IN IT FOR THE EDA FOLKS?

Time: 10:30am - 12:00pm & 1:30 - 3:00pm || Room: 304
Track: Automotive || Topic Area: Automotive Systems

Electronics have already been widely accepted as the distinguishing feature of cars. The focus on automotive embedded systems and software architectures will further increase with Electric Vehicles (EVs) entering the mass market. Traditional design flows in the automotive domain may not be able to cope with the new challenges introduced by EVs, where classical properties such as safety, reliability and efficiency have to be completely redefined. Here, new design automation approaches can be developed and expanded into areas such as battery packs that only recently have gained the attention of the EDA community.

More than ever, algorithms and tools will immediately impact competitiveness in the EV domain and can quickly shuffle the market for car manufacturers, suppliers and design automation companies.

The purpose of this tutorial is to give an introduction to the characteristic properties of EVs and discuss how design automation can expand into areas which are, to date, untapped.

SPEAKERS:
Patrick Groeneveld - *Synopsys, Inc., Mountain View, CA*
Sebastian Steinhorst - *TUM CREATE Ltd., Singapore, Singapore*

Each Tutorial below is presented multiple times to allow you to cover multiple topics.
Special registration required.

TUTORIAL 5: ADVANCED DESIGN AUTOMATION METHODOLOGIES FOR NEXT-GENERATION POWER DELIVERY NETWORKS

Time: 10:30am - 12:00pm & 1:30 - 3:00pm || Room: 305
Track: EDA || Topic Area: Digital Circuits

ORGANIZERS:
Peng Li - *Texas A&M Univ., College Station, TX*
Zhuo Feng - *Michigan Technological Univ., Houghton, MI*
Cheng Zhuo - *Intel Corp., Hillsboro, OR*
Karthikeyan Ramamurthi - *Intel Corp., Folsom, CA*

Nanoscale integrated circuit designs are facing with ever-increasing power densities as well as rapidly-shrinking feature sizes, imposing grand challenges in designing reliable yet energy-efficient power delivery networks. This tutorial will introduce recent advances in design automation methodologies for next-generation power delivery networks by incorporating the latest circuit modeling, analysis and verification techniques.

The tutorial will start with early-stage power delivery network design issues that cover early-stage power grid extraction,modeling and optimization aspects. Next, scalable heterogeneous parallel circuit simulation techniques for large-scale power delivery networks will be presented. Additionally, state-of-the-art methodologies for verifying energy-efficient power delivery networks with integrated voltage regulators will be introduced. In the last, UPF/CPF based Low Power Design Methodology that can help designers successfully develop low-power designs will be introduced.

SPEAKERS:
Cheng Zhuo - *Intel Corp., Hillsboro, OR*
Zhuo Feng - *Michigan Technological Univ., Houghton, MI*
Peng Li - *Texas A&M Univ., College Station, TX*
Karthikeyan Ramamurthi - *Intel Corp., Folsom, CA*

TUTORIAL 6: BUILDING SECURE HARDWARE AND SOFTWARE SYSTEMS

Time: 10:30am - 12:00pm & 1:30 - 3:00pm || Room: 300
Track: Security || Topic Area: Security

Building a secure system is an important but challenging task. System builders, who have traditionally focused on performance, power, and cost, must today be equally concerned with hardening their system against the myriad of hardware and software vulnerabilities that lead to security exploits.

In this tutorial, we will first examine a wide variety of hardware and software exploits that exist today. Then, we will explore design techniques (both preemptive and reactive) that can protect systems from being attacked. Special emphasis will be given on how hardware designers compiler/runtime developers can contribute to the development of secure systems.

SPEAKERS:
Todd Austin - *Univ. of Michigan, Ann Arbor, MI*
Jin Yang - *Intel Corp., Portland, OR*

TUTORIAL 7: ARCHITECTURE AND DESIGN OF ENERGY EFFICIENT HETEROGENEOUS MULTI-CORE PLATFORMS

Time: 1:30 - 3:00pm || Room: 301
4:30 - 6:00pm || Room: 304
Track: Embedded Systems || Topic Area: Embedded System Architecture and Design

ORGANIZER:
Alan Gibbons - *Synopsys, Inc., Reading, United Kingdom*

Energy efficiency is one of the primary design metrics for heterogeneous multi-core mobile compute platforms. These compute platforms comprise complex software and hardware architectures as well as multi-layered system power management and the energy efficiency of the platform will be determined by the way in which these components interact under real software load.

Decisions made early in the platform development cycle will yield the greatest impact in terms of energy efficiency, hence it is essential to address this at the system level. Energy aware system level design techniques and methodologies enable concurrent optimization of the hardware, software and system power management aspects of the platform. Since the way in which a platform is used determines its energy consumption, it is vital that we understand the energy profile of the platform under software load. Once there is visibility into this energy profile, intelligent architecture and design decisions can then be made that consider the associated performance and power trade-offs to improve energy efficiency of the platform.

IP power models can provide this level of visibility into the energy behavior of the platform and are critical in enabling this design methodology. The use of IP power models during system level design allows exploration of the power impact of various hardware and software architectures, as well as to dynamically tune system resources and power management strategies for optimal energy efficient performance.

This tutorial will highlight the challenges associated with energy efficient platform design, the energy aware system level design tools and methodologies that can be used to deal with these challenges, as well as the IP power characterization and modelling approaches that enable these methodologies.

SPEAKERS:
Alan Gibbons - *Synopsys, Inc., Reading, United Kingdom*
Vita Vishnyakov - *Microsoft Corporation, Redmond, WA*
Krishna Sekar - *Qualcomm, Inc., San Diego, CA*

TUTORIAL 8: ADVANCES IN POST SILICON DIAGNOSIS TECHNOLOGIES IN NANO-SCALE ERA

Time: 1:30 - 3:00pm || Room: 302
4:30 - 6:00pm || Room: 305
Track: EDA || Topic Area: Test and Verification

ORGANIZER:
Enamul Amyeen - *Intel Corp., Hillsboro, OR*

Post silicon diagnosis drives the isolation of manufacturing defects and provides feedbacks for process improvement and is critical for enabling Moore's law and semiconductor technology scaling. Due to the increasing complexity of nano-scale manufacturing fabrication, the need for faster root-cause of issues is essential for volume production ramp to meet the product time to market demand. Over the last several years,many innovations have been made and novel solutions are emerging for better and faster defect isolation. With the advent of new transistor devices, lithography, and fabrication processes, the demand for improving the defect isolation and faster yield learning will continue to grow in coming years.

In this tutorial, we will review the basics of diagnosis approaches, and advancements in post silicon diagnosis field. In addition to diagnosis quality improvement, increased focus has been made to volume processing of diagnosis results for yield learning. This has resulted in introduction of new DFT technologies to obtain and process massive amount of fail data, and to provide better controllability and observability of failures to narrow down the defect suspects. Diagnosis algorithms are optimized to provide speed-ups in analysis time. Advancements are made in fault modeling to abstract the complex defect behavior and logical analysis of failures are being incorporated with layout analysis for finer pruning of diagnosis candidates. Hybrid approach of using logical simulation in conjunction with circuit simulation resulted in better isolation of front end and backend defects. Along with diagnosis technology improvements, complementary efforts have been geared towards customized test content to improve diagnostic resolution. We will review emerging techniques of learning based diagnosis approach which combining with process sensitivity, DFM constraints, and lithography simulation will be the key for driving the innovations for future technology generations.

The tutorial is intended for engineers and test practitioners including academics working in test and diagnosis, post silicon debug, fault isolation, failure analysis, and manufacturing yield.
The DAC audience will get the opportunity to know the state of the art diagnosis technologies, and how they are shaping the design and process evolution and manufacturing yield learning in nano-scale era.

SPEAKERS:
Shawn Blanton - *Carnegie Mellon Univ., Pittsburgh, PA*
Enamul Amyeen - *Intel Corp., Hillsboro, OR*
Srikanth Venkataraman - *Intel Corp., Hillsboro, OR*

Each Tutorial below is presented multiple times to allow you to cover multiple topics.
Special registration required.

TUTORIAL 9: INTRODUCTION TO HARDWARE AND EMBEDDED SECURITY

Time: 1:30 - 3:00pm || Room: 303
4:30 - 6:00pm || Room: 300
Track: Security || Topic Area: Security

ORGANIZERS:
Ramesh Karri - *New York Univ., New York, NY*

Globalization of Integrated Circuit (IC) design is making designers and users of IC and Intellectual Property (IP) re-assess their trust in hardware. Driven by cost-conscious consumer electronics, IC design flow spans the globe. Within this context, hardware is increasingly prone to side channel analysis, reverse engineering, IP piracy and malicious modifications (i.e. hardware trojans). An attacker, anywhere within the design flow, can reverse engineer the functionality of an IC/IP, steal and claim ownership of the IP or introduce counterfeits into the supply chain. Moreover, an untrusted IC fab may overbuild ICs and sell them illegally. Finally, rogue elements in a fab may insert hardware trojans into the design without the knowledge of the designer or the end-user of the IC; these backdoor functionality may be exploited to introduce errors in the results,steal sensitive information or incapacitate a fielded system.

Tutorial Topics:
Design and test of novel security primitives. Process variation and device aging play fundamental roles in hardware and system security. They enable powerful new security primitives such as physical unclonable functions (PUFs), public PUFs (PPUFs), truerandom number generators (TRNG) and silicon odometers to meter device usage. This part of the tutorial will survey design and test approaches for these hardware security primitives as well. This part of the tutorial will cover (i) Background and motivation forhardware based primitives (i) PUFs (ii) PPUFs (iii) random number generators (iv) silicon odometers to meter device usage (v) Open challenges; (30 minutes, Miodrag Potkonjak)

Hardware Trojans and Counterfeits:
The migration from a vertical to horizontal business model has made it easier to introduce hardware Trojans and counterfeit electronic parts into the electronic component supply chain. Hardware Trojans are malicious modifications made to original IC designs that reduce system integrity (change functionality, leak private data, etc.). Counterfeit parts are often below specification and/or of substandard quality. The existence of Trojans and counterfeit parts creates risks for the life-critical systems and infrastructures that incorporate them including automotive, aerospace, military, and medical systems. This part of the tutorial will cover(i) Background and motivation for hardware Trojan and counterfeit prevention/ detection;(ii) Hardware Trojan and detection Taxonomies (iii) Counterfeit hardware taxonomies ;(iii) Existing solutions; (iv) Open challenges; (30 minutes, Mark Tehranipoor)

Silicon Roots of Trust: Minimal Foundations for On-Chip Security
First proposed at the system-level in part as a way to address challenges associated with achieving higher assurances in large, complex systems, the Root of Trust concept is being embraced by a semiconductor industry whose products are growing to be equally large and complex,if not more than the systems they power. This part of the tutorial will explore the Root of Trust concept applied to semiconductors and semiconductor IP lifecycle, motivating factors, real world examples, security goals and challenges. (30 minutes, Ron Perez)

SPEAKERS:
Mark Tehranipoor - *Univ. of Connecticut, Storrs, CT*
Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*
Ronald Perez - *Cryptography Research, Inc., San Francisco, CA*

KEYNOTE PRESENTATIONS

VISIONARY TALK - MOORE'S LAW AT FIFTY: NO END IN SIGHT

Vivek Singh - *Intel Fellow, Intel Corp., Hillsboro, OR*

9:00 - 9:15am || Room: Gateway Ballroom
Track: Silicon Design || Topic Area: General Interest

Summary: Moore's Law is an observation that a transistor – the fundamental building block of the digital age – will decrease in cost at a steady, exponential rate. This decrease in cost as well as transistor size over the past 50 years has also led to dramatic increases in compute power and energy efficiency and transformed our world with ever-more powerful smart phones, tablets, personal computers and data centers. It has also enabled computing to become a powerful yet invisible force in our homes, offices, cars, factories and much more. These imperatives are the reason Moore's Law will continue, and motivated teams will continue to find innovative solutions to the engineering challenges of the day, just as they have in the past. This talk will provide some examples of how complex problems have been overcome in recent technology nodes, including those from the field of Computational Lithography. Inverse Lithography and Source Mask Optimization are two such examples that have helped extend the life of 193 patterning. Such innovations, fed by a rich technology pipeline, give us confidence that Moore's Law will continue.

Biography: Vivek Singh is an Intel Fellow and director of computational lithography in Intel's Technology and Manufacturing Group.

He is responsible for all of Intel's CAD and modeling tool development in full chip OPC, lithography verification, rigorous lithography modeling, next-generation lithography selection, inverse lithography technologies and double patterning. He also represents Intel on several external Design for Manufacturability (DFM) forums, and is currently President of the Lithography Workshop.
He holds over 20 patents, has published over 50 technical papers and he and his team have won Four Intel Achievement Awards.

Singh graduated from the Indian Institute of Technology in Delhi with a bachelor's degree in chemical engineering in 1989. He earned a master's degree in chemical engineering in 1990, a Ph.D. minor in electrical engineering in 1993, and a Ph.D. in chemical engineering in 1993, all from Stanford University.

KEYNOTE - THE DESIGN OF INNOVATION THAT DRIVES TOMORROW

Jeffrey Owens - *Chief Technology Officer and Executive Vice President, Delphi Automotive, Troy, MI*

9:15 - 10:00am || Room: Gateway Ballroom
Track: Automotive || Topic Area: Embedded System Architecture and Design

Summary: When people think of high tech devices, they rarely think of their cars, trucks or vans. Similar to the computational power of the human brain, today's vehicles possess more processing power than anything most consumers own or will purchase. A typical car is equipped with more than 50 computers designed to operate at automotive grade capabilities for an extended period of time. Vehicle manufacturers and automotive suppliers around the world are responding to a myriad of consumer preferences and regulatory initiatives -- including enhanced safety features, increased fuel economy, reduced emissions and connectivity. Vehicles of the future will require increased amounts of embedded software and electrical/electronic systems. Addressing this dynamic will require significant design automation aids to handle extreme complexity. Electronics and design automation will play a critical role in shaping the future of automotive by providing design technology that helps save lives, protect the environment and provide a satisfying in-car experience for drivers and passengers alike.

Biography: Jeffrey J. Owens is chief technology officer and executive vice president of Delphi Automotive, a $17B global automotive systems supplier. Owens is responsible for the enterprise information technology function and Delphi's global engineering organization, which includes more than 19,000 technologists located in 15 major technical centers. Owens leads the company's innovation strategies while driving advanced technologies supporting the global megatrends of safe, green and connected. Owens has served in a variety of engineering, manufacturing, finance and product line assignments. He served as president of Delphi Asia Pacific from 2006 to 2009. In his most recent assignment, Owens served as president of Delphi's Electronics & Safety division, establishing key growth product lines including active safety, power electronics for EV/HEVs and consumer connectivity electronics. Owens earned a bachelor's degree in engineering from Kettering University and a master's degree in business from Ball State University. He currently serves as chairman of the Kettering University Board of Trustees.

MANAGEMENT DAY AT DAC

Time: 10:30am - 4:00pm || Room: 309
Track: EDA || Topic Area: Business

ORGANIZERS:
Natesan Venkateswaran - *IBM Corp., Hopewell Junction, NY*
Yervant Zorian - *Synopsys, Inc., Mountain View, CA*

While our research papers dive into algorithms, our designer track addresses the nifty details of every day design and development work, DAC also offers a program just at the right level for Executives. Management Day provides senior executives and managers with timely information to help them make decisions where business and technology intersect. This is a unique opportunity for managers to gain insights from their peers in the industry.

The Internet of Things (IoT) has immense impact on the semiconductor industry: billions of devices connected to central cloud systems, devices connected to humans and devices connected to each other. It covers a variety of applications, including home automation, transportation, environmental monitoring, and medical devices to just name a few. These devices will produce massive amounts of data that will require innovative approaches to Big Data. Analytics will be a key part of Management Day. The design requirements result in several new approaches and innovative methods that work together to enable the network of smart devices and to ensure low power applications. The short shelf life of most IoT devices requires increased productivity and efficient design closure to meet the compressed market windows.

SESSION 1: BIG DATA ANALYTICS IN EDA

Time: 10:30am-12:00pm

With Million+ gate designs becoming the norm rather than the exception, EDA tools are dealing with Big Data. Each tool run produces several tens or even hundreds of diagnostic reports and logfiles that can run to thousands of lines. Due to the sheer volume of data, useful information in these reports and logfiles goes unanalyzed, causing unnecessary design churn. The result is significant loss in productivity. It is high time that the EDA industry put some serious focus on Analytics techniques to help with efficient design closure. This panel brings leading experts from both within and outside the EDA industry who will share their perspectives on Big Data strategy and implementation.

MODERATOR:
Ron Collett - *President & CEO, NMX Global Software, Inc, Cupertino, CA*

PANELISTS:
Dean Drako - *CEO & President, IC Manage, Campbell, CA*
Leon Stok - *Vice President, Electronic Design Automation Technologies, IBM Corporation, Hopewell Junction, NY*
Harnhua Ng - *Co-founder & Vice President of Engineering, Plunify, Singapore, Singapore*
Yaron Kretchmer - *Director of Engineering, Qualcomm Technologies, San Diego, CA*
Sanjay Mathur - *Co-founder & CEO, Silicon Valley Data Science, Mountain View, CA.*

SESSION 2: TRADE-OFFS AND DECISION MAKING FOR EMERGING CHIPS

Time: 2:00-4:00pm

Today's emerging chips have different sets of requirements depending on their applications. The design requirements for very high volume IoT chips are very different than the ones for complex networking applications. These can significantly affect the choice of design flow, methodologies, suppliers, while meeting numerous constraints, including export compliance constraints. This session will cover the design challenges of such emerging chips using examples from IoT up to networking chips, and present corresponding management decision criteria that allow managers to make the right choices from a pool of alternate options, while complying with numerous constraints. This session feature presentations by senior managers representing a range of emerging chip companies and solution providers.

SPEAKERS
Mojy Chian - *CEO, Silicon Cloud International, Singapore, Singapore*
Bill Eklow - *Distinguished Engineer, Cisco Systems, Inc., San Jose, CA*
Sohail Syed - *Senior Director, Marvell Technology Group Ltd., San Jose, CA*
Larry Disenhof - *EDAC Export Committee Chair; Group Director, Cadence Design Systems, Inc., San Jose, CA*
Karthik Laggisetty - *Export Research and Compliance Specialist, Intel Corp., Santa Clara, CA*

10 - SPECIAL SESSION: THE RESEARCHER WHO CRIED WOLF

Time: 10:30am - 12:00pm || Room: 300 || Track: Security || Topic Area: Security

CHAIR:
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
ORGANIZER:
Yier Jin - *Univ. of Central Florida, Orlando, FL*

Consumers are enjoying the convenience offered by the increased deployment of smart devices. Despite repeated warnings from researchers decrying the lack of security and prevalent privacy concerns, very little efforts have been made to secure these smart devices and the network connecting them. Hitherto, the lack of research effort and industry attention has been justified, as attacks have remained largely academic. However, the wolf has come.

In this section, security researchers from both industry and academia will show advanced hacking tools, compromised of smart devices, and hardware Trojans in industrial devices. Demos will be presented to show vulnerabilities of smart devices.

Each presentation will be 22 minutes.

10.1 Hacking the Wireless World with Software Defined Radio – 2.0 (10:30)
Balint Seeber - *Spench.net, San Francisco, CA*

10.2 The Internet of Things (IoT) - The Hidden Danger Exposed (10:50)
Moshe Ben Simon - *TrapX, San Francisco, CA*

10.3 How to Build Hardware Trojans in Industrial Products (11:10)
Georg Becker - *Ruhr Univ. Bochum, Germany*

10.4 Hack-All-The-Things (11:30)
Amir Etemadieh - *GTVHacker, Austin, TX*

11 - SPECIAL SESSION: MODELING, SIMULATION, AND TESTING FOR AUTOMOTIVE EMBEDDED SYSTEMS

Time: 10:30am - 12:00pm || Room: 303 || Track: Automotive || Topic Area: Embedded Software

CHAIR:
Rolf Ernst - *Technische Univ. Braunschweig, Germany*
ORGANIZERS:
Henry Broodney - *IBM Corp., Haifa, Israel*
Wolfgang Ecker - *Infineon Technologies AG, Neubiberg, Germany*

Tacking the increasing complexity of automotive in-vehicle hardware/software architectures calls for innovative modeling and analysis techniques. Here, model-based approaches often need to work at multiple levels of abstraction and take a holistic view of hardware/software architectures in order to provide acceptable solutions. Often, models and simulation techniques need to constructed from operational data and the approaches followed by OEMs, who mostly have to carry out integration, and the suppliers, are different. This session will feature three talks that discuss such approaches from the perspectives of both OEMs and suppliers.

11.1 A Model-Based and Simulation-Assisted FMEDA Approach for Safety-Relevant E/E Systems (10:30)
Moomen Chaari, Wolfgang Ecker, Cristiano Novello, Bogdan-Andrei Tabacaru, Thomas Kruse - *Infineon Technologies AG, Neubiberg, Germany*

11.2 Evaluation of Functional Mock-up Interface for Vehicle Power Network Modeling (11:00)
Kenji Nishimiya, Toru Saito, Satoshi Shimada - *Honda R&D Co., Ltd., Tohigi, Japan*

11.3 System Simulation from Operational Data (11:30)
Armin Wasicek, Edward Lee - *Univ. of California, Berkeley, CA*
Lev Greenberg - *IBM Corp., Haifa, Israel*
Akihito Iwai - *DENSO International America, Inc., San Jose, CA*
Ilge Akkaya, Hokeun Kim - *Univ. of California, Berkeley, CA*

12 - SPECIAL SESSION: IT'S ALL IN THE MARGINS

Time: 10:30am - 12:00pm || Room: 304 || Track: EDA || Topic Area: Physical Design

CHAIR:
Brian Cline - *ARM Ltd., Austin, TX*

ORGANIZER:
Rob Aitken - *ARM, Inc., San Jose, CA*

Timing closure, product performance, yield, test complexity and more are all wrapped up in margins. How do they work and what are people doing with them?

12.1 New Game, New Goal Posts: A Recent History of Timing Closure (10:30)
Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*

12.2 Adaptive Circuits for Mitigating Dynamic Variation Margins (11:00)
Keith Bowman - *Qualcomm, Inc., Raleigh, NC*

12.3 Walking A Thin Line - Performance and Quality Grading Accuracy vs. Yield Overcut (11:30)
Carl Bowen - *Advanced Micro Devices, Inc., Austin, TX*

13 - NOC YOUR SOCS OFF

Time: 10:30am - 12:00pm || Room: 305 || Track: EDA || Topic Area: System-on-Chip Design

CHAIR:
Siddharth Garg - *New York Univ., New York, NY*
CO-CHAIR:
Sudeep Pasricha - *Colorado State Univ., Fort Collins, CO*

Let us show you some exciting ways and technologies to optimize your NoCs that will knock your SoCs into shape! This session takes a holistic view of NoCs from diverse and interrelated angles. We start with communication enhancements with novel wireless and optical interconnects. We accelerate along with techniques to improve communication performance and energy in GPU-like multicore architectures. Finally we explore the integration of emerging non-volatile memory buffer architectures with NoCs.

13.1 Energy Efficient MapReduce with VFI-Enabled Multicore Platforms (10:30)
Karthi Duraisamy, Ryan Kim, Wonje Choi - *Washington State Univ., Pullman, WA*
Guangshuo Liu - *Carnegie Mellon Univ., Pittsburgh, PA*
Partha Pande - *Washington State Univ., Pullman, WA*
Diana Marculescu, Radu Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

13.2 Complementary Communication Path for Energy Efficient On-Chip Optical Interconnects (10:45)
Hui Li, Sébastien Le Beux - *École Centrale de Lyon, France*
Yvain Thonnart - *Univ. Grenoble Alpes - CEA, LETI, Grenoble, France*
Ian O'Connor - *Lyon Institute of Nanotechnology, Ecully, France*

13.3 On-chip Interconnection Network for Accelerator-Rich Architectures (11:00)
Jason Cong, Michael Gill, **Yuchen Hao**, Glenn Reinman, Bo Yuan - *Univ. of California, Los Angeles, CA*

13.4 Bandwidth-Efficient On-Chip Interconnect Designs for GPGPUs (11:15)
Hyunjun Jang, Jinchun Kim, **Paul Gratz**, Ki Hwan Yum, Eun Jung Kim - *Texas A&M Univ., College Station, TX*

13.5 DimNoC: A Dim Silicon Approach Towards Power-Efficient On-Chip Network (11:30)
Jia Zhan - *Univ. of California, Santa Barbara, CA*
Jin Ouyang - *NVIDIA Corporation, Santa Clara, CA*
Fen Ge - *Nanjing Univ. of Aeronautics and Astronautics, Nanjing, China*
Jishen Zhao - *Univ. of California, Santa Cruz, CA*
Yuan Xie - *Univ. of California, Santa Barbara, CA*

13.6 Domain-Wall Memory Buffer for Low-Energy NoCs (11:45)
Donald E. Kline, Jr, Haifeng Xu, Rami Melhem, Alex K. Jones - *Univ. of Pittsburgh, PA*

Q & A Poster Session
12:00 - 12:30pm - Esplanade Foyer

14 - MEMORIES FROM BEHIND BARS

Time: 10:30am - 12:00pm || Room: 310 || Track: EDA || Topic Area: Emerging Technologies

CHAIR:
Subhasish Mitra - *Stanford Univ., Stanford, CA*
CO-CHAIR:
Dimin Niu - *Samsung Electronics Co., Ltd., Sunnyvale, CA*

This session explores resistive RAM crossbars and other memory technologies, including CAD framework and design techniques for neuromorphic computing, memory test procedure for carbon-nanotube FET, and a configurable analog circuit for solving the max-flow problem.

14.1 An EDA Framework for Large Scale Hybrid Neuromorphic Computing Systems (10:30)
Wei Wen - *Univ. of Pittsburgh, PA*
Chi-Ruo Wu - *National Cheng Kung Univ., Tainan, Taiwan*
Xiaofang Hu - *City Univ. of Hong Kong, Hong Kong*
Beiye Liu - *Univ. of Pittsburgh, PA*
Tsung-Yi Ho - *National Chiao Tung Univ., Hsinchu, Taiwan*
Xin Li - *Carnegie Mellon Univ. and Fudan Univ., Pittsburgh, PA*
Yiran Chen - *Univ. of Pittsburgh, PA*

14.2 Merging the Interface: Power, Area and Accuracy Co-Optimization for RRAM Crossbar-Based Mixed-Signal Computing System (10:45)
Boxun Li, Lixue Xia, Peng Gu, Yu Wang, Huazhong Yang - *Tsinghua Univ., Beijing, China*

14.3 A Spiking Neuromorphic Design with Resistive Crossbar (11:00)
Chenchen Liu, Bonan Yan, Chaofei Yang, Linghao Song, Zheng Li, Beiye Liu - *Univ. of Pittsburgh, PA*
Qing Wu - *Air Force Research Lab, Rome, NY*
Hao Jiang - *San Francisco State Univ., San Francisco, CA*
Yiran Chen, Hai Li - *Univ. of Pittsburgh, PA*

14.4 Vortex: Variation-Aware Training for Memristor X-Bar (11:15)
Beiye Liu - *Univ. of Pittsburgh, PA*
Xin Li - *Carnegie Mellon Univ. and Fudan Univ., Pittsburgh, PA*
Qing Wu - *Air Force Research Lab, Rome, NY*
Tingwen Huang - *Texas A&M Univ., College Station, TX*
Hai Li, Yiran Chen - *Univ. of Pittsburgh, PA*

14.5 Jump Test for Metallic CNTs in CNFET-Based SRAM (11:30)
Feng Xie, Xiaoyao Liang - *Shanghai Jiao Tong Univ., Shanghai, China*
Qiang Xu - *Chinese Univ. of Hong Kong, Hong Kong*
Krishnendu Chakrabarty - *Duke Univ., Durham, NC*
Naifeng Jing, **Li Jiang** - *Shanghai Jiao Tong Univ., Shanghai, China*

14.6 A Reconfigurable Analog Substrate for Highly Efficient Maximum Flow Computation (11:45)
Gai Liu, Zhiru Zhang - *Cornell Univ., Ithaca, NY*

*** Indicates Best Paper Candidate**

Q & A Poster Session
12:00 - 12:30pm - Esplanade Foyer

15 - IP VERIFICATION

Time: 10:30 - 11:30am || Room: 101
Track: IP || Topic Area: Designer and IP Track

Sponsored by: ChipEstimate.com

CHAIR:
Warren Savage - *IPextreme, Campbell, CA*

With the complexity of semiconductor IP increasing every year, the verification strategies and techniques required to deal with this complexity are under continuous pressure to keep up. To verify modern SoC's and complex IP subsystems, a diversity of methods, tools, and approaches is often needed.

In this session you will hear real world examples of innovative and practical approaches described by the designers who employed these techniques in their design projects. Immediately following this session is a panel with representatives from companies providing verification technology will discuss their experiences and perspectives on the topic of IP verification.

*** Indicates Best Paper Candidate**

15.1 Testbench Improvisation Recipe for Verification Sign-Off to Ensure Bug-Free Designs (10:30)
Deepmala Sachan, Thameem Syed D, Raghavendra Prakash, Venugopal Jennarapu - *Intel Corp., Bangalore, India*

15.2 Simulation & Modeling of DDR4 Memory Interface and Interposer Test Fixtures (10:45)
Philip Pun - *Cadence Design Systems, Inc., San Jose, CA*
Chung-Chi Huang - *Cadence Design Systems, Inc., San Jose, CA*

15.3 Why Testbench Should Control Processor Execution: "A Novel Approach to Bridge the Gap Between IP and SoC Verification"* (11:00)
Gaurav Gupta, Tejbal Prasad, Rohit Goyal, Sachin K. Jain, **Ritesh Agrawal** - *Freescale Semiconductor, Inc., Noida, India*

15.4 IP-MAP Tool for Design Verification & Validation (11:15)
Aji Varghese - *Texas Instruments, Inc., Dallas, TX*

Q & A Poster Session
4:30 - 6:00pm - Exhibit Floor

16 - KEY CHALLENGES OF VERIFICATION AND VALIDATION OF MODERN SEMICONDUCTOR IP

Time: 11:30am - 12:00pm || Room: 101
Track: IP || Topic Area: Test and Verification

Sponsored by: ChipEstimate.com

MODERATOR:
Brian Bailey - *Semiconductor Engineering, Beaverton, OR*
ORGANIZER:
Warren Savage - *IPextreme, Campbell, CA*

This panel of respected experts will discuss the key challenges of verification and validation of modern semiconductor devices. Topic areas will include verification IP, reusable test benches, best practices for using assertions, hardware prototyping, accelerated models, and emulation. The theme of the panel will be related to how these techniques can be best applied in today's IP-based design methodologies.

PANELISTS:
Tom Anderson - *Breker Verification Systems, Inc., San Jose, CA*
Toshio Nakama - *S2C, Inc., San Jose, CA*
Bernie Delay - *Synopsys, Inc., Hillsboro, OR*
Raik Brinkmann - *OneSpin Solutions GmbH, Munich, Germany*
Frank Schirrmeister - *Cadence Design Systems, Inc., San Jose, CA*

17 - DESIGNER TRACK: PLANAR TO FINFET

Time: 10:30am - 12:00pm || Room: 105
Track: EDA || Topic Area: Designer and IP Track

Sponsored by: Mentor Graphics

CHAIR:
Yatin Trivedi - *Synopsys, Inc., Mountain View, CA*

As planar transistor technology hit device scaling limits at 20nm, FinFET was introduced to move to smaller geometries. FinFET brings a significant performance increase at suppressed leakage current dissipation. At the same time FinFET has introduced new challenges:

- Device drive strength selection is limited by Fin count granularity
- The vertical nature of FinFET transistors lead to a significant increase in cell input capacitance which forces logic cell usage to be reconsidered.
- Both FIN quantization and input capacitance can lead to an increase in dynamic power.
- Lag in metal design rule scaling due to more stringent DFM rule requirements.
- Ever increasing logic power densities in complex SOCs combined with increasing metal resistances increase the metal resource overhead to provide a robust power distribution for SOCs, which in turn puts additional pressure on signal routing congestion and achievable gate densities.

In this session we'll explore the benefits and challenges with FinFET adoption.

17.1 FinFET Design Tools and Flows – Why Do You Need It! How Do You Get It? (10:30)
Kuang-Kuo Lin - *Samsung Electronics America, Inc., Milpitas, CA*

17.2 FinFET Implementation Roller Coaster - What Is Not So Planar (11:00)
Benjamin Mbouombouo - *Avago Technologies, San Jose, CA*

17.3 Seeing Double? How Multiple Patterning Affects FinFET Designs at 16nm/14nm and Beyond (11:30)
Brian Cline - *ARM, Inc., Austin, TX*

SKY TALK: VIRTUAL TO THE (NEAR) END - USING VIRTUAL PLATFORMS FOR CONTINUOUS INTEGRATION

Time: 1:00 - 1:30pm || Room: Booth 311
Track: Embedded Systems || Topic Area: Embedded Software

CHAIR:
Rob Oshana - *Freescale Semiconductor, Inc., Austin, TX*

Continuous integration (CI) is a hot topic in software development. CI make sure code is tested quickly and integrated incrementally, enabling Agile methods, higher quality software, and higher development velocity. Using virtual platforms along with other simulators, it is possible to broadly enable CI for both new hardware designs and existing embedded systems that would otherwise be considered difficult targets for CI. In this talk, we will cover how to enable CI using simulation, and some examples of how simulation-based CI has been used in the telecom and aerospace industries.

SPEAKER:
Jakob Engblom - *Wind River Systems, Inc., Kista, Sweden*

18 - PANEL: DESIGN FOR HARDWARE SECURITY: CAN YOU MAKE CENTS OF IT?

Time: 1:30 - 3:00pm || Room: 300 || Track: Security || Topic Area: Security

MODERATOR:
Saverio Fazzari - *Defense Advanced Research Projects Agency, Washington, DC*

ORGANIZER:
Saverio Fazzari - *Defense Advanced Research Projects Agency, Washington, DC*

Given the proliferation of counterfeit electronics in the supply chain, recent breaches at major retailers and the ever-growing Internet of Things, there is evidence that electronic hardware is the “new frontier” for security compromise. Yet the protection of hardware continues to take a back seat to software in cyber-defense.

How real is the problem of hardware security? Should there be a stronger push to develop and deploy security techniques in design? Finally, is there money to be made in hardware security? Who benefits and who pays?

PANELISTS:
Ingrid Verbauwhede - *Katholieke Univ. Leuven, Belgium*
Siva G. Narendra - *Tyfone, Inc., Portland, OR*
Vincent Zimmer - *Intel Corp., Seattle, WA*
Dino A. Dai Zovi - *New York Univ., New York, NY*
Lisa McIlrath - *Raytheon BBN Technologies, Cambridge, MA*

19 - SPECIAL SESSION: AUTOMOTIVE ARCHITECTURE AND NETWORKS JUNGLE

Time: 1:30 - 3:00pm || Room: 303 || Track: Automotive || Topic Area: Automotive Systems

CHAIR:
Huafeng Yu - *Toyota Motor Corp., Mountain View, CA*

Modern cars today consist of more than 100 electronic control units (ECUs) connected by a complex communication architecture with CAN, FlexRay, Ethernet and a variety of other technologies and gateways. Designing and analyzing such a complex and heterogeneous architecture, ensuring robustness, reliability and isolation between various applications poses a number of technical challenges, some of which are going to be discussed in this session.

19.1 The Convergence of Multiple Vehicle Networks: How to Select One Network Over the Other and the Ensuing Challenges (1:30)
Andrew Patterson - *Mentor Graphics Corp., Wilsonville, OR*

19.2 Robust Design of E/E Architecture Component Platforms (2:00)
Sebastian Graf, Sebastian Reinart, Michael Glaß - *Univ. Erlangen-Nürnberg, Erlangen-Nurnberg, Germany*
Jürgen Teich - *Univ. of Erlangen-Nuremberg, Germany*
Daniel Platte - *Audi AG, Ingolstadt, Germany*

19.3 HW/SW Trade-Offs in I/O Virtualization for Controller Area Network (2:30)
Christian Heber - *Technische Univ. München, Germany*
Dominik Reinhardt - *BMW AG, Munich, Germany*
Andre Richter, **Andreas Herkersdorf** - *Technische Univ. München, Germany*

20 - SPECIAL SESSION: BUILD YOUR OWN? WHY NOT!

Time: 1:30 - 3:00pm || Room: 304
Track: Embedded Systems || Topic Area: Emerging Technologies

CHAIR:
Dominic Pajak - *ARM, Inc., San Jose, CA*
ORGANIZER:
Rob Aitken - *ARM, Inc., San Jose, CA*

There has been a lot of recent interest in the Maker movement. This session shows three ways that you too could build your own electronic products, from using a customizable computer as the base of a system, to 3D printing your desired object, to using plastics to print your own circuits. Learn what you could build!

20.1 Build Your Own System: The Story of OTTO (1:30)
Dave Rauchwerk - *Next Thing Co., San Francisco, CA*

20.2 Build Your Own Product – 3D Printing (2:00)
Matthew Bennett - *Type A Machines, San Francisco, CA*

20.3 Build Your Own Chip - Plastic ICs (2:30)
Jacob Sadie - *Univ. of California, Berkeley, CA*

21 - FOND MEMORIES

Time: 1:30 - 3:00pm || Room: 305
Track: Embedded Systems || Topic Area: Embedded System Architecture and Design

CHAIR:
Mircea Stan - *Univ. of Virginia, Charlottesville, VA*
CO-CHAIR:
Danny Bathen - *Intel Corp., Santa Clara, CA*

Reliability is becoming an issue for DRAM and SRAM, as well as emerging memory such as STT-RAM, RRAM and domain wall memory. In this session, new techniques are proposed to increase energy efficiency and reliability of DRAM, RRAM and STT-RAM. Also, novel solutions to optimize domain wall memory, scratchpad memories and L1 caches are proposed.

21.1 RADAR: A Case for Retention-Aware DRAM Assembly and Repair in Future FGR DRAM Memory (1:30)
Ying Wang - *Chinese Academy of Sciences, Beijing, China*
Cheng Wang - *Chinese Academy of Sciences & Univ. of Chinese Academy of Sciences, Beijing, China*
Huawei Li, Yinhe Han, Xiaowei Li - *Chinese Academy of Sciences, Beijing, China*

21.2 Area and Performance Co-Optimization for Domain Wall Memory in Application-Specific Embedded Systems (1:45)
Shouzhen Gu, Edwin H.-M. Sha, Qingfeng Zhuge - *Chongqing Univ., Chongqing, China*
Jingtong Hu - *Oklahoma State Univ., Stillwater, OK*
Yiran Chen - *Univ. of Pittsburgh, PA*

21.3 Selective Restore: An Energy Efficient Read Disturbance Mitigation Scheme for Future STT-MRAM (2:00)
Rujia Wang, Lei Jiang, Youtao Zhang - *Univ. of Pittsburgh, PA*
Linzhang Wang - *Nanjing Univ., Jiangsu, China*
Jun Yang - *Univ. of Pittsburgh, PA*

21.4 Interleaved Multi-Bank Scratchpad Memories: A Probabilistic Description of Access Conflicts (2:15)
Andreas Tretter - *Eidgenössische Technische Hochschule Zürich, Switzerland*
Pratyush Kumar - *Swiss Federal Institute of Technology, Zurich, Switzerland*
Lothar Thiele - *Eidgenössische Technische Hochschule Zürich, Switzerland*

21.5 PRES: Pseudo-Random Encoding Scheme to Increase the Bit FlipReduction in the Memory (2:30)
Seyed Mohammad Seyedzadeh, Rakan Maddah, Alex K. Jones, Rami Melhem - *Univ. of Pittsburgh, PA*

21.6 Guidelines to Design Parity Protected Write-Back L1 Data Caches (2:45)
Yohan Ko - *Yonsei Univ., Seoul, Republic of Korea*
Reiley Jeyapaul - *Arizona State Univ., Tempe, AZ*
Youngbin Kim, Kyoungwoo Lee - *Yonsei Univ., Seoul, Republic of Korea*
Aviral Shrivastava - *Arizona State Univ., Phoenix, AZ*

Q & A Poster Session
3:00 - 3:30pm - Esplanade Foyer

22 - NOT YOUR FATHER'S DIGITAL IMPLEMENTATION

Time: 1:30 - 3:00pm || Room: 310 || Track: EDA || Topic Area: Physical Design

CHAIR:
Patrick Groeneveld - *Synopsys, Inc., Mountain View, CA*
CO-CHAIR:
Ismail Bustany - *Mentor Graphics Corp., Fremont, CA*

Physical design algorithms for placement, routing, and clocking have been around for half a century, so one might think there is nothing new in physical design. However, design flows have become increasingly challenging, requiring awareness of the complexities of timing, reconfigurability, incrementality, and DFM. This session presents two papers each in placement and clocking, one on routing, and one on power estimation, which integrate modern constraints and emerging technologies into their formulations. See how far PD has come since your dad did place and route!

22.1 Construction of Reconfigurable Clock Trees for MCMM designs (1:30)
Rickard Ewetz - *Purdue Univ., West Lafayette, IN*
Shankarshana Janarthanan - *NVIDIA Corporation, Santa Clara, CA*
Cheng-Kok Koh - *Purdue Univ., West Lafayette, IN*

22.2 A Global-Local Optimization Framework for Simultaneous Multi-Mode Multi-Corner Clock Skew Variation Reduction (1:45)
Kwangsoo Han - *Univ. of California at San Diego, La Jolla, CA*
Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*
Jong Pil Lee - *Samsung Electronics Co., Ltd., Yongin-City, Republic of Korea*
Jiajia Li, Siddhartha Nath - *Univ. of California at San Diego, La Jolla, CA*

22.3 Routing-Architecture-Aware Analytical Placement for Heterogeneous FPGAs (2:00)
Sheng-Yen Chen, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

22.4 PARR: Pin Access Planning and Regular Routing for Self-Aligned Double Patterning (2:15)
Xiaoqing Xu, **Bei Yu** - *Univ. of Texas at Austin, TX*
Jhih-Rong Gao - *Cadence Design Systems, Inc. & IEEE CEDA, Austin, TX*
Che-Lun Hsu, David Z. Pan - *Univ. of Texas at Austin, TX*

22.5 Local Search Algorithms for Timing Driven Placement under Accurate Delay Models (2:30)
Adrian A. Bock, **Stephan Held**, Nicolas Kämmerling, Ulrike Schorr - *Univ. of Bonn, Germany*

22.6 3D-IC Benefit Estimation and Implementation Guidance From 2D-IC Implementation (2:45)
Wei-ting Chan, Andrew B. Kahng, **Siddhartha Nath** - *Univ. of California at San Diego, La Jolla, CA*
Kambiz Samadi, Yang Du - *Qualcomm Technologies, Inc., San Diego, CA*

Q & A Poster Session
3:00 - 3:30pm - Esplanade Foyer

23 - IP STRATEGIES & MANAGEMENT

Sponsored by: ChipEstimate.com

Time: 1:30 - 2:30pm || Room: 101
Track: IP || Topic Area: Designer and IP Track

CHAIR:
Heather Monigan - *Intel Corp., Phoenix, AZ*

Deciding which IPs to buy, and which to build as you assemble today's SoC is not an exact science - experience plays a big part as you tend to continue to use IPs from vendors who have served you well in the past. Are their metrics you can use to assess a new IP provider? Are their classes of IP that it will just make sense to acquire from specialized vendors? How can you leverage your companies core design competency to create your own IPs for reuse? Attend this session to gather insight from other designs experiences in this area.

*** Indicates Best Paper Candidate**

23.1 Toward Predicting Verification Closure of IP Designs (1:30)
John Brennan - *Cadence Design Systems, Inc., Chelmsford, MA*
Jason Sprott - *Verilab Ltd., Edinburgh, United Kingdom*

23.2 MIPI Beyond Mobile: Which IP for IoT, Wearable and More?* (1:45)
Eric H. Esteve - *IP-nest, Marseille, France*

23.3 IP is Dead, Long Live IP (2:00)
Vishal Moondhra - *Methodics, Inc., Mountain View, CA*

23.4 What's in Your IP Wallet? (2:15)
Warren Savage - *IPextreme, Campbell, CA*

Q & A Poster Session
4:30 - 6:00pm - Exhibit Floor

24 - IP MANAGEMENT IN 2020

Sponsored by: ChipEstimate.com

Time: 2:30 - 3:00pm || Room: 101 || Track: IP || Topic Area: Business

MODERATOR:
John Blyler - *IP Systems, JB Systems Media, Portland, OR*
ORGANIZER:
Heather Monigan - *Intel Corp., Phoenix, AZ*

In this panel, the panel participants are asked to imagine what five years in the future looks like for IP Management. Given projected growth of the IP ecosystem as whole, in this not-so-distant world: does an IP or an IP segment dominate the market? Does the ecosystem remain a "Wild West" with a disjoint set of suppliers, or does a new segment emerge? Do IP subsystems conquer the market? What challenges would IP companies expect in this brave new world? What new management tools or techniques would be needed?

PANELISTS:
Martin Lund - *Cadence Design Systems, Inc., San Jose, CA*
John Koeter - *Synopsys, Inc., Austin, TX*
Krishna Yarlagadda - *Imagination Technologies Ltd., Sunnyvale, CA*
Suk Lee - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*

SKY TALK: THE PERFECT STORM: TRENDS IN FUNCTIONAL VERIFICATION

Time: 3:30 - 4:00pm || Room: Booth 311 || Track: EDA || Test and Verification

CHAIR:
Kevin Morris - *EE Journal, Portland, OR*

Between 2006 and 2014, the average number of IPs integrated into an advanced SoC increased from about 30 to over 120--while the average number of embedded processors increased from one to as many as 20. Yet, increased design size is only one dimension of the growing verification complexity challenge. Beyond basic functionality are new layers of requirements that must be verified—such as multiple clock domains, interacting power domains, security domains, and complex HW/SW interactions. Add all these challenges together, and you have the perfect storm brewing. This talk presents the latest trends in functional verification and then charts a course for navigating the perfect storm.

SPEAKER:
Harry D. Foster - *Mentor Graphics Corp., Wilsonville, OR*

25 - DESIGNER TRACK: INNOVATIVE FRONT-END DESIGN AND VALIDATION AT SYSTEM LEVEL

Time: 1:30 - 3:00pm || Room: 105
Track: Silicon Design || Topic Area: Designer and IP Track

Sponsored by: Mentor Graphics®

CHAIR:
Harsh Patel - *Mentor Graphics Corp., Fremont, CA*
CO-CHAIRS:
Erik Seligman - *Intel Corp., Hillsboro, OR*

With the increasing tension between accelerated delivery schedules and continual growth in design complexity, it has become critical for front-end teams to expand their focus from block-level analysis to the full scope of the system. Our speakers in this session have tackled a wide range of system-level issues, from instruction sets and high-level testbench design down to temperature-dependence at the system level. Come learn how you can improve your design and validation processes by taking these issues into account at the system level.

25.1 Enabling Efficient Validation of Temperature-Dependent System Behavior Through Co-Emulation (1:30)
Tanguy Sassolas, Caaliph Andriamisaina - *CEA-LIST, Gif-sur-Yvette Cedex, France*
Simone Bacles-Min, Pascal Vivet - *CEA-LETI, Grenoble, France*
Sylvian Kaiser, Nicolas Peltier, Hela Boussetta - *DOCEA Power Inc., Moirans, France*

25.2 SAE-Platform: A Platform for System Architecture Exploration* (1:45)
Qiang Wang - *Huawei Technologies Co., Ltd., Santa Clara, CA*
Fang Yu - *FutureWei Technologies, Inc., Santa Clara, CA*
Dezheng Zhan, Qiang Li, Liling Yuan, Junping Li, Ruiqing Chen - *Huawei Technologies Co., Ltd., Shanghai, China*

25.3 Creating Reusable UVM Testbenches for Seamless Transition Between Simulation & Emulation (2:00)
Parag Goel, Amit Sharma - *Synopsys (India) Pvt. Ltd, Bangalore, India*
Nathan Womack - *Synopsys, Inc., Mountain View, CA*

25.4 Walking the Graph: A Holistic Approach to Graph-Based Verification for Logic with Sparse State Space (2:15)
Holger Horbach, Klaus Keuerleber, Alexander Jung - *IBM Deutschland Research & Development GmbH, Böblingen, Germany*

25.5 Cosimulating SystemC Models and SystemVerilog UVM Test Bench Using UVMC Open Source Library in a WiFi Modem Verification Project (2:30)
Sadegh Jahanpour - *Qualcomm Technologies, Inc., San Diego, CA*
Sam Ng - *Qualcomm Atheros, Inc., San Jose, CA*
Lijun Li - *Qualcomm Technologies, Inc., San Diego, CA*

25.6 Automatic Generation & Integration Of Test Management Structure at SoC Level Using IP-XACT Methodology* (2:45)
Surat S. Devulapalli, Rakesh Gulati, Pankaj Panjwani, Rangarajan Ramanujam - *STMicroelectronics, Greater Noida, India*
Vivek Dhankhar - *Atrenta Inc., Noida, India*
Sanjeev Bansal - *Atrenta Inc., San Francisco, CA*

*** Indicates Best Paper Candidate**

Q & A Poster Session
4:30 - 6:00pm - Exhibit Floor

26 - BATTERIES NOT INCLUDED: SECURITY TECHNOLOGIES FOR EMBEDDED SYSTEMS

Time: 4:30 - 6:00pm || Room: 300 || Track: Security || Topic Area: Security

CHAIR:
Anand Rajan - *Intel Corp., Hillsboro, OR*
CO-CHAIR:
Leyla Nazhandali - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*

This session introduces new and advanced techniques for side channel analysis as well as for secure and trustworthy computation for embedded systems. Topics include fault analysis, side channel analysis, secure medical devices, and advances in secure architecture design and computation.

26.1 DERA: Yet Another Differential Fault Attack on Cryptographic Devices Based on Error Rate Analysis* (4:30)
Yannan Liu, Jie Zhang, Lingxiao Wei, Feng Yuan, Qiang Xu - *Chinese Univ. of Hong Kong, Hong Kong*

26.2 Vibration-Based Secure Side Channel for Medical Devices (4:45)
Younghyun Kim, Woo Suk Lee, Vijay Raghunathan - *Purdue Univ., West Lafayette, IN*
Niraj Jha - *Princeton Univ., Princeton, NJ*
Anand Raghunathan - *Purdue Univ., West Lafayette, IN*

26.3 Information Leakage Chaff: Feeding Red Herrings to Side Channel Attackers (5:00)
Giovanni Agosta, **Alessandro Barenghi**, Gerardo Pelosi, Michele Scandale - *Politecnico di Milano, Italy*

26.4 TyTAN: Tiny Trust Anchor for Tiny Devices (5:15)
Ferdinand Brasser, Brahim El Mahjoub - *Technische Univ. Darmstadt, Germany*
Patrick Koeberl - *Intel Corp., Darmstadt, Germany*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Christian Wachsmann - *Intel Collaborative Research Institute for Secure Computing, Darmstadt, Germany*

26.5 Memory Heat Map: Anomaly Detection in Real-Time Embedded Systems Using Memory Behavior (5:30)
Man-Ki Yoon, Sibin Mohan - *Univ. of Illinois at Urbana-Champaign, IL*
Jaesik Choi - *Ulsan National Institute of Science and Technology, Ulsan, Republic of Korea*
Lui Sha - *Univ. of Illinois at Urbana-Champaign, IL*

26.6 Compacting Privacy-Preserving k-Nearest Neighbor Search using Logic Synthesis (5:45)
Ebrahim M. Songhori, Siam U. Hussain - *Rice Univ., Houston, TX*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Farinaz Koushanfar - *Rice Univ., Houston, TX*

*** Indicates Best Paper Candidate**

Q & A Poster Session
6:00 - 7:00pm - Exhibit Floor

27 - ENERGY EFFICIENT, SAFE AND SECURE AUTOMOTIVE SOFTWARE AND SYSTEMS

Time: 4:30 - 6:00pm || Room: 303 || Track: Automotive || Topic Area: Automotive Systems

CHAIR:
Dirk Ziegenbein - *Bosch Research, Renningen, Germany*
CO-CHAIR:
Haibo Zeng - *Virginia Polytechnic Institute and State Univ., Blackburg, VA*

This session presents new exciting results on embedded automotive systems, architectures, and algorithms, covering a broad range of topics with an overall focus on energy efficiency, timeliness, safety and security.

During the session we discuss model-based analysis, and a novel algorithm that considers HVAC systems while improving the energy management of electric vehicles. We explore the security and safety analysis of complex networked systems using formal methods and provide design solutions for more secure communication systems. Finally, we cover analysis methods for real-time (Ethernet-based) networks and systems.

27.1 Battery Lifetime-Aware Automotive Climate Control for Electric Vehicles (4:30)*
Korosh Vatanparvar, Mohammad Abdullah Al Faruque - *Univ. of California, Irvine, CA*

27.2 Security Analysis of Automotive Architectures using Probabilistic Model Checking (4:45)
Philipp Mundhenk, Sebastian Steinhorst, Martin Lukasiewycz - *TUM CREATE Ltd., Singapore, Singapore*
Suhaib A. Fahmy - *Nanyang Technological Univ., Singapore, Singapore*
Samarjit Chakraborty - *Technische Univ. München, Germany*

27.3 Security Aware Network Controllers for Next Generation Automotive Embedded Systems (5:00)
Shanker Shreejith, Suhaib A. Fahmy - *Nanyang Technological Univ., Singapore, Singapore*

27.4 Analysis and RTL Correlation of Instruction Set Simulators for Automotive Microcontroller Robustness Verification (5:15)
Jaime Espinosa - *Univ. Politècnica de València, Spain*
Carles Hernandez, **Jaume Abella** - *Barcelona Supercomputing Center, Barcelona, Spain*
David de Andres, Juan Carlos Ruiz - *Technical Univ of Valencia, Spain*

27.5 Improving Formal Timing Analysis of Switched Ethernet by Exploiting FIFO Scheduling (5:30)
Daniel Thiele, Philip Axer, Rolf Ernst - *Technische Univ. Braunschweig, Germany*

27.6 Parallel Execution of AUTOSAR Legacy Applications on Multicore ECUs with Timed Implicit Communication (5:45)
Sebastian Kehr - *Denso Automotive Deutschland GmbH, Eching, Germany*
Eduardo Quinones - *Barcelona Supercomputing Center, Barcelona, Spain*
Bert Böddeker - *Denso Automotive Deutschland GmbH, Eching, Germany*
Günter Schäfer - *Technische Universität Ilmenau, Germany*

*** Indicates Best Paper Candidate**

Q & A Poster Session
6:00 - 7:00pm - Exhibit Floor

28 - PANEL: DOES DFM NOW STAND FOR "DON'T FORGET ABOUT ME"?

Time: 4:30 - 6:00pm || Room: 304 || Track: EDA || Topic Area: Design for Manufacturability

MODERATOR:
Andrew B. Kahng - *Univ. of California at San Diego, San Diego, CA*

ORGANIZER:
Andrew B. Kahng - *Univ. of California at San Diego, San Diego, CA*

At 20nm and below, manufacturing techniques have led to a regime of extreme rule-based IC design. Design for manufacturability has been replaced by "design-technology co-optimization": ground rules from foundries, libraries from IP providers, place-and-route tools from EDA vendors. But, while designers might now have freedom-from-choice, today's reality is one of long design cycles, with poor incremental value at leading-edge nodes.

Why is this happening? How much of the value proposition of a new technology is lost in making it accessible to designers? Who is responsible for losing this value?

PANELISTS:
Mahbub Rashed - *GLOBALFOUNDRIES, Cupertino, CA*
Kee Sup Kim - *Synopsys, Inc., Mountain View, CA*
Karim Arabi - *Qualcomm Technologies, Inc., San Diego, CA*
Julien Ryckaert - *IMEC, Leuven, Belgium*
Vivek Singh - *Intel Corp., Hillsboro, OR*

29 - HAPI: HETEROGENEITY, ACCELERATORS AND IP INTEGRATION

Time: 4:30 - 6:00pm || Room: 305 || Track: EDA || Topic Area: System-on-Chip Design

CHAIR:
Muhammad Shafique - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

CO-CHAIR:
Brett Meyer - *McGill Univ., Montreal, QC, Canada*

Heterogeneity paves the way for improving efficiency, making designers and users happy. However, this comes at the cost of increased design complexity. Efficient IP-integration mechanisms are key enablers to harness the power of heterogeneity. This session covers methods for designing, using and integrating accelerators in system-on-chip, from heterogeneous architectures to near-memory processing.

29.1 Nautilus: Fast Automated IP Design Space Search Using Guided Genetic Algorithms (4:30)
Michael K. Papamichael - *Carnegie Mellon Univ., Pittsburgh, PA*
Peter Milder - *Stony Brook Univ., Stony Brook, NY*
James C. Hoe - *Carnegie Mellon Univ., Pittsburgh, PA*

29.2 An Analysis of Accelerator Coupling in Heterogeneous Architectures (4:45)
Emilio G. Cota, Paolo Mantovani, Giuseppe Di Guglielmo, Luca P. Carloni - *Columbia Univ., New York, NY*

29.3 Execution-Driven Parallel Simulation of PGAS Applications on Heterogeneous Tiled Architectures (5:00)
Sascha Roloff, David Schafhauser, Frank Hannig, Jürgen Teich - *Univ. Erlangen-Nürnberg, Erlangen, Germany*

29.4 Acceleration of Control Flows on Reconfigurable Architecture with a Composite Method (5:15)
Junbin Wang, Leibo Liu, Jianfeng Zhu, Shouyi Yin, Shaojun Wei - *Tsinghua Univ., Beijing, China*

29.5 GRIP: Grammar-Based IP Integration and Packaging for Acceleration-Rich SoC Designs (5:30)
Munish Jassi, Daniel Mueller-Gritschneder, Ulf Schlichtmann - *Technische Univ. München, Germany*

29.6 ProPRAM: Exploiting the Transparent Logic Resources in Non-Volatile Memory for Near Data Processing (5:45)
Ying Wang, Yinhe Han, Lei Zhang, Hauwei Li, Xiaowei Li - *Chinese Academy of Sciences, Beijing, China*

Q & A Poster Session
6:00 - 7:00pm - Exhibit Floor

30 - VERIFICATION FROM TRANSACTIONS TO TRANSISTORS

Time: 4:30 - 6:00pm || Room: 310 || Track: EDA || Topic Area: Test and Verification

CHAIR:
Amitava Bhaduri - *Intel Corp., Sunnyvale, CA*

CO-CHAIR:
Avi Ziv - *IBM Research - Haifa, Israel*

This session presents innovations in both static and dynamic verification, covering the development lifecycle from initial high-level models to post-silicon and runtime checking.

We begin with a comprehensive review of changes in functional verification practices in the industry over the last few years, showing trends in the changing focus of verification activity. We then visit a range of functional verification challenges, spanning formal techniques, temporal monitors, arithmetic circuit correctness, and clock gating optimization. Finally, we conclude with the last stages of the verification process: post-silicon validation and debug.

30.1 Trends in Functional Verification: A 2014 Industry Study* (4:30)
Harry D. Foster - *Mentor Graphics Corp., Plano, TX*

30.2 Verifying SystemC using Stateful Symbolic Simulation (4:45)
Vladimir Herdt, Hoang Le, Rolf Drechsler - *Univ. of Bremen, Germany*

*** Indicates Best Paper Candidate**

30.3 In-Circuit Temporal Monitors for Runtime Verification of Reconfigurable Designs (5:00)
Tim Todman - *Imperial College London, United Kingdom*
Stephan Stilkerich - *Airbus, Ottobrunn, Germany*
Wayne Luk - *Imperial College London, United Kingdom*

30.4 Sequential Equivalence Checking of Clock-Gated Circuits (5:15) **Yu-Yun Dai** - *Univ. of California, Berkeley, CA*
Kei-Yong Khoo - *Cadence Design Systems, Inc., San Jose, CA*
Robert K. Brayton - *Univ. of California, Berkeley, CA*

30.5 Verification of Gate-Level Arithmetic Circuits by Function Extraction (5:30)
Maciej Ciesielski, **Cunxi Yu**, Walter E. Brown, Duo Liu - *Univ. of Massachusetts, Amherst, MA*
Andre Rossi - *Univ. de Bretagne SUD, Lorient, France*

30.6 Hybrid Quick Error Detection (H-QED): Accelerator Validation and Debug using High-Level Synthesis Principles (5:45)
Keith A. Campbell - *Univ. of Illinois at Urbana-Champaign, IL*
David Lin, Subhasish Mitra - *Stanford Univ., Stanford, CA*
Deming Chen - *Univ. of Illinois at Urbana-Champaign, IL*

Q & A Poster Session
6:00 - 7:00pm - Exhibit Floor

DESIGNER AND IP TRACK NETWORKING RECEPTION AND POSTER SESSION

Time: 4:30 - 6:00pm

NEW LOCATION! TODAY'S POSTER SESSION IS ON THE EXHIBIT FLOOR.

Sponsored by: Mentor Graphics, ChipEstimate.com

During the Poster Presentation, you will interact directly with poster presenters in a small group setting, during which DAC will be serving complimentary refreshments.

As the limited time available in the Designer and IP Track session program was exceeded by the quantity of great submitted content, we present the following posters in the Designer & IP Track Poster Session and Reception, held Tuesday, June 9 from 4:30 to 6:00pm on the Exhibit Floor.

31.1 Assertion Based FSM Verification Methodology Using Formal Techniques
Sandesh V. Borgaonkar, Mohammed Shariq, Deepanjan Roy - *NVIDIA Corporation, Bangalore, India*
Prosenjit Chatterjee - *NVIDIA Corporation, Santa Clara, CA*

31.2 Multicore CPU-Sub-System Design Automation
Patrick Labrousse - *STMicroelectronics & Atrenta Inc., Grenoble, France*
Francois Oswald - *ST-Ericsson, Grenoble, France*
Jerome Avezou - *Atrenta Inc., Grenoble, France*
Anshuman Nayak - *Atrenta Inc., Noida, India*
Kiran Vittal - *Atrenta Inc., San Jose, CA*

31.3 Early Power Grid Prototyping in 14nm Atom Cores
Manju Shamanna - *Intel Corp., Austin, TX*

31.4 Automatic Watching and Terminating Test Using UVM
Amish Shah, Shahriar Seyedhosseini - *Aquantia Corp., Milpitas, CA*

31.5 VIP Development Techniques – A View Into Controlling Features Effectively
Ranganath S. Kempanahally, Deepak Kumar E V, **Vikas Billa** - *elitePLUS Semiconductors Technologies Pvt Ltd, Bangalore, India*

31.7 Accurate RTL Power Estimation and Reduction with Clock Tree Mesh
Kinchit Desai, **Wayne Szeto** - *Intel Corp., Folsom, CA*

31.8 Design Methods for High Performance Graphics with Efficient Clock and Data Optimization
Raghavendra Raja Dwaraka, Madhu Vakil, Raj Varada - *Intel Corp., Santa Clara, CA*

31.9 A Case Study: Low-Power Methodology Achieves Power Requirements in a Camera SoC Without Losing Performance
Devendra V. Godbole, Ganesh Venkatakrishnan - *Open-Silicon, Inc., Pune, IN*
Venugopal V. P. - *Open-Silicon, Inc., Bangalore, India*

31.10 Automated RTL Power Estimation and Tracking for IP Blocks
Don Lee - *Broadcom Corp., San Diego, CA*
Yue Cao, Vikram R. Shamirpeta - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., San Jose, CA*
John Redmond - *Broadcom Corp., Escondido, CA*

31.11 Secure System Design with Tortuga Logic's Prospect
Jason Oberg, Jonathan Valamehr, Ryan Kastner, Timothy Sherwood - *Tortuga Logic, San Diego, CA*

31.12 Scan-IR Simulation for PDN Robustness Improvement and Yield Recovery
Sree Rajesh Saha - *Advanced Micro Devices, Inc., Bengaluru, India*
Erhan Ergin - *Advanced Micro Devices, Inc., Brooklyn, NY*
Nagesh Tamarapalli - *Advanced Micro Devices, Inc., Bengaluru, India*
Silqun Leung - *Advanced Micro Devices, Inc., Markham, ON, Canada*
Mahesh Sharma - *Advanced Micro Devices, Inc., Austin, TX*
Tony Todesco - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Lingaiah Karre - *Advanced Micro Devices, Inc., Bengaluru, India*
Piyush Jain, Nayan Chandak - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., Bengaluru, India*

31.13 Coverage Driven Functional CDC Verification Flow
Abhineet K. Bhojak, Snehlata Gutgutia - *Freescale Semiconductor, Inc., Noida, India*
Sudeep Mondal, Anshu Malani, Paras M. Jain - *Atrenta Inc., Noida, India*
Shaker Sarwary - *Atrenta Inc., San Jose, CA*
Amit Goldie - *Atrenta Inc., Noida, India*

31.14 Efficient FinFET Device Model Implementation for SPICE Simulation
Alexander Korobkov, Amit Agarwal, Subramanian Venkateswaran - *Oracle Corporation, Santa Clara, CA*

31.15 Utilizing PCIe Performance for Mobile Platforms
Shrinivasan Jaganathan, **Osman Javed** - *Cadence Design Systems, Inc., San Jose, CA*

31.16 Maximizing ROI Using Power Exploration
Shankar Kozhumam - *Marvell Semiconductor, Inc., Austin, TX*
Guillaume Boillet - *Atrenta Inc., San Jose, CA*

31.17 QOR Gains Ex Nihilo
Nikhil Murgai - *Freescale Semiconductor, Inc., Noida, India*
Anshuman Bansal - *Cadence Design Systems, Inc., Noida, India*

31.18 Analog Constraints Management and Validation
Manju Chinya - *Intel Corp., Folsom, CA*
Karthik Srikanta Murthy - *Intel Corp., Santa Clara, CA*

31.19 PERColating a Schematic-Based ERC Reliability Methodology for FPGAs
Ranjit Eswaran - *Xilinx, Inc., Hyderabad, India*
Haim Horovitz, Mark Roberts - *Xilinx, Inc., San Jose, CA*
Kiran YDV - *Xilinx, Inc., Hyderabad, India*
Dina Medhat - *Mentor Graphics Corp., Cairo, Egypt*
Lata Valluri - *Mentor Graphics Corp., Fremont, CA*

31.20 Verification Challenges with Power, Clock and Reset Domains
Ping Yeung - *Mentor Graphics Corp., Fremont, CA*
Alex Chen - *Advanced Micro Devices, Inc., Shanghai, China*

31.22 Hardware Random Transaction Generator for Validation
Mrugesh Walimbe, Kotavamsikrishna Darsi, Pankaj Prajapati, Virat Sharma - *Open-Silicon, Inc., Pune, India*

31.23 Pin Density Aware Legalization for Area Efficiency
Taeil Kim, Sungmin Bae - *Samsung Semiconductor, Inc., Gyeonggi-do, Republic of Korea*
Soonkeol Ryu - *Samsung Semiconductor, Inc., Yongin-City, Republic of Korea*
YongDurk Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Hyung-Ock Kim - *Samsung Semiconductor, Inc., Yong-in, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*
SungHo Park - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

31.25 Migrating Intel SoC Low Power Methodology to UPF (IEEE 1801)
Jimmy Cassis - *Intel Corp., Hillsboro, OR*

31.27 Plan & Execute a Verification Project Using Lean & Agile Methodology
Bodo E. Hoppe - *IBM Systems and Technology Group, Ingersheim, Germany*
Reinhard Ernst - *IBM Deutschland Research & Development GmbH, Boeblingen, Germany*

31.28 A Simple Interface for Adding Custom Peripherals to a Virtual Prototype
Robert Kaye, Christopher Lamb - *ARM Ltd., Cambridge, United Kingdom*

31.29 Standard Cell Manufacturability Analysis
Zexi Deng, Ralph Chen, **Lijuan Zou**, Xue Li, Sid Hone - *Semiconductor Manufacturing International, Shanghai, China*
Yifan Zhang - *Cain Communications, Inc., Shanghai, China*
Jason Sweis - *Cadence Design Systems, Inc. & IEEE CEDA, San Jose, CA*
Danlian Huang, Philippe Hurat, Ya-Chieh Lai, Hua Ding, Jason Huang - *Cadence Design Systems, Inc., San Jose, CA*

31.30 Multiple Power Plane Aware Full Chip Repeater Insertion and Accurate PV Analysis
Kousik Debnath - *Intel Corp., Bangalore, India*

31.31 Automated Power Mesh Evaluation and Optimization for Routing Resources
YongDurk Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Hyung-Ock Kim - *Samsung Semiconductor, Inc., Yong-in, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*
SungHo Park - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

31.32 A Flow to Accelerate Power Simulation with Gate-Level Timed Net-List
Daeseo Cha - *Samsung Electronics Co., Ltd., Youngin, Republic of Korea*
ByoungWoong Jeon - *Synopsys, Inc., SeongNam-si, Republic of Korea*
Anand Hebbalalu - *Synopsys, Inc., Mountain View, CA*
Matar Shih, Chia-Chih Yen - *Synopsys, Inc., Hsinchu, Taiwan*
Byeong Min - *Synopsys, Inc., SungNamSi, Republic of Korea*

31.33 HLS Soft-IP: The New Standard in Soft-IP Creation
Elad Litman - *Intel Corp., Petah-Tikva, Israel*
Tom Alsop - *Intel Corp., Hillsboro, OR*
Ashfaq Khan - *Intel Corp., Folsom, CA*
Bob Condon, Matthew J. Bone - *Intel Corp., Hillsboro, OR*

31.34 A New DSP-Based Satellite Transponder SoC for the Brazilian System of Data Collection
Marcelo Negreiros, David Cordova, Everton Reckziegel, Lucas A. Paris, Jerson P. Guex, Pedro Toledo, **Eric Fabris** - *NSCAD Microeletrônica, Porto Alegre, Brazil*

31.35 A New Stimulus Model For CPU Instruction Sets
Staffan Berg - *Mentor Graphics Corp., Kista, Sweden*
Mike Andrews - *Mentor Graphics Corp., Wilsonville, OR*

31.36 System Level Thermal Analysis Platform for Mobile SoC
Wook Kim, Joohee Choung, Kyungtae Do - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

31.37 New RTL Verification Signoff Metrics Using Assertion Synthesis Properties
Toshiyuki Uemura - *Renesas Electronics Corp., Itami, Japan*

31.38 Unified Flow for Test Coverage Improvement
Ankur Krishna, Virat Sharda, Shreya Singh - *Freescale Semiconductor, Inc., Noida, India*
Amit Goldie, Aditya Vij, Navneet Chaurasia, Anuj Kumar - *Atrenta Inc., Noida, India*
Al Joseph - *Atrenta Inc., San Jose, CA*

31.40 Accelerating Early Power Grid Design
Srinivas Chilukuri, Mamta Bansal - *Qualcomm Technologies, Inc., San Diego, CA*
Binu Abraham, Roshan Roy, Sankar Ramachandran, Nita Simon - *ANSYS, Inc., San Jose, CA*

31.41 Deep Submicron Multimillion Gates Implementation of Fiber- Optic Nonlinear Equalizers Using High Level Synthesis
Stenio M. Ranzini, Victor Parahyba, João B. Tardelli, Eduardo O. Schneider, Tomaz Vilela, **Eudes P. Lopes**, Jacklyn D. Reis, Juliano F. Oliveira - *CPqD Research and Development, Campinas, Brazil*

31.42 Framework for Automated Early Area and Power Estimation
Pramod S. Warrier - *Infineon Technologies AG, Bengaluru, India*
Juergen Karmann, **Moomen Chaari** - *Infineon Technologies AG, Neubiberg, Germany*

31.43 Reset Domain Crossing Verification
Ankush Sethi - *Freescale Semiconductor, Inc., Austin, TX*
Arjun Chowdhury, Neha Agarwal, Rohan Poudel - *Freescale Semiconductor, Inc., Noida, India*
Paras M. Jain, Amit Goldie - *Atrenta Inc., Noida, India*
Shaker Sarwary - *Atrenta Inc., San Jose, CA*
Deepak Verma - *Atrenta Inc., Noida, India*

31.44 Network Packet Header Generation Using Portable Stimulus
Jay O'Donnell - *Mentor Graphics Corp., Seahurst, WA*
Sridevi Navulur, Satheesh Parasumanna - *Xilinx, Inc., Hyderabad, India*
Rama Chaganti - *Mentor Graphics Corp., Hyderabad, India*
Amine Kandalaft - *Xilinx, Inc., Hazlet, NJ*

DESIGNER AND IP TRACK POSTER SESSION

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31.45 Electromigration Analysis – A Billion-Interconnect Problem!
Palkesh Jain - *Qualcomm India Pvt. Ltd., Bangalore, India*
Jai Pollayil, Vinayakam Subramaniam - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., Bangalore, India*
Aveek Sarkar - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., San Jose, CA*

31.46 Low Power Implementation on 14 nm Intel® Core™ M Processor
Jimmy Cassis - *Intel Corp., Hillsboro, OR*

31.47 Coherency Verification of Complex Multi-Processor SOCs with Reusable VIP
Sarath Chandran, Ajay Ganesh, Devendra Mulakkayala, Ravikrishnan Sree - *NVIDIA Corporation, Bangalore, India*
Smit Vora - *Synopsys, Inc., Bangalore, India*
Shawn Honess - *Synopsys, Inc., Mountain View, CA*

31.49 Designing Analog IP's for Automotive Applications
Ritesh Saraf, Claude Gauthier - *OmniPhy, San Jose, CA*

31.50 Breaking the Barriers of Languages by Unleashing the Power of Bind
Gaurav K. Verma, Doug Warmke - *Mentor Graphics Corp., Fremont, CA*

31.51 DDR4 Subsystem Implementation on 16FF+
Anurag Jain - *Cadence Design Systems, Inc., San Jose, CA*

31.52 Enable Efficiency in Clock Domain Crossing Using Flat and Hierarchical Approach
Pazhanimala Bijoy, Gaurav Goel, **Chalapathi Gandu** - *Intel Corp., Bangalore, India*

31.53 Ordered-List Coherency Verification for Pre-Silicon Simulation
Jon Hsieh, Dean Bair, Eugene Rotter - *IBM Corp., Poughkeepsie, NY*
Matthew Pardini - *IBM Corp., Natick, MA*

31.54 Statistical Single Timing Run Methodology for Signoff and Optimization
Eric Foreman - *IBM Systems and Technology Group, Essex Junction, VT*
Nathan Buck - *IBM Systems and Technology Group, Underhill, VT*
Michael Wood - *IBM Server and Technology Group, Poughkeepsie, NY*
Stephen Shuma - *IBM Systems and Technology Group, Essex Junction, VT*
Vladimir Zolotov - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Jeffrey G. Hemmett - *IBM Systems and Technology Group, Essex Junction, VT*

31.55 Electromigration FIT Rate Estimation
Shane Stelmach - *Texas Instruments, Inc., Allen, TX*
Gautam Kapila - *Texas Instruments, Inc., Dallas, TX*

31.56 Advancements in Test Circuits for Accurate Measurement of Setup/Hold and Delay Time of Standard Cell IPs
Joonsoo Park - *ARM Ltd., San Jose, CA*
Neha Agarwal, Anand Balan - *ARM Ltd., Bangalore, India*
Faisal Khoja - *ARM Ltd., San Jose, CA*
Ramesh Manohar, **Sagar Undale** - *ARM Ltd., Bangalore, India*
Rupal Gandhi - *ARM Ltd., San Jose, CA*

31.57 Code and Functional Coverage Closure Using Formal UNReachability Analysis
Puneet Anand - *Qualcomm Technologies, Inc., San Diego, CA*

31.58 Enhancing CDC Tools for High-Performance Designs
Iredamola Olopade - *Intel Corp., Portland, OR*

31.59 Accelerating Algorithmic Design with Application Specific Processors
Neil P. Hand - *Codasip, Ltd., San Jose, CA*
Thomas Daniel - *Exar Corporation, Fremont, CA*

31.60 Synthetic Trace Model in Wireless Communication System Design
YwhPyng Harn, Fa Yin - *Huawei Technologies Co., Ltd., Santa Clara, CA*
Xiaotao Chen - *Huawei Technologies Co., Ltd., Bridgewater, NJ*

31.61 Leveraging Automated Assertion Synthesis Increase Verification Efficiency in Real Time
Ravikiran Kaidala Lakshman - *Cisco Systems, Inc., San Jose, CA*
Yong Liu - *Atrenta Inc., San Jose, CA*

31.62 Developing a Physical Verification Solution for IC-Package Co-Design
Anup Keval, **Magesh Govindarajan** - *Qualcomm Technologies, Inc., San Diego, CA*
Ken Nguyen, Kai Liu - *STATS ChipPAC Ltd., Tempe, AZ*
John Ferguson - *Mentor Graphics Corp., Wilsonville, OR*
Tarek Ramadan - *Mentor Graphics Corp., Cairo, Egypt*

31.63 Acceleration Friendly Verification IP
Alicia Strang, Pei Suen - *Cadence Design Systems, Inc., Irvine, CA*

31.64 Digital IC Design Flow Aiming Electromigration Effects Minimization
Lucas A. de Paris - *NSCAD Microeletrônica, Porto Alegre, Brazil*
Gracieli Posser, Ricardo Reis - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*

31.65 IR Analysis for Multi-Die Devices
Kamran N. Khan, Subbarao Govardhanagiri, Ranganadh Mudumbai - *Xilinx, Inc., Hyderabad, India*

31.66 Memristor Crossbars for Parallel Big-Data Stochastic Computing
Alvaro Velasquez - *Univ. of Central Florida, West Palm Beach, FL*
Sumit Kumar Jha - *Univ. of Central Florida, Orlando, FL*

31.67 Assured Trust Through RTL-to-GDSII Formal Equivalence
Tom J. Mannos, Jason Michnovicz - *Sandia National Laboratories, Albuquerque, NM*

31.68 Physical IP for Embedded FPGA Core
Cheng C. Wang, Fang-Li Yuan - *Flex Logix Technologies, Inc., Mountain View, CA*

31.69 Architectural Trade-Off Analysis
Minyoung Mo, Jianfeng Liu, Kyungtae Do - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*
SungHo Park - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

31.70 Optimized ASIC Design Integrating 28Gbps SerDes
Naveen H N - *Open-Silicon, Inc., Bangalore, India*
Steven C. Eplett, Abu Eghan - *Open-Silicon, Inc., Milpitas, CA*

31.71 How to Use oaxPop to Find Optimal Via Placements
James D. Masters - *Intel Corp., Folsom, CA*

31.72 Evaluation by Protocol of the Subsystem IP Proportion for USB, PCIe, DMC, SATA, HDMI and MIPI
Eric H. Esteve - *IP-nest, Marseille, France*

31.73 System Level Emulation for SoCs
Prasad Bolisetty, **Pirzad J. Motafram** - *Soft Machines, Santa Clara, CA*

31.74 VLSI Wide Bus Synthesis
Duo Ding, Akshay Sharma, Huy Vo, Manesh Patel
- *Oracle Corporation, Austin, TX*

31.75 Developing Common UVM Testbench for Simulation and Emulation Platforms to Reduce Verification Effort Across Different Abstraction Levels
Ranganath S. Kempanahally, Deepak Kumar E V, **Vikas Billa** - *elitePLUS Semiconductors Technologies Pvt Ltd, Bangalore, India*

31.76 Intel SOC CTP Common Trace Port
Aviv Barkai, Tsvika Kurts - *Intel Corp., Haifa, Israel*
Amit Menachem - *Intel Corp., Yakum, Israel*

31.77 Hierarchical Static Low Power Verification
Bhaskar Pal, Akanksha Maurya, Rajarshi Mukherjee
- *Synopsys India Pvt. Ltd., Bangalore, India*
Kaushik De - *Synopsys, Inc., Mountain View, CA*

31.78 Unscrambling Memory Scrambling
Srisurya Konduri, **Radhika Gupta**, Atul Bhargava
- *STMicroelectronics, Greater Noida, India*
Lionel Maiaux - *STMicroelectronics, Crolles, France*

31.79 Estimation of Whole Pattern Types with Process Risk Through Pattern Profiling
Jae-Hyun Kang, Nam Jae Kim, Seung Weon Paek, In Hack Lee
- *Samsung Electronics Co., Ltd., Yongin-si, Republic of Korea*

31.80 Physical Hierarchy Creation for Complex High Performance Graphics IP
Radu Zlatanovici, Rishita Manne - *Intel Corp., Santa Clara, CA*
Ken Banas - *Intel Corp., Dunedin, New Zealand*
Raj Varada - *Intel Corp., Santa Clara, CA*

31.81 Scaling Formal Verification to Verify a Level3 Cache Unit
Fady Copty - *IBM Systems and Technology Group, Haifa, Israel*
Viresh Paruthi - *IBM Systems and Technology Group, Austin, TX*
Katia Patkin - *IBM Systems and Technology Group, Haifa, Israel*

31.82 Connectivity Model Approach for Connectivity Verification
Mrugesh Walimbe, Mitesh D. Thakkar - *Open-Silicon, Inc., Pune, India*

31.83 20nm Custom Digital Circuit Structured Layout Auto Route with IC Compiler
Chern Zhe Teh - *Altera Corp., Penang, Malaysia*

31.84 SystemC Builder: New Modelling Approach for Virtual Prototyping
Simranjit Singh, Anand Patil, Ankur Saini, MaheshKumar Simpy, Rajashekar Somashekar - *Infineon Technologies AG, Bengalooru, India*
Moomen Chaari - *Infineon Technologies AG, Neubiberg, Germany*

31.86 SynthOS - Push-Button Creation of an Optimized Application Specific OS
Bob Zeidman - *Zeidman Consulting, Cupertino, CA*
Jacob Harel - *Zeidman Technologies, Cupertino, CA*

31.87 RTL Power Estimation for High-Speed Serial I/Os with Complex Clocking and Multi-Library Architecture
Sirisha B. Venkata, Aditya Ramachandran, **Deepmala Sachan**, Thameem Syed D - *Intel Corp., Bangalore, India*

31.88 Software/Hardware Interface for Multi-Manycore - SHIM
Masaki Gondo - *eSOL Co.,Ltd., Nakano-ku, Japan*

31.89 Efficient Clock Domain Crossing (CDC) Verification Methodology for MP-Core Asynchronous Interfaces
Mejid Kebaili, Jean-Christophe Brignone - *STMicroelectronics, Grenoble, France*
Shaker Sarwary - *Atrenta Inc., San Jose, CA*
Paras M. Jain - *Atrenta Inc., Noida, India*

31.90 Modular Chip Level Verification of Non-Mainline Chip Processor Functions
Matteo Michel - *IBM Deutschland Research & Development GmbH, Chemnitz, Germany*
Johannes Koesters - *IBM Corp., Boeblingen, Germany*
Benedikt Geukes - *IBM Deutschland Research & Development GmbH, Boeblingen, Germany*

31.91 Creative Formal Techniques to Verify PCache
Normando M. Montecillo, Keyu Chang - *Broadcom Corp., Santa Clara, CA*
Ipshita Tripathi - *Oski Technology, Inc., Mountain View, CA*
HarGovind Singh - *Oski Technology, Inc., Gurgaon, India*
Vigyan Singhal - *Oski Technology, Inc., Mountain View, CA*

31.92 A Hybrid Approach to Standard Cell Power Characterization Based on PVT Independent Contributor Modeling for Use in Traditional Power Analysis Flows
Nagu Dhanwada - *IBM Corp., Hopewell Junction, NY*
Arun Joseph, Spandana Rachamalla - *IBM Systems and Technology Group, Bangalore, India*
William Dungan - *IBM Systems and Technology Group, Hopewell Junctiion, NY*
Arya Madhusoodanan - *IBM Systems and Technology Group, Bangalaore, India*
Suriya T. Skariah - *IBM Systems and Technology Group, Bangalore, India*
Karl Moody - *IBM Systems and Technology Group, Essex Junction, VT*
David Kadzov - *IBM Systems and Technology Group, Williston, VT*

31.93 Cadence DDR IP Power and Noise Optimization Techniques for High Speed Memory Subsystems
Amjad Qureshi, Devin Persaud, **Chung Huang** - *Cadence Design Systems, Inc., San Jose, CA*

WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 - 7:00pm

NEW LOCATION! TODAY'S POSTER SESSION IS ON THE EXHIBIT FLOOR.

85.1 Approximate Kernel Acceleration on FPGAs
Abbas Rahimi, Atieh Lotfi - *Univ. of California at San Diego, La Jolla, CA*
Divya Mahajan, Hadi Esmaeilzadeh - *Georgia Institute of Technology, Atlanta, GA*
Rajesh Gupta - *Univ. of California at San Diego, La Jolla, CA*

85.2 Stochastic Analysis of Replay-Based Resilient Architectures
Chenyue Meng - *Tsinghua Univ., Beijing, China*
Dylan Hand, Hsin-Ho Huang - *Univ. of Southern California, Los Angeles, CA*
Matheus T. Moreira - *Univ. of Southern California & Pontificia Univ. Católica do Rio Grande do Sul, Los Angeles, CA*
Peter Beerel - *Univ. of Southern California, Los Angeles, CA*

85.3 Union Page Cache for Embedded Systems with PCM-Based Storage Devices
Shuo-Han Chen, Tseng-Yi Chen - *National Tsing Hua Univ., Hsinchu, Taiwan*
Yuan-Hao Chang - *Academia Sinica, Taiper, Taiwan*
Hsin-Wen Wei - *Tamkang Univ., New Taipei City, Taiwan*
Wei-Kuan Shih - *National Tsing Hua Univ., Hsinchu, Taiwan*

85.4 Physical Co-Design for Micro-Fluidically cooled 3D ICs
Zhiyuan Yang - *Univ. of Maryland, Greenbelt, MD*
Ankur Srivastava - *Univ. of Maryland, College Park, MD*

85.5 PolyGP: Improving GP-Based Analog Optimization through Accurate High-Order Monomials and Semidefinite Relaxation
Ye Wang, Constantine Caramanis, Michael Orshansky - *Univ. of Texas at Austin, TX*

85.6 SiLego: A Micro-Architectural Level Regular Layout as the Basis for System Level Synthesis of Hardware
Nasim Farahini, Ahmed Hemani, Hassan Sohofi, Shuo Li- *KTH Royal Institute of Technology, Stockholm, Sweden*

85.7 System-HDL based Virtual Prototyping of RF Transceivers for Verification and IP-Reuse.
Stefan J. Heinen - *RWTH Aachen Univ., Aachen, Germany*
Zhimiao Chen - *Aachen Univ. of Technology, Aachen, Germany*
Ralf Wunderlich - *RWTH Aachen Univ., Aachen, Germany*

85.8 An Efficient Design of a Configurable ROPUF using Programmable XOR Gates
Fathi Amsaad, Muslim Mustapa, Mohammed Niamat - *Univ. of Toledo, OH*

85.9 Adaptive Sprinting for Systems with Phase Change Material
Fulya Kaplan, Ayse K. Coskun - *Boston Univ., Boston, MA*

85.10 A Mixed-Signal Simulation Methodology using HVL DV Environment for Verifying MIPI DPHY IP using Custom Interface-Elements/Connect-Modules
Somasunder K. Sreenath, **Vinayak Hegde**, Madhu Kiran, Ajay B S - *Cadence Design Systems, Inc., Bangalore, India*

85.11 Elevator-Based Key Management to Support Secure Deletion for Resource-Constrained Flash-Memory Storage Devices
Wei-Lin Wang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Yuan-Hao Chang - *Academia Sinica, Taiper, Taiwan*
Po-Chun Huang - *Yuan Ze Univ., Taipei, Taiwan*
Chia-Heng Tu - *Institute for Information Industry, Taipei, Taiwan*
Hsin-Wen Wei - *Tamkang Univ., New Taipei City, Taiwan*
Wei-Kuan Shih - *National Tsing Hua Univ., Hsinchu, Taiwan*

85.12 Wide I/O or LPDDR3? Exploring and Analysis of Performance, Power and Temperature of Emerging DRAM Technologies in Embedded MPSoCs
Mohammad Hossein Hajkazemi, Mohammad Khavari Tavana, Houman Homayoun - *George Mason Univ., Fairfax, VA*

85.14 Reducing WCET Using Function Splitting for Code Management on Software-Managed Multicores
Yooseong Kim - *Arizona State Univ., Tempe, AZ*
Aviral Shrivastava - *Arizona State Univ., Phoenix, AZ*
David Broman - *KTH Royal Institute of Technology, Kista, Sweden*
Vijetha Kumar, Prashant Ramachandra - *Toyota Technical Center, Ann Arbor, MI*

85.15 A Length Matching Routing Algorithm for Set-Pair Routing in Interposer Design
Yuta Nakatani - *Tokyo Institute of Technology, Tokyo, Japan*
Atsushi Takahashi - *Tokyo Institute of Technology, Meguro, Japan*

85.16 Area-Efficient Reconfigurable Processing Element for Crypto-Systems on Xilinx FPGA Platform
Mohamed El-Hadedy - *Univ. of Virginia, Chartlottesville, VA*
Kevin Skadron - *Univ. of Virginia, Charlottesville, VA*
Hristina Mihajloska - *Saints Cyril and Methodius Univ. of Skopje, Macedonia*
Danilo Gligoroski - *Norwegian Univ. of Science and Technology, Trondheim, Norway*

85.17 Sequential C-code to Distributed Pipelined Heterogeneous MPSoC Synthesis for Streaming Applications
Jude Angelo Ambrose, Jorgen Peddersen - *Univ. of New South Wales, Sydney, Australia*
Yusuke Yachide, Kapil Batra - *Canon Information Systems Research Australia Pty. Ltd., Sydney, Australia*
Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*

85.18 Contention-Free Multicore Real-Time Memory System by Splitting the Data Bus
Javier Jalle, Eduardo Quinones, Jaume Abella - *Barcelona Supercomputing Center, Barcelona, Spain*
Luca Fossati, Marco Zulianello - *European Space Agency, Noordwijk, The Netherlands*
Francisco J. Cazorla - *Barcelona Supercomputing Center, Barcelona, Spain*

85.19 Optimizing Delay Tests at the Memory Boundary
Kelly A. Ockunzzi, Michael R. Ouellette - *IBM Corp., Essex Junction, VT*
Kevin W. Gorman - *INVECAS, Inc., Williston, VT*

85.20 A Parallelizable Approach for Tracking Down Design Behaviours Through Dynamic Analysis of Execution Traces
Alessandro Danese, Luca Piccolboni - *Verona Univ., Verona, Italy*
Graziano Pravadelli, **Michele Lora** - *Univ. of Verona, Verona, Italy*

85.21 Post Placement Leakage Reduction with Stress-Enhanced Filler Cells
Jun-Ho Choy - *Mentor Graphics Corp., Fremont, CA*
Armen Kteyan, Henrik Hovsepyan - *Mentor Graphics Corp., Yerevan, Armenia*
Ramnath Venkatraman - *Avago Technologies, San Jose, CA*
Valeriy Sukharev - *Mentor Graphics Corp., Fremont, CA*
Ruggero Castagnetti - *Avago Technologies, San Jose, CA*

85.22 A Synthesis-Parameter Tuning System for Autonomous Design-Space Exploration
Matthew M. Ziegler - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Hung-Yi Liu - *Columbia Univ., New York, NY*
George D. Gristede - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Bruce Owens - *IBM Systems and Technology Group, Rochester, MN*
Ricardo Nigaglioni - *IBM Systems and Technology Group, Austin, TX*
Luca P. Carloni - *Columbia Univ., New York, NY*

85.23 Comprehensive Testbed for Integrated Secure and Reliable Vehicular Ad-Hoc Network Protocols
Kevin Lindenmayer - *Univ. of Mississippi, University, MS*
Matthew Morrison - *Univ. of Mississippi, Oxford, MS*

85.24 A Top-Down Design Methodology for Reconfigurable Quadrature Sigma-Delta Data Converters
Ye Zhang - *Aachen Univ. of Technology, Aachen, Germany*
Oner Haday, Ralf Wunderlich, Stefan J. Heinen - *RWTH Aachen Univ., Aachen, Germany*

85.25 Error Handling and Self Testing Mechanism for Automotive Safety
Ritesh Agrawal, Shreya Singh - *Freescale Semiconductor, Inc., Noida, India*
Dirk Wendel - *Freescale Semiconductor, Inc., Munich, Germany*

85.26 BoardPUF: Physical Unclonable Functions for Printed Circuit Board Authentication
Lingxiao Wei, Yannan Liu, Jie Zhang, Chaosheng Song, Feng Yuan, Qiang Xu - *Chinese Univ. of Hong Kong, Hong Kong*

85.27 Reliable PUF Design Using Machine Learning for CRP Enrollment
Xiaolin Xu, Wayne Burleson - *Univ. of Massachusetts, Amherst, MA*

85.28 Solving Constraints in FPGA Detailed Routing without Track to Channel Encoding
Mona Safar - *Ain Shams Univ., Cairo, Egypt*
Ashraf Salem - *Mentor Graphics Corp., Cairo, Egypt*

85.29 HyNoC: An All-Direction Millimetre-Wave Wireless and Wired Reconfigurable Communication Fabric Design for Network-on-Chip
He Zhou - *Univ. of Arizona, Tucson, AZ*
Sungjong Yoo - *Univ. of Arizona, Tempe, AZ*
Kathleen Melde, Janet M. Roveda - *Univ. of Arizona, Tucson, AZ*

85.30 Circuit and System Design Methodologies for Improved Reliability of MTJs in STTRAM Arrays
Anirudh S. Iyengar, Nitin Rathi, **Swaroop Ghosh** - *Univ. of South Florida, Tampa, FL*

85.31 Functional Coverage Planning and Automation for Highly Configurable IP
Jeremy Ridgeway - *Avago Technologies, Fort Collins, CO*
Karishma Dhruv - *Consultant, Milpitas, CA*
Kavitha Chaturvedula - *Avago Technologies, San Jose, CA*

85.32 RAPITIMATE: Rapid Performance Estimation of Pipelined Processing Systems Containing Shared Memory
Su Shwe - *Univ. of New South Wales, Sydney, Australia*
Kapil Batra, Yusuke Yachide - *Canon Information Systems Research Australia Pty. Ltd., Sydney, Australia*
Jorgen Peddersen, Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*

85.33 Reinforcement Learning-Based DPM-DVFS Trade-Off for Thermal-Aware Power Optimization of Embedded Systems
Anup K. Das, Mathew J. Walker, Geoff V. Merrett, Bashir M. Al-Hashimi - *Univ. of Southampton, Southampton, United Kingdom*

85.34 Trigger Graphs for Fast and Accurate NoC Endpoint Simulation
Eric Norige, Alex X. Liu - *Michigan State Univ., East Lansing, MI*
Sailesh Kumar - *NetSpeed Systems, San Jose, CA*

85.35 Novel SEU Analysis Strategy Based on MCMC Sampling
Meng Li, Ye Wang, Michael Orshansky - *Univ. of Texas at Austin, TX*

85.36 Process Variation Aware Timing Analysis Methodology based on a Monte Carlo Framework
Taizhi Liu, Woongrae Kim, Chang-Chih Chen, Linda Milor - *Georgia Institute of Technology, Atlanta, GA*

85.37 Nonvolatile Memory Allocation for High-level Synthesis with Loop Transformations
Shuangchen Li - *Univ. of California, Santa Barbara, CA*
Ang Li, Zhe Yuan - *Tsinghua Univ., Beijing, China*
Peng Li - *Univ. of California, Los Angeles, CA*
Guangyu Sun - *Peking Univ., Beijing, China*
Yongpan Liu, Huazhong Yang - *Tsinghua Univ., Beijing, China*
Yuan Xie - *Univ. of California, Santa Barbara, CA*

85.38 Computing Secrets on a Resistive Memory Array
Pierre-Emmanuel Gaillardon, **Luca Amaru** - *Swiss Federal Institute of Technology, Lausanne, Switzerland*
Anne Siemon, Eike Linn, Rainer Waser - *RWTH Aachen Univ., Aachen, Germany*
Anupam Chattopadhyay - *Nanyang Technological Univ., Singapore, Singapore*
Giovanni De Micheli - *Swiss Federal Institute of Technology, Lausanne, Switzerland*

85.39 Design and Benchmarking of Hybrid CMOS-Spin Wave Device Circuits Compared to 10nm CMOS
Odysseas Zografos, Bart Soree, Adrien Vaysset - *IMEC, Leuven, Belgium*
Stefan Cosemans - *IMEC, Heverlee, Belgium*
Luca Amaru, Pierre-Emmanuel Gaillardon - *Swiss Federal Institute of Technology, Lausanne, Switzerland*
Giovanni De Micheli - *Ecole Polytechnique Fédérale de Lausanne, Switzerland*
Safak Sayan - *IMEC, Leuven, Belgium*
Rudy Lauwereins, **Praveen Raghavan** - *IMEC, Heverlee, Belgium*
Iuliana Radu, Aaron Thean - *IMEC, Leuven, Belgium*

85.40 DDAANN: Data-Driven Logic Synthesizer for Acceleration of Forward Propagation in Artificial Neural Networks
William Smith, Mark Fishkin, Viktor Pracht, Timothy N. Miller - *SUNY Binghamton, NY*

85.41 Non-Sequential FEV Based Test Automation for Fault Grading
Raghavendra B. Adiga, **Isha Das** - *Intel Corp., Bangalore, India*

WORK-IN-PROGRESS POSTER SESSION

85.44 A 3-D Signature Compaction Method for SoC Buggy Cycle Identification
Tai-Feng Chen, Ing-Jer Huang - *National Sun Yat-sen Univ., Kaohsiung, Taiwan*

85.45 Accelerating Deep Learning Neural Networks with Heterogenous System Architectures
Ziyang Qi, Barbara Yuan - *Univ. of California, Santa Barbara, CA*

85.46 Electromigration-Aware Placement for 3D-ICs
Tiantao Lu - *Univ. of Maryland, Collge Park, MD*
Zhiyuan Yang - *Univ. of Maryland, Greenbelt, MD*
Ankur Srivastava - *Univ. of Maryland, College Park, MD*

85.47 DR-Scan: A Test Methodology for Dual-Rail Asynchronous Circuits
Shih-An Hsieh - *National Taiwan Univ., Taipei, Taiwan*
Yu-Sheng Lu, Ying-Hsu Wang, Kuan-Yen Huang, **James Chien-Mo Li** - *National Taiwan Univ., Taipei, Taiwan*

85.48 Optimal Multi-Tapeout Project Scheduling for Enterprise-Scale Design Management and Cost Reduction
Prabhav Agrawal - *Univ. of California at San Diego, La Jolla, CA*
Biswadeep Chatterjee - *Qualcomm India Pvt. Ltd., Bangalore, India*
Andrew B. Kahng, Pranay K. Myana, **Siddhartha Nath** - *Univ. of California at San Diego, La Jolla, CA*

85.50 On the Design of an Energy-Efficient Digital Accelerator for Large Scale Multilayer Perceptron with On-Chip Training Utilizing Energy-Quality Trade-off
Duckhwan Kim, **Jaeha Kung**, Saibal Mukhopadhyay - *Georgia Institute of Technology, Atlanta, GA*

85.51 A Multi-Objective Framework for Co-Optimization of Buffer and Wire Sizes in High Performance Clock Trees
Amin Farshidi, Logan M. Rakai, Laleh Behjat, David Westwick - *Univ. of Calgary, AB, Canada*

85.52 Reliable and Anti-Cloning PUFs Based on Configurable Ring Oscillators
Mingze Gao, Khai Lai, Jiliang Zhang, **Gang Qu** - *Univ. of Maryland, College Park, MD*

85.53 An Analytic Approach on End-to-End Packet Error Rate Estimation for Network-on-Chip
Michael Vonbun, Stefan Wallentowitz, Andreas Oeldemann, Andreas Herkersdorf - *Technische Univ. München, Germany*

85.54 Secure Gate Sizing
Chongxi Bao, Ankur Srivastava - *Univ. of Maryland, College Park, MD*

85.55 Write Back Energy and Throughput Optimizations for STT-RAM Based Cache using Data Pattern Characterization
Xiaolong Zhang, Yuanqing Cheng - *Beihang Univ., Beijing, China*
Ying Wang - *Chinese Academy of Sciences, Beijing, China*
Weisheng Zhao - *Beihang Univ., Beijing, China*
Aida Todri-Sanial - *Centre National de la Recherche Scientifique, Montpellier, France*

85.57 Full-Chip Electromigration Assessment for Power Grid Networks: Effect of Cross-Layout Temperature and Thermal Stress Distributions
Xin Huang - *Univ. of California, Riverside, CA*
Valeriy Sukharev, Jun-Ho Choy, Marko Chew, Ara Aslyan - *Mentor Graphics Corp., Fremont, CA*
Patrick Gibson - *Mentor Graphics Corp., Wilsonville, OR*
Sheldon X.-D. Tan, **Hengyang Zhao** - *Univ. of California, Riverside, CA*

85.58 Parana: Fast Parallel Application and Multiprocessor Design Space Exploration from Sequential Code
Vítor Schwambach, Sébastien Cleyet-Merle, Alain Issard - *STMicroelectronics, Grenoble, France*
Stéphane Mancini - *TIMA Lab, CNRS/Grenoble INP/UJF, Grenoble, France*

85.59 Threshold Logic Synthesis Based on Cut Pruning
Augusto Neutzling, Jody Maick Matos - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*
Alan Mishchenko - *Univ. of California, Berkeley, CA*
Renato P. Ribas, Andre I. Reis - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*

85.60 FASTrust: Feature Analysis for Third-Party IP Trust Verification
Song Yao - *Tsinghua Univ., Beijing, China*
Xiaoming Chen - *Carnegie Mellon Univ., Pittsburgh, PA*
Jie Zhang - *Chinese Univ. of Hong Kong, Hong Kong*
Jia Wang - *Illinois Institute of Technology, Chicago, IL*
Qiang Xu - *Chinese Univ. of Hong Kong, Hong Kong*
Yu Wang, Huazhong Yang - *Tsinghua Univ., Beijing, China*

85.61 Process, Design Rule and Layout Co-Optimization for sub-10nm FinFet Devices using Directed Self-Assembly
Joydeep Mitra - *Mentor Graphics Corp., Austin, TX*
Andres Torres - *Mentor Graphics Corp., Wilsonville, OR*
David Z. Pan - *Univ. of Texas at Austin, TX*

85.62 Progressive Legalization During Global Placement
Nima Karimpour Darav, Laleh Behjat - *Univ. of Calgary, AB, Canada*
Andrew Kennings - *Univ. of Waterloo, ON, Canada*
David Westwick - *Univ. of Calgary, AB, Canada*

85.63 HALTimer: A Fast Vt Replacement Heuristic for Leakage Power Minimization using Adaptive Lazy Timer
Patanjali S. L. P. S. K., Seetal Potluri, Kamakoti Veezhinathan - *Indian Institute of Technology Madras, Chennai, India*

85.64 Design and Analysis of Pulsed-Index Protocols for Single-Channel, Low-Power, Dynamic Signaling
Shahzad Muzaffar - *Masdar Institute of Science and Technology, Abu-Dhabi, United Arab Emirates*
Ibrahim (Abe) Elfadel - *Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates*

85.66 STT-MRAM Cell Design with Partial Source Line Planes: Improving the Trade-Off Between Area and Series Resistance
Raf Appeltans - *Katholieke Univ. Leuven, Belgium*
Stefan Cosemans, Praveen Raghavan, Diederik Verkest, Liesbet Van der Perre - *IMEC, Heverlee, Belgium*
Wim Dehaene - *Katholieke Univ. Leuven, Belgium*

85.67 Design and Evaluation of a Low-Latency AVB Ethernet Endpoint based on ARM SoC
Christian Herber, Ammar Saeed, Andreas Herkersdorf - *Technische Univ. München, Germany*

85.68 A New Pattern Classification Framework Based on Nonlinear Dimensionality Reduction and Nonparametric Bayes Model
Tetsuaki Matsunawa - *Toshiba Corp., Saiwai-Ku, Kawasaki-Shi, Japan*
Bei Yu, David Z. Pan - *Univ. of Texas at Austin, TX*

85.69 ReCycling of Elastic Systems without Throughput Penalty
Rafael Trapani Possignolo, Elnaz Ebrahimi, Jose Renau - *Univ. of California, Santa Cruz, CA*

85.70 Hardware-Trojan Ranking at Gate-Level Netlists based on Trojan Net Features
Masaru Oya, Youhua Shi, Masao Yanagisawa, Nozomu Togawa - *Waseda Univ., Tokyo, Japan*

KEYNOTE PRESENTATION

CYBER THREATS TO CONNECTED CARS: STAYING SAFE REQUIRES MORE THAN FOLLOWING THE RULES OF THE ROAD

9:00 - 10:00am || Room: Gateway Ballroom || Track: Security || Topic Area: Security

Summary: Cars increasingly are networked computing platforms and with this burgeoning connectivity comes more vulnerability to possible cyber-attacks. We expect our vehicles to continue to evolve and support internet capabilities via WiFi and cellular data networks, connect to our mobile computing platforms via Bluetooth, provide GPS navigation assistance, and automatically link to the manufacturer to help with diagnostics. However, all those connectivity features create entry point for hackers. Can we make our cars more secure? Or should we accept the fact that they are as vulnerable as our computers at home? Come hear from the real experts on stage. John McElroy, Producer of Autoline Detroit will guide you through an in-depth chat between Jeffrey Massimilla, Chief of Cybersecurity at GM, and Craig Smith, author of the Car Hacker Manual.

Jeffrey Massimilla

Chief Product Cybersecurity Officer, Vehicle and Vehicle Services Cybersecurity- General Motors Company, Warren, MI

Biography: Jeffrey Massimilla was named chief product cybersecurity officer, Vehicle and Vehicle Services Cybersecurity for General Motors Company effective September 2nd, 2014. This role, was expanded from Massimilla's most recent position as director, vehicle cybersecurity. Massimilla is responsible for leading the team that is developing and implementing protocols and strategies to reduce the risks associated with cybersecurity threats related to the vehicle and vehicle connected services. Prior to this role, he served as the engineering manager, Next-Generation Infotainment Systems and Integrations. During his time in this role, Massimilla led the development and launch of a fully new vehicle infotainment system. Joining GM in 2001, as a design release engineer, Massimilla held multiple roles both in electrical and vehicle product program engineering creating solutions for various in-vehicle components. Jeff holds a Bachelor's Degree in Electrical Engineering from the University of Michigan and Master's degrees in Industrial and Manufacturing Engineering and Business Administration from the University of Michigan.

Craig Smith - *Founder, Theia Labs / OpenGarages.org / IATC, Seattle, WA*

Biography: Craig Smith is the founder of OpenGarages.org, a community driven vehicle research and exploration group. Craig also runs a security consulting firm, Theia Labs, which specializes in reverse engineering and automotive security. Craig has participated as a mentor for several automotive hack-a-thons with Battelle, US Cyber Camp and H3. He also published the 2014 Car Hacker's Manual which is available for free under the Creative Commons license. Craig has produced several open source tools and utilities to accelerate learning and research. Some of these tools include a web based group CAN bus sniffing tool, a tool to fingerprint active BUS network to determine make and model of a vehicle passively without causing network traffic, as well as some penetration testing tools targeted to vehicle communications.Craig Smith currently works closely with automotive manufactures, after market specialists, government organizations and public awareness groups like I am the Calvary (IATC). Craig focuses on collaboration efforts between independent researchers and industry groups entering the array of internet connected equipment. He recently moved to Seattle and started an Open Garage there at Crash Industries.

MODERATOR:

John McElroy - *President, Blue Sky Productions, Inc., Farmington Hills, MI*

Biography: John McElroy is the host of "Autoline Daily" the first industry webcast of industry news and analysis. He is also the host of the television program "Autoline This Week," an Emmy Award-winning, weekly half-hour discussion program featuring top automotive executives and journalists. McElroy also hosts "Autoline After Hours," the first regularly scheduled live webcast about the industry. The shows can be seen online at www.autoline.tv McElroy also broadcasts daily segments on WWJ Newsradio 950, the CBS affiliate in Detroit. He writes a monthly op-ed article for Ward's Auto World.

32 - SPECIAL SESSION: THE 4TH INDUSTRIAL REVOLUTION: SECURITY AND PRIVACY CHALLENGES IN INDUSTRIAL INTERNET OF THINGS

Time: 10:30am - 12:00pm || Room: 300 || Track: Security || Topic Area: Security

CHAIR:
Farinaz Koushanfar - *Rice Univ., Houston, TX*

ORGANIZER:
Ahmad-Reza Sadeghi - *Technische University Darmstadt, Germany*

Current Industrial trends aim at "connecting the unconnected": from the "Internet of Things" (IoT) to "Industrial Internet". Analysts predict billions of connected cyberphysical systems, enabling new services and experiences. These trends will improve customer value through increased individualization and more efficient production by taking advantage of machine-to-machine communication and integrating production and business IT. On the flipside, these systems will be appealing targets of attacks.

Attacks on IoT systems are crucial since they can have disastrous consequences in the physical world. Due to safety criticality and the vital role of emerging and envisioned personal, business, government and economic IoT systems, leaving security as an afterthought is perilous. The complexity of these systems and the scope of attacks raise new challenges and require networking, security and privacy as well as embedded systems communities to seek for practical solutions, in particular for identity management, knowledge protection and design and test methodologies.

32.1 Security and Privacy Challenges in Industrial Internet of Things (10:30)
Michael Waidner - *Fraunhofer Institute for Security Technologies, Darmstadt, Germany*
Ahmad-Reza Sadeghi - *Technische University Darmstadt, Germany*
Christian Wachsmann - *Intel Collaborative Research Institute for Secure Computing, Darmstadt, Germany*

32.2 IoT Security and Challenges (11:00)
Annabel Nickles - *Intel Corp., Hillsboro, OR*

32.3 Blocking Unsafe Behaviors in Control Systems through Static and Dynamic Policy Enforcement (11:30)
Stephen McLaughlin - *Samsung Research America, Sunnyvale, CA*

33 - SPECIAL SESSION: THE DIFFERENT FACETS OF AUTOMOTIVE EMBEDDED SOFTWARE

Time: 10:30am - 12:00pm || Room: 303 || Track: Automotive || Topic Area: Automotive Systems

CHAIR:
Samarjit Chakraborty - *Technische Univ. München, Germany*

Modern cars have several millions of lines of software code that run on a highly distributed architecture consisting of as many as 100 Electronic Control Units (ECUs) connected by a heterogeneous communication subsystem consisting of CAN, FlexRay and Ethernet among others. Both the design and the analysis of such software involves a number of challenges and calls for great engineering innovation. This session will discuss various aspects of automotive software, such as model-based design, component integration and timing analysis.

33.1 Timing-Aware Control Software Design for Automotive Systems (10:30)
Dirk Ziegenbein, Arne Hamann - *Robert Bosch GmbH, Renningen, Germany*

33.2 Compositional Modeling and Analysis of Automotive Feature Product Lines (11:00)
Sankara Narayanan Krishna - *Indian Institute of Technology, Bombay, India*
Ganesh Narwane - *Huawei Technologies Co., Ltd., Mumbai, India*
Sethu Ramesh - *General Motors Company, Warren, MI*
Ashutosh Trivedi - *Indian Institute of Technology, Bombay, India*

33.3 The Challenge of Interoperability: Model-Based Integration for Automotive Control Software (11:30)
Huafeng Yu - *Toyota InfoTechnology Center, Mountain View, CA*
Prachi Joshi - *Virginia Polytechnic Institute and State Univ., Arlington, VA*
Jean-Pierre Talpin - *INRIA, Rennes, France*
Sandeep Shukla - *Virginia Polytechnic Institute and State Univ., Arlington, VA*
Shinichi Shiraishi - *Toyota InfoTechnology Center, Mountain View, CA*

34 - SPECIAL SESSION: EMERGING PROBABILISTIC CIRCUITS FROM STOCHASTIC TO QUANTUM: WILL THEY SCALE?

Time: 10:30am - 12:00pm || Room: 304 || Track: EDA || Topic Area: Emerging Technologies

CHAIR:
Rolf Drechsler - *Univ. of Bremen, Germany*

ORGANIZER:
Ilia Polian - *Univ. of Passau, Germany*

After the recent collapse of Dennard scaling, the focus of the design community is progressively shifting towards emerging computing paradigms. In contrast to the architectures of the past, which were mostly deterministic, many of the new approaches are of probabilistic nature. This special session will focus on two different representatives from the domain of probabilistic computing: stochastic circuits and error-corrected topological quantum architectures and specifically investigate their scalability. The rationale for selecting these two paradigms is provided by a number of breakthroughs which have been recently achieved in both fields.

The three presentations will be given by experts on stochastic and topological quantum computing, providing Physics and Computer Engineering perspective on the issues. Covering two approaches to probabilistic computing within the Special Session will help the attendees to identify properties that are specific for a particular technology as opposed to generic features common for emerging probabilistic architectures.

34.1 Introduction to Stochastic Computing and its Challenges (10:30) **John Hayes** - *Univ. of Michigan, Ann Arbor, MI*

34.2 An Introduction into Fault-Tolerant Quantum Computing (11:00) **Simon Devitt** - *National Institute of Informatics, Tokyo, Japan*
Alexandru Paler - *Univ. of Passau, Germany*

34.3 Design Automation Challenges for Scalable Quantum Architectures (11:30)
Ilia Polian - *Univ. of Passau, Germany*
Austin G. Fowler - *Google, Inc. & Univ. of California, Santa Barbara, CA*

35 - COOL PLATFORMS AND APPLICATIONS

Time: 10:30am - 12:00pm || Room: 305
Track: EDA || Topic Area: Embedded System Architecture and Design

CHAIR:
Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
CO-CHAIR:
Chia-Lin Yang - *National Taiwan Univ., Taipei, Taiwan*

Improving energy efficiency requires consideration of various system layer aspects from applications to devices. This session first introduces platforms for mobile computing and near threshold computing. Then, domain specific energy efficient designs including low-power digital signal processing, organic light emitting diode display, and machine learning are presented. These architectures and algorithms are expected to contribute for future cooler IT systems.

35.1 A Control-Theoretic Approach for Energy Efficient CPU-GPU Subsystem in Mobile Platforms* (10:30)
David Kadjo - *Texas A&M Univ., College Station, TX*
Raid Ayoub, Michael Kishinevsky - *Intel Corp., Hillsboro, OR*
Paul Gratz - *Texas A&M Univ., College Station, TX*

35.2 Opportunistic Turbo Execution in NTC: Exploiting the Paradigm Shift in Performance Bottlenecks (10:45)
Hu Chen, Dieudonne Manzi Mugisha, Sanghamitra Roy, Koushik Chakraborty - *Utah State Univ., Logan, UT*

35.3 Domain Wall Memory Based Digital Signal Processors for Area and Energy-Efficiency (11:00)
Jinil Chung - *Korea Univ., Seoul, Republic of Korea*
Kenneth Ramclam - *Univ. of South Florida, Tampa, FL*
Jongsun Park - *Korea Univ., Seoul, Republic of Korea*
Swaroop Ghosh - *Univ. of South Florida, Tampa, FL*

35.4 DaTuM: Dynamic Tone Mapping Technique for OLED Display Power Saving Based on Video Classification (11:15)
Xiang Chen - *Univ. of Pittsburgh, PA*
Chun Jason Xue - *City Univ. of Hong Kong, Hong Kong*
Yiran Chen - *Univ. of Pittsburgh, PA*

35.5 Reno: A Highly-Efficient Reconfigurable Neuromorphic Computing Accelerator Design (11:30)
Xiaoxiao Liu, Mengjie Mao, Beiye Liu - *Univ. of Pittsburgh, PA*
Boxun Li - *Tsinghua Univ., Beijing, China*
Hao Jiang - *San Francisco State Univ., San Francisco, CA*
Yu Wang - *Tsinghua Univ., Beijing, China*
Mark Barnell, Qing Wu - *Air Force Research Lab, Rome, NY*
J. Joshua Yang - *Univ. of Massachusetts, Amherst, MA*
Hai Li, Yiran Chen - *Univ. of Pittsburgh, PA*

35.6 Scalable Effort Classifiers for Energy Efficient Machine Learning (11:45)
Swagath Venkataramani - *Purdue Univ., West Lafayette, IN*
Jie Liu - *Microsoft Research, Redmond, WA*
Anand Raghunathan - *Purdue Univ., West Lafayette, IN*
Mohammed Shoaib - *Microsoft Research, Redmond, WA*

*** Indicates Best Paper Candidate**

Q & A Poster Session
12:00 - 12:30pm - Esplanade Foyer

36 - THE GREAT DFM MELTING POT

Time: 10:30am - 12:00pm || Room: 310 || Track: EDA || Topic Area: Design for Manufacturability

CHAIR:
Rasit Topaloglu - *IBM Corp., Poughkeepsie, NY*
CO-CHAIR:
Shiyan Hu - *Michigan Technological Univ., Houghton, MI*

DFM is a multidisciplinary effort because litho-centric approaches alone cannot achieve the necessary scaling requirements. Design and process co-optimization is only possible when all facets in the electronic design flow are concurrently executed. This session explores several of these areas, including advances in design exploration, routing, mask synthesis and manufacturing. The session melts together the various DFM technologies required to enable more robust and cost effective electronic designs.

36.1 Evaluation of BEOL Design Rule Impacts Using An Optimal ILP-Based Detailed Router (10:30)
Kwangsoo Han, Andrew B. Kahng, **Hyein Lee** - *Univ. of California at San Diego, La Jolla, CA*

36.2 Detailed Routing for Spacer-Is-Metal Type Self-Aligned Double/Quadruple Patterning Lithography (10:45)
Yixiao Ding, Chris Chu - *Iowa State Univ., Ames, IA*
Wai-Kei Mak - *National Tsing Hua Univ., Hsinchu, Taiwan*

36.3 Mask Assignment and Synthesis of DSA-MP Hybrid Lithography for sub-7nm Contacts/Vias (11:00)
Yasmine A. Badr - *Univ. of California, Los Angeles, CA*
Andres Torres - *Mentor Graphics Corp., Wilsonville, OR*
Puneet Gupta - *Univ. of California, Los Angeles, CA*

36.4 High Performance Dummy Fill Insertion with Coupling and Uniformity Constraints (11:15)
Yibo Lin, Bei Yu, David Z. Pan - *Univ. of Texas at Austin, TX*

36.5 An Efficient Shift Invariant Rasterization Algorithm for All-Angle Mask Patterns in ILT (11:30)
Yixiao Ding, Chris Chu - *Iowa State Univ., Ames, IA*
Xin Zhou - *Synopsys, Inc., Mountain View, CA*

36.6 Effective Model-Based Mask Fracturing for Mask Cost Reduction (11:45)
Abde Ali Kagalwalla, Puneet Gupta - *Univ. of California, Los Angeles, CA*

Q & A Poster Session
12:00 - 12:30pm - Esplanade Foyer

37 - DESIGNER TRACK: SECURITY AND ANALYTICS FOR IOT

Sponsored by: Mentor Graphics

Time: 10:30am - 12:00pm || Room: 101
Track: Embedded Systems || Topic Area: General Interest

CHAIR:
Jan Rellermeyer - *IBM Research, Austin, TX*

While IoT gains momentum with each passing day, security and ability to convert massive volumes of data into business insights remain critical challenges. Leaders covering a broad swath of IoT technologies will present their visions and review emerging solutions to meet these challenges. The session will open with a look at IoT from software development perspective. Next, we'll hear how to leverage SDN and NFV technologies to marry IoT networks with cyber security solutions. The session will conclude with a look at technology to turn data into business insights.

37.1 Securing and Moving Data in IoT (10:30)
Sven Brehmer - *PolyCore Software, Inc., Burlingame, CA*

37.2 Achieving Visibility and Security in IoT Networks Using SDN and NFV Technologies (11:00)
Srini Addepalli - *Freescale Semiconductor, Inc., San Jose, CA*

37.3 Delivering Secure, Real-Time Business Insights for the Industrial World with MQTT (11:30)
Arnaud Mathieu - *IBM Corp., Austin, TX*

38 - DESIGNER TRACK: SIGNOFF LIKE CLOCK WORK: CLOCK IN, SIGN OUT!

Sponsored by: Mentor Graphics

Time: 10:30am - 12:00pm || Room: 105
Track: Silicon Design || Topic Area: Designer and IP Track

CHAIR:
Gilda Garreton - *Oracle Corporation, Redwood Shores, CA*

Worried about clock tree structures, skews and signoff issues? As a physical designer, you must deliver performance like nobody else, only if you know some the latest techniques and methodologies in clock layout and final signoff. This session prepares you for sound sleep by dealing with all those noisy topics that could keep you awake at night for your next design.

38.1 A Proactive Approach to Early Detection and Solution to Timing Issues In Slow Stuck-At Fault (SSAF) STA (10:30)
Apurva Chaure, **Rangarajan Ramanujam**, **Rakesh Gulati**, Shreyans Rungta, Swapnil Bahl - *STMicroelectronics, Greater Noida, India*

38.2 Next Generation Hybrid Clock Tree* (10:45)
Nikhil Murgai, Sumit Vyas - *Freescale Semiconductor, Inc., Noida, India*
Anshuman Bansal - *Cadence Design Systems, Inc., Noida, India*

38.3 Reliable Design with Skewed Clocks (11:00)
Anthony M. Hill - *Texas Instruments, Inc., Dallas, TX*
Frank Cano - *Texas Instruments, Inc., Houston, TX*
Krishna Panda, Arjun Rajagopal - *Texas Instruments, Inc., Dallas, TX*

38.4 Accelerating Productivity Using Design Automation for Low Skew Global Clock Distribution in a Complex SoC* (11:15) **Shraddha Padiyar**, Animesh Jain, Shanamaz Ganuga - *Advanced Micro Devices, Inc., Bangalore, India*

38.5 ESD CAD Tools Integration for SoC and IP Sign-Off Flow (11:30) **Che Choi C. Leung** - *Avago Technologies, Allentown, PA*
Chip Brewster - *Avago Technologies, Fort Collins, CO*

38.6 Smart and Efficient Multi-Scenario SoC Timing Closure and ECO Generator (11:45)
Aditi Sharma, Mohita Batra, Apurva Chaure, Rakesh Gulati, Rangarajan Ramanujam - *STMicroelectronics, Greater Noida, India*
Vaibhav Singh - *STMicroelectronics, Santa Clara, CA*

*** Indicates Best Paper Candidate**

Q & A Poster Session
6:00 - 7:00pm - Esplanade Foyer

SKY TALK: BUILDING INFINITE SERVICE OPPORTUNITIES WITH IOT

Time: 1:00 - 1:30pm || Room: Booth 311
Track: Embedded Systems || Topic Area: Business

CHAIR:
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

The IoT revolution will transform many markets from a 'sale of goods' to a 'sale of goods and services' economy. Embedded vendors have an opportunity to leverage IoT capabilities to stay relevant and grow. Intelligent and connected platforms will emerge, enabling new platform- or associated ecosystem- based value chains. Many will attempt to capitalize on the vast IoT opportunity – some will be traditional embedded designers, others experts in application development and software design with imaginative ideas they need to get to market quickly. We will discuss how forward-thinking semiconductor vendors can serve customers through system solutions that let them focus on efficiently designing unique IoT applications.

SPEAKER:
Ali Sebt - *Renesas Electronics America, Santa Clara, CA*

39 - ARMS AND ARMOR FOR THE FUTURE

Time: 1:30 - 3:00pm || Room: 300 || Track: Security || Topic Area: Security

CHAIR:
Jeffrey Draper - *Univ. of Southern California, Marina del Rey, CA*
CO-CHAIR:
Domenic Forte - *Univ. of Connecticut, Storrs, CT*

While people have widely accepted that today's security technologies are not sufficient to protect the nation's interests and our daily lives, this session looks into tomorrow's technology for a panacea. Security-enhanced processors mitigating software vulnerabilities, novel architecture for information flow tracking, post-CMOS devices based root of trust and emerging attack vectors, innovative characterization and emulation methods empowering PUFs, and hardware verification methods for Trojan detection, you name it - we have it.

39.1 HAFIX: Hardware-Assisted Flow Integrity Extension* (1:30)
Orlando Arias - *Univ. of Central Florida, Orlando, FL*
Lucas V. Davi, Matthias Hanreich - *Technische Univ. Darmstadt, Germany*
Yier Jin - *Univ. of Central Florida, Orlando, FL*
Patrick Koeberl - *Intel Corp., Darmstadt, Germany*
Debayan Paul, Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Dean Sullivan - *Univ. of Central Florida, Orlando, FL*

39.2 Performance Analysis of a Memristive Crossbar PUF Design (1:45)
Garrett S. Rose, Chauncey A. Meade - *Univ. of Tennessee, Knoxville, TN*

39.3 Adaptive Characterization and Emulation of Delay-based Physical Unclonable Functions Using Statistical Models (2:00)
Teng Xu - *Univ. of California, Los Angeles, CA*
Dongfang Li - *Huazhong Univ. of Science & Technology, Wuhan, China*
Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

39.4 Self-Correcting STTRAM under Magnetic Field Attacks (2:15)
Jae-Won Jang - *Univ. of South Florida, Tampa, FL*
Jongsun Park - *Korea Univ., Seoul, Republic of Korea*
Swaroop Ghosh - *Univ. of South Florida, Tampa, FL*
Swarup Bhunia - *Case Western Reserve Univ., Cleveland, OH*

39.5 On Using Control Signals for Word-Level Identification in A Gate-Level Netlist (2:30)
Edward L. Tashjian, Azadeh Davoodi - *Univ. of Wisconsin, Madison, WI*

39.6 Efficient Dynamic Information Flow Tracking on a Processor with Core Debug Interface. (2:45)
Jinyong Lee, **Ingoo Heo**, Yongje Lee, Yunheung Paek - *Seoul National Univ., Seoul, Republic of Korea*

*** Indicates Best Paper Candidate**

Q & A Poster Session
3:00 - 3:30pm - Esplanade Foyer

40 - PANEL: ARE YOU READY FOR THE RIGORS OF AUTOMOTIVE RELIABILITY?

Time: 1:30 - 3:00pm || Room: 303 || Track: Automotive || Topic Area: Automotive Systems

MODERATOR:
Matthew Hogan - *Mentor Graphics Corp., Wilsonville, OR*
ORGANIZER:
Gene Forte - *Mentor Graphics Corp., Wilsonville, OR*

The electronics design community is looking to the automotive market with new eyes as the digital content of modern vehicles is skyrocketing. While everyone would like a piece of the pie, are potential new market entrants really prepared for the rigors of automotive electronics reliability? Is it possible to adapt existing designs to meet the reliability requirements of automotive systems? What about in-vehicle infotainment systems: from a reliability standpoint, are they just like consumer products, or do they have their own special requirements? What technical, process and cultural changes are needed to be successful in transportation industries?

PANELISTS:
Ertugrul Demircan - *Freescale Semiconductor, Inc., Eugene, OR*
Ofer Tamir - *TowerJazz, Netanya, IL*
Ron Miller - *Delphi Automotive, Kokomo, IN*
Ray Notarantonio - *Infineon Technologies Americas, Livonia, MI*

41 - SPECIAL SESSION: CYBER-PHYSICAL SYSTEM ARCHITECTURES AND DESIGN METHODOLOGIES

Time: 1:30 - 3:00pm || Room: 304
Track: Embedded Systems || Topic Area: Embedded System Architecture and Design

CHAIR:
Mohammad Al Faruque - *Univ. of California, Irvine, CA*
ORGANIZERS:
Mohammad Al Faruque - *Univ. of California, Irvine, CA*
Marilyn Wolf - *Georgia Institute of Technology, Atlanta, GA*

This special session will provide a CAD-centric view of challenges in the design of cyber-physical systems (CPS). Cyber-physical systems require a co-design approach that tightly integrates control system design with computing hardware and software design. Cyber-physical systems often require networked computing architectures. Traditional CAD challenges, such as timing analysis, co-simulation, and design verification become more complex when translated to the cyber-physical domain. CPS architectures and methodologies bear some important similarities to system-on-chip design but have many significant differences as well.

41.1 What Don't We Know About CPS Architecture? (1:30)
Marilyn Wolf, Eric Feron - *Georgia Institute of Technology, Atlanta, GA*

41.2 Design Tool Chain for Cyber-Physical Systems: Lessons Learned (2:00)
Janos Sztipanovits, Ted Bapty, Sandeep Neema, Xenofon Koutsoukos, Ethan Jackson - *Vanderbilt Univ., Nashville, TN*

41.3 Models, Abstractions, and Architectures: The Missing Links in Cyber-Physical Systems (2:30)
Bharathan Balaji - *Univ. of California at San Diego, La Jolla, CA*
Mohammed Al Faruque, Nikil Dutt - *Univ. of California, Irvine, CA*
Rajesh Gupta - *Univ. of California at San Diego, La Jolla, CA*
Yuvraj Agarwal - *Carnegie Mellon Univ., Pittsburgh, PA*

42 - NEED FOR SPEED: ACCELERATING EMBEDDED SYSTEMS

Time: 1:30 - 3:00pm || Room: 305
Track: Embedded Systems || Topic Area: Embedded System Architecture and Design

CHAIR:
Michael Huebner - *Ruhr Univ. Bochum, Germany*
CO-CHAIR:
Houman Homayoun - *George Mason Univ., Fairfax, VA*

The session focuses on pushing embedded system performance by using accelerators. The session begins with a warp scheduler to reduce the cache miss rate in GPGPU applications. The scalability of heterogeneous accelerator-based CMPs is then discussed. The next paper introduces a configurable NoC architecture for energy efficiency, performance and reliability. Then, an approximate configurable adder is presented to trade-off performance and output quality. The session continues with an efficient accelerator for real-time image feature extraction. We conclude with a talk on exploiting the cell level write imbalance to mitigate write disturbance in dense Phase Change Memory.

42.1 VWS: A Versatile Warp Scheduler for Exploring Diverse Cache Localities of GPGPU Applications (1:30)
Mengjie Mao - *Univ. of Pittsburgh, PA*
Jingtong Hu - *Oklahoma State Univ., Stillwater, OK*
Yiran Chen, Hai Li - *Univ. of Pittsburgh, PA*

42.2 Revisiting Accelerator-Rich CMPs: Challenges and Solutions (1:45)
Nasibeh Teimouri, **Hamed Tabkhi,** Gunar Schirner - *Northeastern Univ., Boston, MA*

42.3 SuperNet: Multimode Interconnect Architecture for Manycore Chips (2:00)
Haseeb Bokhari - *Univ. of New South Wales, Syndey, Australia*
Haris Javaid - *Google, Inc., Mountain View, CA*
Muhammad Shafique, Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*

42.4 A Low Latency Generic Accuracy Configurable Adder (2:15)
Muhammad Shafique - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Waqas Ahmad, Rehan Hafiz - *National University of Science and Technology, Islamabad, Pakistan*
Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

42.5 A 127 fps in Full HD Accelerator Based on Optimized AKAZE with Efficiency and Effectiveness for Image Feature Extraction (2:30)
Guangli Jiang, Leibo Liu, Wenping Zhu, Shouyi Yin, Shaojun Wei - *Tsinghua Univ., Beijing, China*

42.6 Exploit Imbalanced Cell Writes to Mitigate Write Disturbance in Dense Phase Change Memory (2:45)
Rujia Wang, Lei Jiang, Youtao Zhang - *Univ. of Pittsburgh, PA*
Linzhang Wang - *Nanjing Univ., Jiangsu, China*
Jun Yang - *Univ. of Pittsburgh, PA*

Q & A Poster Session
3:00 - 3:30pm - Esplanade Foyer

43 - MAKING DESIGNS MORE RELIABLE AND ROBUST

Time: 1:30 - 3:00pm || Room: 310 || Track: EDA || Topic Area: Digital Circuits

CHAIR:
Chung-Kuan Cheng - *Univ. of California at San Diego, La Jolla, CA*
CO-CHAIR:
Cheng Zhuo - *Intel Corp., Hillsboro, OR*

Reliability and power integrity are increasingly important concerns for digital designers, due to increased integration density, decreased supply voltages and new architectures. Traditional methods may suffer from either inefficiency or large guard bands. In this session, you will learn techniques spanning from system level soft error simulation to power integrity analysis and optimization, as well as methods of enhancing resiliency and power efficiency of SoCs and 3D system designs.

43.1 Understanding Soft Errors in Uncore Components (1:30)
Hyungmin Cho - *Stanford Univ., Stanford, CA*
Chen-Yong Cher - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Thomas Shepherd, Subhasish Mitra - *Stanford Univ., Standford, CA*

43.2 Interconnect Reliability Modeling and Analysis for Multi-Branch Interconnect Trees (1:45)
Hai-Bao Chen - *Shanghai Jiao Tong Univ., Shanghai, China*
Sheldon X.-D. Tan - *Univ. of California, Riverside, CA*
Valeriy Sukharev - *Mentor Graphics Corp., Fremont, CA*
Xin Huang, **Taeyoung Kim** - *Univ. of California, Riverside, CA*

43.3 Design, Packaging, and Architectural Policy Co-Optimization for DC Power Integrity in 3D DRAM (2:00)
Yarui Peng, Bon Woong Ku - *Georgia Institute of Technology, Atlanta, GA*
Younsik Park, Kwang-Il Park, Seong-Jin Jang, Joo Sun Choi - *Samsung Electronics Co., Ltd., Gyeonggi-do, Republic of Korea*
Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*

43.4 Tier-Partitioning for Power Delivery vs Cooling Tradeoff in 3D VLSI for Mobile Applications (2:15)
Shreepad Panth - *Georgia Institute of Technology, Atlanta, GA*
Kambiz Samadi, Yang Du - *Qualcomm Technologies, Inc., San Diego, CA*
Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*

43.5 Novel Power Grid Reduction Method based on L1 Regularization (2:30)
Ye Wang, Meng Li, Xinyang Yi, Zhao Song, Michael Orshansky, Constantine Caramanis - *Univ. of Texas at Austin, TX*

43.6 A Statistical Methodology for Noise Sensor Placement and Full-Chip Voltage Map Generation (2:45)
Xiaochen Liu - *ShanghaiTech Univ., Shanghai, China*
Shupeng Sun - *Carnegie Mellon Univ., Pittsburg, PA*
Pingqiang Zhou - *ShanghaiTech Univ., Shanghai, China*
Xin Li - *Carnegie Mellon Univ. and Fudan Univ., Pittsburgh, PA*
Haifeng Qian - *IBM T.J. Watson Research Center, Yorktown Heights, NY*

Q & A Poster Session
3:00 - 3:30pm - Esplanade Foyer

44 - DESIGNER TRACK: TOOLING AND SOFTWARE FOR EMBEDDED SYSTEMS

Sponsored by: Mentor Graphics®

Time: 1:30 - 3:00pm || Room: 101
Track: Embedded Systems || Topic Area: Embedded Software

CHAIR:
Andrew Putnam - *Microsoft Research, Redmond, WA*
CO-CHAIR:
Jan Rellermeyer - *IBM Research, Austin, TX*

The software portion of embedded systems is getting increasingly more important as devices are becoming more flexible and powerful. At the same time, there is a continued need for tooling around embedded platforms. This session highlights latest advancements in software/tooling for the areas of design, power checking, debugging, and simulation.

44.1 Early Power Checker Tool (1:30)
Rohit K. Murarka, Deepak K. Arora, Pankaj Agarwal - *STMicroelectronics, Greater Noida, India*
Chetan Bisht - *STMicroelectronics, Lawrenceville, GA*

44.2 Continuous Integration Build and Release Ingredients* (1:45)
Chin Liang See, **Tien Hock Loh** - *Altera Corp., Penang, Malaysia*

44.3 FPGA Design Validation Using System Console (2:00)
Lean Kim Ong - *Altera Corp., Bayan Lepas, Malaysia*

44.4 Cw: Domain-Specific C for Wireless (2:15)
Debashis Bhattacharya - *Huawei Technologies Co., Ltd., Plano, TX*
Mark Brown, Lee McFearin - *FutureWei Technologies, Inc., Plano, TX*
Ankit Sethia, Janghaeng Lee, Scott Mahlke - *Univ. of Michigan, Ann Arbor, MI*

44.5 System Simulator for High-Speed Link Design* (2:30)
Shengbo Xu, Chao Wang, An-Jui Shey - *Oracle Corporation, Santa Clara, CA*

44.6 HW/SW Debug in Post-Silicon Environments (2:45)
Brian Bowen - *Intel Corp., Camino, CA*

*** Indicates Best Paper Candidate**

Q & A Poster Session
6:00 - 7:00pm - Esplanade Foyer

45 - DESIGNER TRACK: THE EXPANDING WORLD OF SYSTEM VERIFICATION

Sponsored by: Mentor Graphics

Time: 1:30 - 3:00pm || Room: 105 || Track: Security || Topic Area: Security

CHAIR:
Jennifer Shen Hwang - *QuickLogic Corp., Sunnyvale, CA*

As System Complexity increases so has the resultant verification problem, this session explores the expanding areas that system level verification must include. Over time the verification problem has added more and more system aspects that need to be validated. Hardware/ Software verification has been prevalent for a while, Analog mixed signal verification has now become a standard aspect of verification plans. What other areas should we consider when we plan what we need to do to verify of our chips and how will new techniques allow for better efficiency in our Giga-Scale world.

45.1 How to Secure Embedded Devices in Today's Hostile Environment (1:30)
Amrit Mundra - *Texas Instruments, Inc., Dallas, TX*
45.2 System Level Verification of High Speed Serial Interfaces (2:00)
Faisal Haque - *Verification Central LLC, Santa Clara, CA*
45.3 Above OS Level Software Testing for Mobile SOC (2:30)
Vikramjeet Singh - *NVIDIA Corporation, Santa Clara, CA*

SKY TALK: CHIPS FOR AUTOMOTIVE - IC ROBUSTNESS VERIFICATION IN THE BRAVE NEW WORLD OF ISO 26262

Time: 3:30 - 4:00pm || Room: Booth 311
Track: Automotive || Topic Area: Physical Design

CHAIR:
Anthony Cooprider - *Ford Motor Co., Dearborn, MI*

Electronics are playing an expanding role in automotive platforms. Their application is no longer tied to traditional systems such as airbag controllers or engine control but also expanding rapidly into advanced driver assistance systems. Reliable design of robust semiconductors for such systems, including compliance to industry standards like ISO 26262, became a critical success factor in this market. Meeting such standards - especially in the physical layout domain - requires advanced verification tool functionality and frameworks to ensure a reliable and traceable flow of requirements from the specification down to the layout development.

SPEAKER:
Maik Herzog - *Infineon Technologies AG, Munich, Germany*

46 - SPECIAL SESSION: SECURING CYBER-PHYSICAL SYSTEMS: FROM SURVEILLANCE TO TRANSPORTATION AND HOME

Time: 4:30 - 6:00pm || Room: 300 || Track: Security || Topic Area: Security

CHAIR:
Xin Li - *Carnegie Mellon Univ., Pittsburg, PA*
ORGANIZER:
Qi Zhu - *Univ. of California, Riverside, CA*

Security attacks could have critical impact on cyber-physical systems, endangering users and causing large-scale infrastructure failures in extreme circumstances. Compared with traditional computing systems,addressing CPS security faces many unique challenges, with the fast increase of system scale and complexity, the close interactions with dynamic physical environment and human activities, the large volume and variations of sensor inputs, the employment of distributed architectural platforms, and the often tight real-time constrains. In this session, speakers from government agency, industry, and research institutions will introduce the security challenges in several critical CPS domains including surveillance, transportation, and energy systems. They will demonstrate the importance of having design automation methodologies and tools for combating CPS security challenges, and present promising approaches in quantitative modeling, simulation and analysis of security elements, and in automated security-aware optimization and verification.

46.1 Cloning Your Mind: Security Challenges in Cognitive System Designs and Their Solutions (4:30)
Beiye Liu, Chunpeng Wu - *Univ. of Pittsburgh, PA*
Qing Wu, Mark Barnell - *Air Force Research Lab, Rome, NY*
Qinru Qiu - *Syracuse Univ., Syracuse, NY*
Hai (Helen) Li, Yiran Chen - *Univ. of Pittsburgh, PA*
46.2 Design and Verification for Transportation System Security (5:00)
Bowen Zheng - *Univ. of California, Riverside, CA*
Wenchao Li - *SRI International, Menlo Park, CA*
Peng Deng - *Univ. of California, Riverside, CA*
Léonard Gérard - *SRI International, Menlo Park, CA*
Qi Zhu - *Univ. of California, Riverside, CA*
Natarajan Shankar - *SRI International, Menlo Park, CA*
46.3 Impact Assessment of Net Metering on Smart Home Cyberattack Detection (5:30)
Yang Liu, **Shiyan Hu** - *Michigan Technological Univ., Houghton, MI*
Jie Wu, Yiyu Shi - *Missouri Univ. of Science and Technology, Rolla, MO*
Yier Jin - *Univ. of Central Florida, Orlando, FL*
Yu Hu, Xiaowei Li - *Chinese Academy of Sciences, Beijing, China*

47 - SPECIAL SESSION: SAFETY COMPLIANCE IN AUTOMOTIVE SYSTEMS: STANDARDS, TECHNIQUES AND CHALLENGES

Time: 4:30 - 6:00pm || Room: 303 || Track: Automotive || Topic Area: Automotive Systems

CHAIR:
Juergen Teich - *Univ. of Erlangen-Nuremberg, Germany*
ORGANIZERS:
Samarjit Chakraborty - *Technische Univ. München, Germany*
Anthony Cooprider - *Ford Motor Co., Dearborn, MI*

Given the safety-critical nature of many automotive applications, compliance with safety standards is one of the most important problems in this domain. While techniques for ensuring conformance with safety standards in other domains like avionics is well-studied, the cost-sensitive nature of the automotive domain, coupled with the push towards off-the-shelf components and the need for component reuse, makes safety-related problems much more challenging for the automotive systems design. This session will feature three talks addressing different aspects of the ISO 26262 standard for the automotive domain and discuss design issues around it.

47.1 Ensuring Functional Safety Compliance for ISO 26262 (4:30)
Adam Sherer, John Rose - *Cadence Design Systems, Inc., Chelmsford, MA*
Riccardo Oddone - *Cadence Design Systems, Inc., Milan, Italy*

47.2 Automating Design-Space Exploration: Optimal Deployment of Automotive SW-Components in an ISO26262 Context (5:00)
Bernhard Schatz, Sebastian Voss, Sergey Zverlov - *fortiss GmbH, München, Germany*

47.3 Developing to ISO 26262 Compliance for Component Reuse (5:30)
Robert Bates - *Mentor Graphics Corp., Fremont, CA*

48 - PANEL: SCALABLE VERIFICATION: EVOLUTION OR REVOLUTION?

Time: 4:30 - 6:00pm || Room: 304
Track: Embedded Systems || Topic Area: Test and Verification

MODERATOR:
Brian Bailey - *Semiconductor Engineering, Beaverton, OR*
ORGANIZERS:
Graham Bell - *Real Intent, Inc., Sunnyvale, CA*
Harry Foster - *Mentor Graphics Corp., Plano, TX*

The EDA industry has made great strides in improving IP blocks and subsystem designs through the adoption of industry verification standards, such as SystemVerilog, Unified Power Format (UPF), Unified Coverage Interoperability Standard (UCIS), and the Universal Verification Methodology (UVM). While the industry generally agrees on methodologies used to verify IP blocks or subsystems, we lack consensus on approaches required to verify SoC integration and system-level functionality of embedded systems. Can existing standards and methodologies be extended to address system-level challenges, or are new approaches required?

PANELISTS:
Hillel Miller - *Freescale Semiconductor, Inc., Austin, TX*
Mark Glasser - *NVIDIA Corporation, Santa Clara, CA*
Ali Habibi - *Qualcomm, Inc., San Diego, CA*
Steven Jorgensen - *Hewlett-Packard Co., Sacramento, CA*
Bill Greene - *ARM Ltd., Austin, TX*

49 - ENERGY-AWARE MEMORY DESIGN AND MODELS FOR RESILIENCY

Time: 4:30 - 6:00pm || Room: 305
Track: EDA || Topic Area: Embedded System Architecture and Design

CHAIR:
Jose Ayala - *Complutense Univ., Madrid, Spain*
CO-CHAIR:
Eli Bozorgzadeh - *Univ. of California, Irvine, CA*

This session presents various methods for designing energy-efficient memories ranging from Content Addressable Memories to STT-RAMs as well as error models-to facilitate energy-accuracy trade-offs at the architecture and dataflow levels. In particular, four papers address energy and aging issues in the memory sub-system by using techniques at the circuit and architectural level. The other two papers focus on aspects related to approximate computing, in particular the use of approximate operators and the definition of error models for overscaled computational units.

49.1 Energy-Efficient Non-Volatile TCAM Search Engine Design Using Priority-Decision in Memory Technology for DPI (4:30)
Hsiang-Jen Tsai, Keng-Hao Yang, Yin-Chi Peng - *National Chiao Tung Univ., Hsinchu, Taiwan*
Chien-Chen Lin - *National Tsing Hua Univ., Hsinchu, Taiwan*
Ya-Han Tsao - *National Chiao Tung Univ., Hsinchu, Taiwan*
Meng-Fan Chang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Tien-Fu Chen - *National Chiao Tung Univ., Hsinchu, Taiwan*

49.2 EnAAM: Energy-Efficient Anti-Aging for On-Chip Video Memories (4:45)
Muhammad Shafique, Muhammad Usman
Karim Khan, Orcun Tuefek, Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

49.3 Mitigating the Impact of Faults in Unreliable Memories For Error-Resilient Applications (5:00)
Shrikanth Ganapathy - *École Polytechnique Fédérale de Lausanne, Switzerland*
Georgios Karakonstantis - *Queen's Univ. Belfast & École Polytechnique Fédérale de Lausanne, Switzerland*
Adam Teman, Andreas Burg - *École Polytechnique Fédérale de Lausanne, Switzerland*

49.4 A STT-RAM-based Low-Power Hybrid Register File for GPGPUs (5:15)
Gushu Li - *Tsinghua Univ., Beijing, China*
Xiaoming Chen - *Carnegie Mellon Univ., Pittsburgh, PA*
Guangyu Sun - *Peking Univ., Beijing, China*
Henry Hoffmann - *Univ. of Chicago, IL*
Yongpan Liu, Yu Wang, Huazhong Yang - *Tsinghua Univ., Beijing, China*

49.5 Joint Precision Optimization and High Level Synthesis for Approximate Computing (5:30)
Chaofan Li, Wei Luo - *Texas A&M Univ., College Station, TX*
Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*
Jiang Hu - *Texas A&M Univ., College Station, TX*

49.6 b-HiVE: A Bit-Level History-Based Error Model with Value Correlation for Voltage-Scaled Integer and Floating Point Units (5:45)
Georgios Tziantzioulis, Ali Murat Gok - *Northwestern Univ., Evanston, IL*
S M Faisal - *Ohio State Univ., Columbus, OH*
Nikos Hardavellas, Seda Ogrenci-Memik - *Northwestern Univ., Evanston, IL*
Srinivasan Parthasarathy - *Ohio State Univ., Columbus, OH*

Q & A Poster Session
6:00 - 7:00pm - Esplanade Foyer

50 - EMBEDDED SOFTWARE FOR HETEROGENEOUS PLATFORMS

Time: 4:30 - 6:00pm || Room: 310
Track: Embedded Systems || Topic Area: Embedded Software

CHAIR:
Frank Slomka - *Univ. of Ulm, Germany*
CO-CHAIR:
Jian-Jia Chen - *Technische Univ. Dortmund, Germany*

The papers in this session present techniques aimed at solving some of the most important issues regarding efficient use of heterogeneous architectures in modern embedded systems. Some of the papers present specific solutions to software optimization for general purpose GPU-based mobile platforms. The main application areas considered are gaming, real-time scene labeling, and image processing. The solutions proposed are compile time optimization based as well as intelligent runtime resource management approaches.

50.1 SVP: Host-GPU Multiplexing for Efficient Simulation of Multiple Embedded GPUs on Virtual Platforms (4:30)
YoungHoon Jung, Luca P. Carloni - *Columbia Univ., New York, NY*

50.2 Power-Performance Modelling of Mobile Gaming Workloads on Heterogeneous MPSoCs (4:45)
Anuj Pathania - *Karlsruhe Institute of Technology, Karlsruhe., Germany*
Alexandru Irimiea, **Alok Prakash**, Tulika Mitra - *National Univ. of Singapore, Singapore*

50.3 HARS: a Heterogeneity-Aware Runtime System for Self-Adaptive Multithreaded Applications (5:00)
Jaeyoung Yun, Jinsu Park, Woongki Baek - *Ulsan National Institute of Science and Technology, Ulsan, Republic of Korea*

50.4 Accelerating Real-Time Embedded Scene Labeling with Convolutional Networks (5:15)
Lukas Cavigelli, Michele Magno, Luca Benini - *Swiss Federal Institute of Technology, Zurich, Switzerland*

50.5 SmartBalance: A Sensing-Driven Linux Load Balancer for Energy Efficiency of Heterogeneous MPSoCs (5:30)
Santanu Sarma, Tiago R. Muck, Luis A. Bathen, Nikil Dutt, Alex Nicolau - *Univ. of California, Irvine, CA*

50.6 Optimizing Stream Program Performance on CGRA-based Systems (5:45)
Hongsik Lee, Dong M. Nguyen, **Jongeun Lee** - *Ulsan National Institute of Science and Technology, Ulsan, Republic of Korea*

Q & A Poster Session
6:00 - 7:00pm - Esplanade Foyer

51 - DESIGNER TRACK: TAMING THE COMPLEXITY BEAST

Sponsored by: Mentor Graphics

Time: 4:30 - 6:00pm || Room: 101
Track: EDA || Topic Area: Designer and IP Track

CHAIR:
Ruggero Castagnetti - *Avago Technologies, San Jose, CA*

Every new process node and every new application demands ever more complex chips. The industry continues to redefine how we measure the complexity of chips from gates/transistors and performance to the large number of integrated IP blocks and processor cores to how little power is consumed by the so-called Dark Silicon. Then there is the physical design complexity of implementing all that in the smallest die size, integrating analog components and sensors, on a new process that is barely out of R&D labs, and of course, making them manufacturable for the greatest yield. Whatever your definition of complexity, as designers we must adapt our tools and methodologies to manage such complexity and deliver working chips that are at the heart of today's systems.

In this session, speakers will share insight they gained from the challenges they faced in their most recent projects and what they would differently next time.

51.1 Fast Custom Repowering; From the Ground Up (4:30)
Greg Ford - *IBM Corp., San Jose, CA*

51.2 Building Reliability Into Large Integrated SOCs (5:00)
Anthony Hill - *Texas Instruments, Inc., Dallas, TX*

51.3 Reducing the Complexity of Power Management and Verification (5:30)
Ken Wagner - *PMC-Sierra, Inc., Burnaby, CA*

52 - DESIGNER TRACK: NEW DIRECTIONS IN STATIC AND FORMAL METHODS

Sponsored by: Mentor Graphics

Time: 4:30 - 6:00pm || Room: 105
Track: Silicon Design || Topic Area: Test and Verification

CHAIR:
Vigyan Singhal - *Oski Technology, Inc., Mountain View, CA*
CO-CHAIR:
Nitin Mhaske - *Atrenta Inc., Austin, TX*

Static and formal methods continue to play a critical role in the validation of modern designs. Increasing complexity makes it continually more important to "shift left" and validate each aspect of a system at the earliest possible point, and these types of methods are often the key enablers of this shift. In this session we will hear about a variety of innovative new ways to use these technologies, covering a broad range of static and formal areas including traditional property verification, linting strategies, assertion synthesis, clock domain crossing, and formal equivalence.

52.1 Better Schedule with Formal Verification (4:30)
Paul Jagodik - *Soft Machines, Santa Clara, CA*

52.2 RTL2RTL Formal Equivalence: Boosting the Design Confidence* (4:45)
Achutha Kiran Kumar V. Madhunapantula, Aarti Gupta, Bindumadhava S. Singanamalli - *Intel Corp., Bangalore, India*

52.3 Synthesis of SystemVerilog Assertion(SVA) (5:00)
Mala Bandyopadhyay, Abhijit Chakrabarty, **Sayantan Das** - *Verific Design Automation, Alameda, CA*

52.4 Clock Domain Crossing Considerations with Deep Sequential Optimizations for Low Power (5:15)
Jianfeng Liu, Mi-Suk Hong, Kyungtae Do - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*
SungHo Park - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Mohit Kumar, Srihari Yechangunja, Vishnu Kanwar, Gagan Minocha, Divya Parihar - *Calypto Design Systems, Inc., Noida, India*

52.5 Hierarchical Lint with Abstract Models: An Efficient, Practical and Scalable Flow for Billion Gate SoCs* (5:30)
Hameed Shaik, Sreenivas Akurati - *Broadcom Corp., Benguluru, India*
Anuj Kumar - *Atrenta Inc., Noida, India*
Lokesh Kapoor, Anup Gupta - *Atrenta Inc., Bengaluru, India*
Manoj Bhatnagar - *Atrenta Inc., San Jose, CA*

52.6 System Verilog Assertion Based CDC Verification Flow (5:45)
Sudhakar Surendran - *Texas Instruments, Inc., Bangalore, India*
Harish Maruthiyodan, Gokulakrishnan Manoharan - *Texas Instruments India Pvt. Ltd., Bangalore, India*
Venu S - *Texas Instruments, Inc., Freising, Germany*
Jagdish C. Rao - *Texas Instruments, Inc., Bangalore, India*
Deepak Ahuja, Paras M. Jain, Ravindra Nibandhe - *Atrenta Inc., Noida, India*
Shaker Sarwary - *Atrenta Inc., San Jose, CA*
Sudeep Mondal - *Atrenta Inc., Noida, India*

*** Indicates Best Paper Candidate**

Q & A Poster Session
6:00 - 7:00pm - Esplanade Foyer

WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 - 7:00pm

TODAY'S POSTER SESSION IS IN THE ESPLANADE FOYER.

86.1 Effective Routing Pattern Generation for Self-Aligned Quadruple Patterning
Takeshi Ihara, Atsushi Takahashi - *Tokyo Institute of Technology, Meguro, Japan*
Chikaaki Kodama - *Toshiba Corp., Yokohama, Japan*

86.2 Adaptive Lane Borrowing of Hybrid Memory Cube
Xianwei Zhang, Youtao Zhang, Jun Yang - *Univ. of Pittsburgh, PA*

86.3 Virtual Collision Array Based Router Design for Network-on-Chip
He Zhou, Linda S. Powers - *Univ. of Arizona, Tucson, AZ*
Jin Sun - *Nanjing Univ., Jiangsu, China*
Janet M. Roveda - *Univ. of Arizona, Tucson, AZ*

86.4 Deep Packet Field Extraction Engine (DPFEE): A Pre-Processing Module for Network Intrusion Detection and Denial-of-Service Detection Systems
Vinayaka Jyothi - *New York Univ., Ozone Park, NY*
Sateesh K. Addepalli - *New York Univ., San Jose, CA*
Ramesh Karri - *New York Univ., Brooklyn, NY*

86.6 Multilayer MoS2 Based Tunnel Transistor-An Effective Switching for Logic Applications
Muhammad Sanaullah, Masud H. Chowdhury - *Univ. of Missouri, Kansas City, MO*

86.7 Compact Piece-Wise Linear Digital Logic Approximations of Hyperbolic Tangent
Mark Fishkin, **William Smith**, Viktor Pracht, Timothy N. Miller - *SUNY Binghamton, NY*

86.8 Robust Online Monitoring of Signal Temporal Logic
Jyotirmoy V. Deshmukh - *Toyota Technical Center, Gardena, CA*
Alexandre Donze, Shromona Gosh - *Univ. of California, Berkeley, CA*
Xiaoqing Jin - *Toyota Technical Center, Gardena, CA*
Garvit Juniwal, Sanjit Seshia - *Univ. of California, Berkeley, CA*

86.9 Reconfigurable Three Dimensional Photovoltaic Panel Architecture for Solar-Powered Time Extension
Donghwa Shin - *Yeungnam Univ., Gyeongsan, Republic of Korea*
Naehyuck Chang - *Korea Advanced Institute of Science and Technology, Kaejeon, Republic of Korea*
Yanzhi Wang, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

86.10 Uniform Control Over Heterogeneous Cores Through NoC-Level Isolation
Nils Asmussen, Benedikt Nöthen, Marcus Völp, Oliver Arnold, Hermann Härtig, Gerhard Fettweis - *Technische Univ. Dresden, Germany*

86.11 Xronos: High-Level Synthesis of Streaming Applications
Endri Bezati - *École Polytechnique Fédérale de Lausanne, Switzerland*
Simone Casale Brunet, Marco Mattavelli - *Swiss Federal Institute of Technology, Lausanne, Switzerland*
Jorn Janneck - *Lund Univ., Lund, Sweden*

86.12 Polyhedral-Based Loop Fusion for Highly Efficient Accelerator Synthesis
Kenshu Seto - *Tokyo City Univ., Setagaya-ku, Japan*

86.13 Post-Silicon Model Checking of Analog/RF Designs Using Cooperative Test Generation and Behavior-Learning
Barry Muldrey, Sabyasachi Deyati, Abhijit Chatterjee - *Georgia Institute of Technology, Atlanta, GA*

86.15 Flexible FFT Optimization and RTL Generation in the Chisel Hardware Description Language
Stephen D. Twigg, John Wawrzynek - *Univ. of California, Berkeley, CA*

86.16 Hardware Bug Triage Using Machine Learning
Rico Angell, Benjamin Oztalay, Noel Bhattacharyya, **Andrew DeOrio** - *Univ. of Michigan, Ann Arbor, MI*

86.17 An Optimal Microarchitecture for Finding Similarities in Complex Networks Based on Optimal Memory Hierarchies
Christian Brugger, Valentin Grigorovici, Matthias Jung, Christian Weis, Christian De Schryver, Katharina A. Zweig, Norbert Wehn - *Univ. of Kaiserslautern, Germany*

86.18 PAC: Probabilistic Approximation Compiler
Pooja Roy, Jianxing Wang, Weng-Fai Wong - *National Univ. of Singapore, Singapore*

86.20 Synthesis of Efficient Stochastic Logic for Multivariate Polynomials
Kyounghoon Kim - *Samsung Electronics Co., Ltd and Seoul National Univ., Seoul, Republic of Korea*
Jongeun Lee - *Ulsan National Institute of Science and Technology, Ulsan, Republic of Korea*
Kiyoung Choi - *Seoul National Univ., Seoul, Republic of Korea*

86.21 Generic, EDA-Standard Based Elaboration Scheme for the Efficient Monolithic Simulation of Heterogeneous Systems
Cédric Ben Aoun, Liliana L. Andrade, Torsten Maehne, François Pêcheux, Marie-Minerve Louërat - *Pierre-and Marie-Curie Univ., Paris, France*
Alain Vachoux - *Ecole Polytechnique Fédérale de Lausanne, Switzerland*

86.22 Robust Key Extraction from SRAM-PUFs for Embedded Systems
Zhenglin Liu, **Wenchao Liu**, Zhenhua Zhang, Zhenhua Zhang, Miaoxin Li, Xuecheng Zou, Qiaoling Tong - *Huazhong Univ. of Science & Technology, Wuhan, China*

86.23 Privacy and Security in Internet of Things: A Case Study on Google Nest Thermostat
Orlando Arias, Grant Hernandez, **Yier Jin** - *Univ. of Central Florida, Orlando, FL*

86.24 DC2: A Distributed Connected Components Detection Algorithm for Large-Scaled On-Chip Networks
Pengju Ren, Chenxi Yang, Kang Hu, Nanning Zheng - *Xi'an Jiaotong Univ., Xi'an, China*

86.25 Ultra-Low Read Leakage SRAM Cell Utilizing Independently-Controlled-Gate FinFETs
Mohsen Imani, Shruti Patil - *Univ. of California at San Diego, La Jolla, CA*
Mohsen Jafari - *Univ. of Michigan, Ann Arbor, MI*
Tajana Rosing - *Univ. of California at San Diego, La Jolla, CA*

86.26 Read Leveling for Flash Storage Systems
Chun-Yi Liu - *Academia Sinica, Taipei, Taiwan*
Yu-Ming Chang - *Macronix International Co., Ltd., Hsinchu, Taiwan*
Yuan-Hao Chang - *Academia Sinica, Taipei, Taiwan*

86.27 Multi-Stage Multi-Rate Digital Filters Design Automation Using Global Optimization
Ahmed M. Ibrahim - *Nile Univ., 6th of October City, Egypt*
Amr G. Wassal - *Cairo Univ., Giza, Egypt*

86.28 Combined SRAM Read/Write Assist Techniques for Near/Sub-Threshold Voltage Operation
Farah B. Yahya, Harsh N. Patel, Benton H. Calhoun
- Univ. of Virginia, Charlottesville, VA
Vikas Chandra - *ARM Ltd., San Jose, CA*

86.29 A Fast Hierarchical Arbitration in Optical Network-on-Chip Based on Multi-Level Priority QOS Service
Jian Jie, Lai Mingche, Xiao Liquan - *National Univ. of Defense Technology, Changsha, China*

86.30 ApproxEigen: An Approximate Computing Technique for Large-Scale Eigen-Decomposition
Qian Zhang, Ting Wang, Ye Tian, Feng Yuan, Qiang Xu
- Chinese Univ. of Hong Kong, Hong Kong

86.31 Operation-Level Approximations for Quality-Energy Optimization in Hardware/Software Compilation
Seogoo Lee, Dongwook Lee, Lizy K. John, Andreas Gerstlauer
- Univ. of Texas at Austin, TX

86.32 Design Methodologies, Models and Tools for Very-Large-Scale Integration of NEM Relay-Based Circuits
Tian Qin, Sunil Rana - *Univ. of Bristol, Bristol, United Kingdom*
Christopher L. Ayala - *IBM Research - Zurich, Switzerland*
Antonios Bazigos - *Ecole Polytechnique Fédérale de Lausanne, Switzerland*
Christoph Hagleitner - *IBM Research - Zurich, Switzerland*
Adrian M. Ionescu - *Ecole Polytechnique Fédérale de Lausanne, Switzerland*
Roberto A. Canegallo - *STMicroelectronics, Agrate Brianza, Italy*
Dinesh Pamunuwa - *Univ. of Bristol, Bristol, United Kingdom*

86.33 A New Tightly-Coupled Transient Electro-Thermal Co-Simulator with Capacitance and Matrix Exponential Method
Quan Chen, **Qinggao Mei** - *Univ. of Hong Kong, Hong Kong*
Wim Schoenmaker - *Magwel, Leuven, Belgium*
Ngai Wong - *Univ. of Hong Kong, Hong Kong*

86.34 An Efficient Verification Framework for Audio/Video Interfaces of State of the Art Entertainment Products
Noha A. Shaarawy, Mustafa M. Khairallah, Khaled Khalifa, Hany Salah, Mohamed El Ashrafy - *Boost Valley, Cairo, Egypt*
Maged Ghoneima - *Ain Shams Univ., Cairo, Egypt*
Randa Hashem - *Boost Valley, Cairo, Egypt*

86.35 A Methodology to Generate Evenly Distributed Input Stimuli By Clustering of Variable Domain
Jomu George Mani Paret, **Otmane Ait Mohamed** - *Concordia Univ., Montréal, QC, Canada*

86.37 A Lossless Compressive Sensing for 3D-IC Test Data Compression
Hantao Huang, Sai Manoj P D, Hao Yu - *Nanyang Technological Univ., Singapore, Singapore*
Fengbo Ren - *Univ. of California, Los Angeles, CA*
Senthilkumar Jayapal - *MediaTek, Singapore Pte. Ltd., Singapore, Singapore*

86.38 Verification of Sequential Arithmetic Circuits
Cunxi Yu, Walter E. Brown, Duo Liu, Samaneh Ghandali, Maciej Ciesielski - *Univ. of Massachusetts, Amherst, MA*

86.39 Guiding CLB Placement to Speed Up Reconfiguration and Improve Endurance of NVM-Based FPGAs
Yuan Xue - *Univ. of Delaware, Newark, Germany*
Patrick T. Cronin - *Univ. of Delaware, Townsend, Germany*
Chengmo Yang - *Univ. of Delaware, Newark, Germany*
Jingtong Hu - *Oklahoma State Univ., Stillwater, OK*

86.40 Machine Learning Recommender System for Detailed Placement
Aysa Fakheri Tabrizi, Logan M. Rakai, Laleh Behjat
- Univ. of Calgary, AB, Canada

86.41 Subarray Level Power-Gating in STT-MRAM Caches to Mitigate Energy Impact of Peripheral Circuits
Eishi Arima - *Univ. of Tokyo, Japan*
Hiroki Noguchi - *Toshiba Corp., Kawasaki, Japan*
Takashi Nakada, Shinobu Miwa - *Univ. of Tokyo, Japan*
Susumu Takeda - *Toshiba Corp., Kawasaki-shi, Japan*
Shinobu Fujita - *Toshiba Corp., Kawasaki, Japan*
Hiroshi Nakamura - *Univ. of Tokyo, Japan*

86.42 A Reconfigurable Virtual Channel Allocator for Many-Core Systems
Mohammad Sadrosadati, Amirhossein Mirhosseini
- Sharif Univ. of Technology, Tehran, Iran
Fatemeh Aghamohammadi - *Univ. of Southern California, Los Angeles, CA*
Mehdi Modarressi - *Univ. of Tehran, Tehran, Iran*
Hamid Sarbazi-Azad - *Sharif Univ. of Technology, Tehran, Iran*

86.43 A Simplified Phase Model for Oscillator Based Computing
Yan Fang, Victor V. Yashin, Nicholas M. Moellers, Andrew J. Seel, Donald Chiarulli, **Steven Levitan** - *Univ. of Pittsburgh, PA*

86.44 Phone-Nomenon: A System-Level Thermal Simulator for Smartphones
Chi-Wen Pan - *National Chiao Tung Univ., Hsinchu, Taiwan*
Hung Wen Chiou - *National Chiao Tung Univ., Taipei, Taiwan*
Yu-Min Lee - *National Chiao Tung Univ., Hsinchu, Taiwan*
Tai-Yu Chen, Sheng-Liang Li, Wen-Sung Hsu, Tao Cheng
- MediaTek, Inc., Hsinchu, Taiwan

86.45 Parallel FPGA Router Using OpenMP for Multicore Platforms
Abhijit S. Deshpande, Sheetalkumar R. Mehta, Shridhar Laddha
- Sasken Communication Technologies Ltd., Bangalore, India
Shihming Liu, Chao-Chiang Chen - *Agate Logic, Inc., Santa Clara, CA*

86.46 Energy-Aware Memory Mapping for Hybrid FRAM-SRAM Based Microcontrollers
Hrishikesh Jayakumar, Arnab Raha, Vijay Raghunathan - *Purdue Univ., West Lafayette, IN*

86.47 Having Your Cake and Eating It Too: Energy Savings Without Performance Loss Through Resource Sharing Driven Power Management
Jae-Yeon Won, **Paul Gratz**, Srinivas Shakkottai, Jiang Hu
- Texas A&M Univ., College Station, TX

86.48 A New Random Walk Algorithm for 3-D Capacitance Extraction Considering Boundary Element Macromodel
Wenjian Yu, Bolong Zhang, Chao Zhang, Haiquan Wang
- Tsinghua Univ., Beijing, China
Luca Daniel - *Massachusetts Institute of Technology, Cambridge, MA*

WORK-IN-PROGRESS POSTER SESSION

86.49 Dynamic Data Migration to Eliminate Bank-Level Interference for Data Parallel Applications in Multicore Systems
Wei-Hen Lo, Yen-Hao Chen, TingTing Hwang - *National Tsing Hua Univ., Hsinchu, Taiwan*

86.50 Equivalence Checking Between SLM and RTL Using Machine Learning Techniques
Jian Hu, Tun Li, Sikun Li, Yu Luo - *National Univ. of Defense Technology, Chang Sha, China*

86.51 Big Data on Little Cores - Are Low Power Processors a Good Fit for Big Data Workloads?
Maria Malik, Houman Homayoun - *George Mason Univ., Fairfax, VA*

86.52 Runtime Detection of a Bandwidth Denial Attack from a Rogue Network-on-Chip
Rajesh Jayashankara Shridevi, Dean Ancajas, Koushik Chakraborty, Sanghamitra Roy - *Utah State Univ., Logan, UT*

86.53 A Scalable Simulation Framework for Network/System Co-Simulation
Jungsoo Kim - *Samsung Electronics Co., Ltd., Suwon-Si, Republic of Korea*
Hansu Cho - *Samsung Electronics Co., Ltd., Suwon-Si, Republic of Korea*
Xinnian Zheng, Parisa Razaghi - *Univ. of Texas at Austin, TX*
Seungwook Lee, Byeong Kil Lee, Seungwook Lee - *Samsung Electronics Co., Ltd., Suwon-si, Republic of Korea*

86.54 MEMMap: Memory-Aware Application Mapping on Coarse-Grained Reconfigurable Architectures
Shouyi Yin, Xianqing Yao, Leibo Liu, Shaojun Wei - *Tsinghua Univ., Beijing, China*

86.55 A Novel Approach for Automatically Comparing Analog Behavior
Alexander W. Rath, Sebastian Simon - *Infineon Technologies AG, Neubiberg, Germany*
Volkan Esen - *Infineon Technologies AG, Munich, Germany*
Wolfgang Ecker - *Infineon Technologies AG, Neubiberg, Germany*

86.56 Tenacious Hardware Trojans Due to High Temperature in Middle Tiers of 3-D ICs
Syed Rafay Hasan, Siraj Fulum Mossa, Omar Elkeelany - *Tennessee Technological Univ., Cookeville, TN*

86.57 A Methodology to Optimize Design Pattern Context Size Using Pattern Association Tree (PAT)
Piyush Pathak, Shikha Somani, Piyush Verma, Sriram Madhavan - *GLOBALFOUNDRIES, Santa Clara, CA*
Luigi Capodieci - *GLOBALFOUNDRIES, Milpitas, CA*

86.58 ApproxBER: A Checkpointing Framework for Quality-Guaranteed Approximate Computing
Ting Wang, Qian Zhang, Ye Tian, Feng Yuan, Qiang Xu - *Chinese Univ. of Hong Kong, Hong Kong*

86.59 Development of a Cooperative Hardware/Software Instruction Fetch (CIF) Mechanism for Designing Mobile Application Processors
Yong Kyu Jung, Paul S. Jung - *Adaptmicrosys LLC, Erie, PA*

86.60 High-Sigma Performance Analysis Using Multi-Objective Evolutionary Algorithms
Martin Trefzer, James A. Walker, Simon J. Bale, Andy Tyrrell - *Univ. of York, United Kingdom*

86.61 Design and Analysis of Sequential Reversible Logic Structures Using Nanomagnet Logic
Alexander Gunter, Matthew Morrison - *Univ. of Mississippi, Oxford, MS*

86.62 Design of a Cost-Effective Real-Time Simulator Platform Capable of Hardware-in-the-Loop Simulation for an Automated Collision Prevention (ACoP) System
Troy Silloway, **Yong-Kyu Jung**, Idrees Alzahid - *Gannon Univ, Erie, PA*

86.63 Automated Voltage-Aware Design Rule Checking
Dina Medhat - *Mentor Graphics Corp., Cairo, Egypt*
Sophie Billy - *Mentor Graphics Corp., Meudon, France*

86.64 Overcoming the Challenges of Analog Mixed Signal Simulation: Custom Boundary Elements
Pulkit Bhatnagar, Amit Singh, Saurabh Jha - *STMicroelectronics, Greater Noida, India*

86.65 LEF/DEF IO Ring Check Automation
Dina Medhat - *Mentor Graphics Corp., Cairo, Egypt*
Matthew Hogan - *Mentor Graphics Corp., Wilsonville, OR*
Fabrice Blanc, Abdellah Bakhali - *ARM Ltd., Grenoble, France*

86.66 Towards Efficient Hardware Debugging Using Parameterized FPGA Reconfiguration
Alexandra Kourfali, Dirk Stroobandt - *Ghent Univ., Belgium*

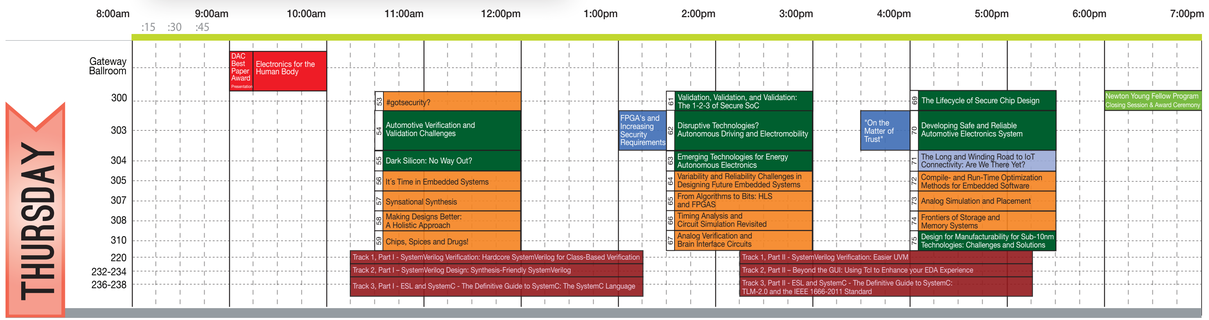
86.67 Dual Computational Layer Based Logic Design for QCA Circuits
Arman Roohi, Ronald F. DeMara, Navid Khoshavi - *Univ. of Central Florida, Orlando, FL*

86.69 A Novel PUF Based on Cell Error Rate Distribution of STT-RAM
Xian Zhang, Guangyu Sun - *Peking Univ., Beijing, China*
Yaojun Zhang, Wujie Wen, Yiran Chen - *Univ. of Pittsburgh, PA*
Jia Di - *Univ. of Arkansas, Fayetteville, AR*

86.70 Decentralized Diagnosis of Permanent Faults in Automotive E/E Architectures
Peter Waszecki, Martin Lukasiewycz - *TUM CREATE Ltd., Singapore, Singapore*
Samarjit Chakraborty - *Technische Univ. München, Germany*

86.71 Fault Diagnosis and Logic Debugging of Arithmetic Circuits
Samaneh Ghandali, **Cunxi Yu**, Duo Liu, Walter E. Brown, Maciej Ciesielski - *Univ. of Massachusetts, Amherst, MA*

THURSDAY SCHEDULE



THURSDAY - NETWORKING RECEPTION

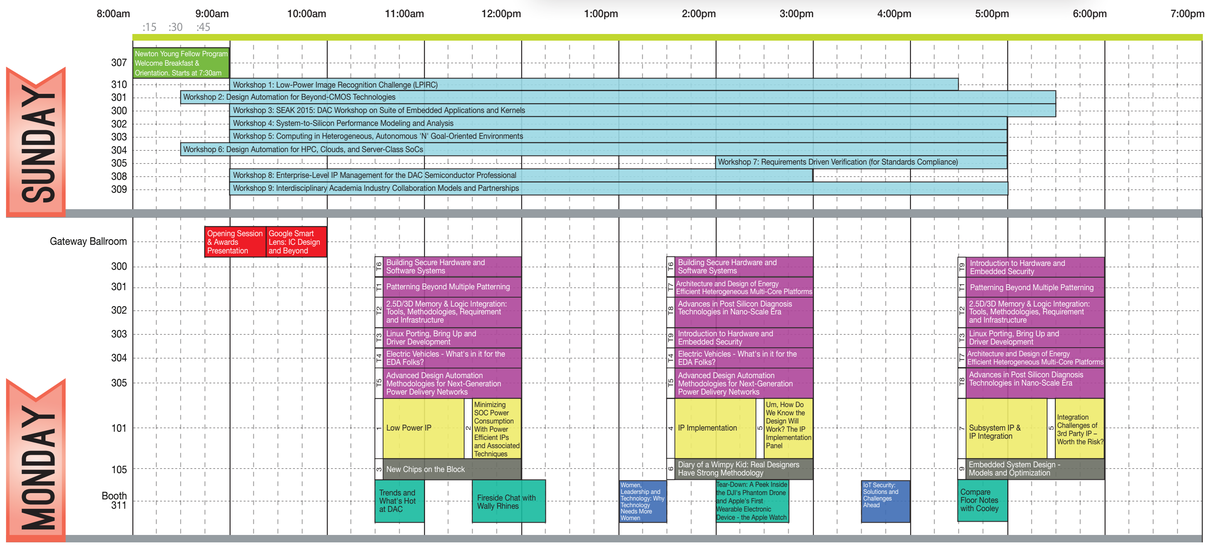
5:30 - 6:30PM | ESPLANADE FOYER

Join attendees for refreshments and lively discussion recapping the days' events.

EVENT TYPES LEGEND:

- Keynotes
- SKY Talks
- Research Sessions
- Special Sessions
- Technical Panels
- DAC Pavilion
- Designer Track
- IP Track
- Tutorials
- Workshops
- Thursday is Training Day
- Work-in-Progress
- Management Day
- Additional Meeting

SUNDAY/MONDAY SCHEDULE



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SUNDAY - WELCOME RECEPTION

5:30 - 7:00PM | INTERCONTINENTAL HOTEL

Join fellow attendees for the first event to network and kick-off DAC 2015!

Sponsored by: Austin – THE MUSIC CAPITAL OF THE WORLD –

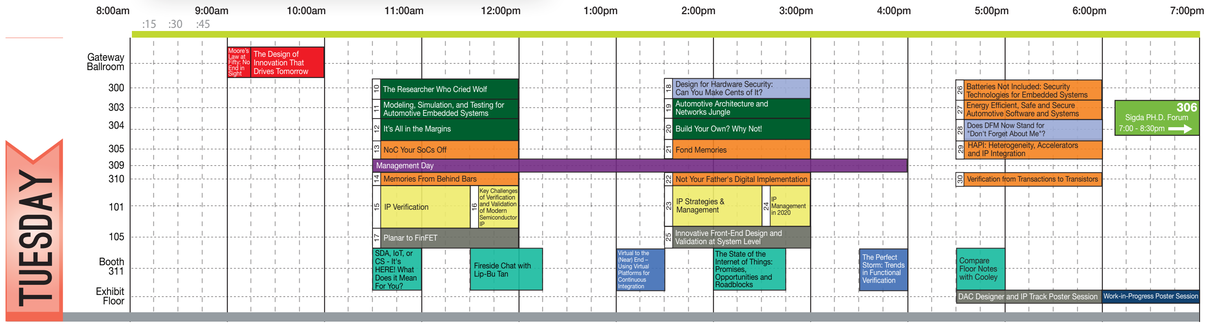
MONDAY - COCKTAILS & CONVERSATIONS

Sponsored by: AMIQ, 25 Years Excellence in Engineering, University of Southampton, OpenTeXT, SILVACO, ESC

6:00 - 7:00PM | EXHIBIT FLOOR

Join us on the Exhibit floor to meet with exhibitors and enjoy light hors' d'oeuvres and beverages.

TUESDAY SCHEDULE



TUESDAY - DAC IP TRACK & DESIGNER TRACK POSTER SESSION

4:30 - 6:00PM | EXHIBIT FLOOR

Sponsored by:

ChipEstimate.com Mentor Graphics

TUESDAY - COCKTAILS & CONVERSATIONS WORK-IN-PROGRESS POSTER SESSION

6:00 - 7:00PM | EXHIBIT FLOOR

Join us on the Exhibit floor to meet with exhibitors and enjoy light hors' d'oeuvres and beverages.

Sponsored by:

AMIQ 25 concept engineering DASSAULT SYSTEMES The 3DEXPERIENCE Company OPENTEXT SILVACO S2C FPGA PROTOTYPING SOLUTIONS

EVENT TYPES LEGEND:

- Keynotes
- SKY Talks
- Research Sessions
- Special Sessions
- Technical Panels
- DAC Pavilion
- Designer Track
- IP Track
- Tutorials
- Workshops
- Thursday is Training Day
- Work-in-Progress
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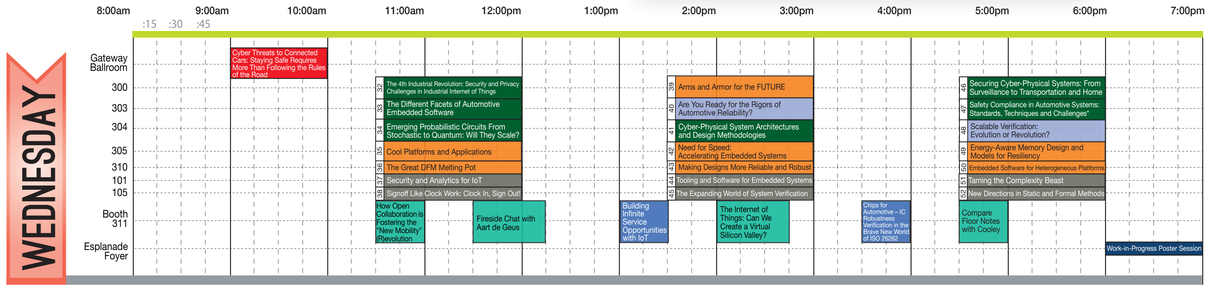
- Additional Meeting

WEDNESDAY SCHEDULE



WEDNESDAY - NETWORKING RECEPTION & WORK-IN-PROGRESS POSTER SESSION

6:00 - 7:00PM | ESPLANADE FOYER

The DAC Work-in-Progress (WIP) poster session aims to provide authors and opportunity to network with peer feedback on current work and preliminary results. Join the presenters in the Esplanade Foyer for their presentations.

Sponsored by:

SemiWiki.com

EVENT TYPES LEGEND:

- Keynotes
- SKY Talks
- Research Sessions
- Special Sessions
- Technical Panels
- DAC Pavilion
- Designer Track
- IP Track
- Tutorials
- Workshops
- Thursday is Training Day
- Work-in-Progress
- Management Day
- Additional Meeting

DAC BEST PAPER AWARD PRESENTATION

Time: 9:00am - 9:15am || Room: Gateway Ballroom

KEYNOTE PRESENTATION

ELECTRONICS FOR THE HUMAN BODY

John Rogers - *Professor, Univ. of Illinois at Urbana-Champaign, IL*

Time: 9:15am - 10:00am || Room: Gateway Ballroom Track: Silicon Design
Topic Area: General Interest

Summary: Biology is soft, curvilinear and adaptable; silicon technology is rigid, planar and immutable. Electronic systems that eliminate this profound mismatch in properties create opportunities for devices that can intimately integrate with the body, for diagnostic, therapeutic or surgical function with important, unique capabilities in biomedical research and clinical healthcare. Over the last decade a convergence of new concepts in materials science, mechanical engineering, manufacturing techniques and device designs has led to the emergence of diverse classes of 'biocompatible' electronics. This talk describes the key ideas, with examples ranging from 'cellular-scale' light emitting diodes that can be injected into the brain for optogenetic behavioral control to bioresorbable electronics that can serve as non-antibiotic bacteriocides for treating surgical site infections.

Biography: Professor John A. Rogers obtained BA and BS degrees in chemistry and in physics from the University of Texas, Austin, in 1989. From MIT, he received SM degrees in physics and in chemistry in 1992 and the PhD degree in physical chemistry in 1995. From 1995 to 1997, Rogers was a Junior Fellow in the Harvard University Society of Fellows. He joined Bell Laboratories as a Member of Technical Staff in the Condensed Matter Physics Research Department in 1997, and served as Director of this department from the end of 2000 to 2002. He is currently Swanlund Chair Professor at University of Illinois at Urbana/Champaign, with a primary appointment in the Department of Materials Science and Engineering, and joint appointments in several other departments, including Chemistry. He is Director of the Seitz Materials Research Laboratory. Rogers' research includes fundamental and applied aspects of materials for unusual electronic and photonic devices, with an emphasis on bio-integrated and bio-inspired systems. He is a member of the National Academy of Engineering and the American Academy of Arts and Sciences. He won a MacArthur Fellowship in 2009, the Lemelson-MIT Prize in 2011 and the Smithsonian Award for Ingenuity in the Physical Sciences in 2013.

53 - #GOTSECURITY?

Time: 10:30am - 12:00pm || Room: 300 || Track: Security || Topic Area: Security

CHAIR:
Sandip Ray - *Intel Corp., Hillsboro, OR*
CO-CHAIR:
Yier Jin - *Univ. of Central Florida, Orlando, FL*

Modern globalization of the electronic supply chain has resulted in significant vulnerabilities related to hardware Trojans, IP piracy, and counterfeit electronics. This session contains a potpourri of work addressing these contemporary issues. This includes novel optical imaging and formal verification methods for hardware Trojan detection, novel watermarking and obfuscation techniques to protect IP at chip and PCB levels respectively, on-chip voltage regulators that suppress side channel information leakage, and a novel TRNG design for FPGAs.

53.1 Detecting Hardware Trojans Using Backside Optical Imaging of Embedded Watermarks (10:30)
Boyou Zhou, Ronen Adato, Mahmoud Zangeneh, Tianyu Yang, Aydan Uyar, Bennett Goldberg, Selim Unlu, Ajay Joshi
- Boston Univ., Boston, MA

53.2 Detecting Malicious Modifications of Data in Third Party Intellectual Property Cores (10:45)
Jeyavijayan Rajendran - *Polytechnic Institute of New York Univ., Brooklyn, NY*
Vivekananda Vedula - *TSR Labs, Austin, TX*
Ramesh Karri - *New York Univ., Brooklyn, NY*

53.3 A Practical Circuit Fingerprinting Method Utilizing Observability Don't Care Conditions (11:00)
Carson J. Dunbar, **Gang Qu** - *Univ. of Maryland, College Park, MD*

53.4 Investigation of Obfuscation-based Anti-Reverse Engineering for Printed Circuit Boards (11:15)
Zimu Guo - *Univ. of Connecticut, Storrs, CT*
Jia Di - *Univ. of Arkansas, Fayetteville, AR*
Mark Tehranipoor, Domenic Forte - *Univ. of Connecticut, Storrs, CT*

53.5 Leveraging On-Chip Voltage Regulators as a Countermeasure Against Side-Channel Attacks (11:30)
Selcuk Kose, **Weize Yu**, Orhun Aras Uzun - *Univ. of South Florida, Tampa, FL*

53.6 Highly Efficient Entropy Extraction for True Random Number Generators on FPGAs (11:45)
Vladimir Rožić, Bohan Yang, Wim Dehaene, Ingrid Verbauwhede
- Katholieke Univ. Leuven, Belgium

Q & A Poster Session
12:00 - 12:30pm - Esplanade Foyer

54 - SPECIAL SESSION: AUTOMOTIVE VERIFICATION AND VALIDATION CHALLENGES

Time: 10:30am - 12:00pm || Room: 303 || Track: Automotive || Topic Area: Automotive Systems

CHAIR:
Anthony Cooprider - *Ford Motor Co., Dearborn, MI*

The highly cost sensitive nature of the automotive domain - and therefore the tight resource budgets - brings up new challenges in certification, verification and validation, that do not exist in other domains like avionics. Further, since both hardware and software components are sourced from different suppliers, verification and validation is all the more challenging. This session will feature three talks discussing different aspects of automotive verification and the associated challenges.

54.1 Mining Requirements from Closed Loop Control Models (10:30)
Xiaoqing Jin - *Toyota Technical Center, Torrance, CA*

54.2 Design & Verification of Automotive SoC Firmware (11:00)
Veit Kleeberger, Stefan Rutkowski, Ruth Coppens
- Infineon Technologies AG, Neubiberg, Germany

54.3 Model Based Testing of Automotive Software: Some Challenges and Solutions (11:30)
Alexandre Petrenko, Omer Nguena Timo - *Computer Research Institute of Montreal, QC, Canada*
Sethu Ramesh - *General Motors Company, Warren, MI*

55 - SPECIAL SESSION: DARK SILICON: NO WAY OUT?

Time: 10:30am - 12:00pm || Room: 304
Track: Embedded Systems || Topic Area: Embedded System Architecture and Design

CHAIR:
Ulf Schlichtmann - *Technische Univ. München, Germany*
ORGANIZERS:
Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Muhammad Shafique - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

The goal of this special session is to expose Dark Silicon challenges for design automation, architecture, and system-level design communities along with an overview of some of the early research efforts that are attempting to shape the design and run-time management of future generation heterogeneous Dark Silicon processors. In particular, this special session aims at clarifying whether "Dark Silicon introduces fundamentally new challenges for the community" or "the Dark Silicon is merely an additional constraint for the system designer". Our broader goal is to spur greater awareness and discussion of these challenges in the design automation community, and to position the Dark Silicon problem as one that this community can have a large impact on solving.

55.1 New Trends in Dark Silicon (10:30)
Jörg Henkel, Heba Khdr, Santiago Pagani, Muhammad Shafique - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

55.2 Approximate Computing and the Quest for Computing Efficiency (11:00)
Swagath Venkataramani - *Purdue Univ., West Lafayette, IN*
Srimat Chakradhar - *NEC Labs America, Inc., Princeton, NJ*
Kaushik Roy - *Purdue Univ., West Lafayette, IN*
Anand Raghunathan - *Purdue Univ., Lafayette, IN*

55.3 Core vs. Uncore: Which Part of Silicon is Darker? (11:30)
Yuan Xie - *Univ. of California, Santa Barbara, CA*
Hsiangyun Cheng - *Pennsylvania State Univ., Univerity Park, PA*
Jia Zhan - *Univ. of California, Santa Barbara, CA*
Jishen Zhao - *Univ. of California, Santa Cruz, CA*
Jack Sampson, Mary Jane Irwin - *Pennsylvania State Univ., Univerity Park, PA*

56 - IT´S TIME IN EMBEDDED SYSTEMS

Time: 10:30am - 12:00pm || Room: 305
Track: Embedded Systems || Topic Area: Embedded System Architecture and Design

CHAIR:
Alexandre Donze - *Univ. of California, Berkeley, CA*
CO-CHAIR:
Miroslav Velev - *Aries Design Automation, LLC, Chicago, IL*

Many embedded systems are concerned with the timing behavior as well as timeliness. This session presents novel approaches to analyze and optimize the execution and response time of embedded systems in the worst case and with probabilistic guarantees, harvest power to run an application to meet a required timing behavior using a technique called energy migration, and design and synthesize a set of embedded platforms rather than a single system by presenting an efficient design space exploration methodology.

56.1 A Generic Representation of CCSL Time Constraints for UML/MARTE Models (10:30)
Judith Peters - *Univ. of Bremen, Germany*
Robert Wille - *Univ. of Bremen & DFKI GmbH, Bremen, Germany*
Nils Przigoda, Ulrich Kühne - *Univ. of Bremen, Germany*
Rolf Drechsler - *Univ. of Bremen & DFKI GmbH, Bremen, Germany*

56.2 Improving Worst-Case Cache Performance through Selective Bypassing and Register-Indexed Cache (10:45)
Mohamed Ismail, Daniel Lo, G. Edward Suh - *Cornell Univ., Ithaca, NY*

56.3 PACO: Fast Average-Performance Estimation for Time-Randomized Caches (11:00)
Suzana Milutinovic - *Barcelona Supercomputing Center and Univ. Politecnica de Catalunya, Barcelona, Spain*
Eduardo Quinones, Jaume Abella, Francisco J. Cazorla - *Barcelona Supercomputing Center, Barcelona, Spain*

56.4 Increasing Confidence in Measurement-Based Contention Bounds for Real-Time Round-Robin Buses (11:15)
Gabriel A. Fernandez - *Barcelona Supercomputing Center and Univ. Politecnica de Catalunya, Barcelona, Spain*
Javier Jalle, Jaume Abella, Eduardo Quinones - *Barcelona Supercomputing Center, Barcelona, Spain*
Tullio Vardanega - *Univ. of Padova, Italy*
Francisco J. Cazorla - *Barcelona Supercomputing Center, Barcelona, Spain*

56.5 Deadline-Aware Task Scheduling for Solar-Powered Nonvolatile Sensor Nodes with Global Energy Migration (11:30)
Daming Zhang, Yongpan Liu, Xiao Sheng, Jinyang Li, Tongda Wu - *Tsinghua Univ., Beijing, China*
Chun Jason Xue - *City Univ. of Hong Kong, Hong Kong*
Huazhong Yang - *Tsinghua Univ., Beijing, China*

56.6 Efficient Design Space Exploration of Embedded Platforms (11:45)
Martin Lukasiewycz, Florian Sagstetter, Sebastian Steinhorst - *TUM CREATE Ltd., Singapore, Singapore*

Q & A Poster Session
12:00 - 12:30pm - Esplanade Foyer

57 - SYNSATIONAL SYNTHESIS

Time: 10:30am - 12:00pm || Room: 307 || Track: EDA || Topic Area: Synthesis and FPGAs

CHAIR:
Lingyi Liu - *Synopsys, Inc., Mountain View, CA*
CO-CHAIR:
William Hung - *Synopsys, Inc., Mountain View, CA*

The mapping of RTL to logic gates is one of the miracles of design automation. The quality of the design in terms of power, area, and the ability to close timing critically depends on the quality of the underlying logic synthesis algorithms. This session presents innovations in Boolean optimization, synthesis of circuits that operate at multiple operating points, graphene-based logic circuits, and circuits with retention registers for power gating.
It also explores the synthesis of stochastic logic, which is an alternative model of using pseudo-random bit-streams.

57.1 Boolean Logic Optimization in Majority-Inverter Graphs (10:30)
Luca Amaru, Pierre-Emmanuel Gaillardon - *Swiss Federal Institute of Technology, Lausanne, Switzerland*
Giovanni De Micheli - *Ecole Polytechnique Fédérale de Lausanne, Switzerland*

57.2 One-Pass Logic Synthesis for Graphene-Based Pass-XNOR Logic Circuits (10:45)
Valerio Tenace, **Andrea Calimera**, Enrico Macii, Massimo Poncino - *Politecnico di Torino, Italy*

57.3 OSFA: A New Paradigm of Gate Sizing for Power/ Performance Optimizations under Multiple Operating Conditions (11:00)
Subhendu Roy, Derong Liu - *Univ. of Texas at Austin, TX*
Junhyung Um - *Samsung Semiconductor, Inc., Yongin City, Republic of Korea*
David Z. Pan - *Univ. of Texas at Austin, TX*

57.4 Scalable Sequence-Constrained Retention Register Minimization in Power Gating Design (11:15)
Ting-Wei Chiang - *National Taiwan Univ., Taipei, Taiwan*
Kai-Hui Chang - *Avery Design Systems, Inc., Tewksbury, MA*
Yen-Ting Liu - *Avery Design Systems, Inc., Andover, MA*
Jie-Hong (Roland) Jiang - *National Taiwan Univ., Taipei, Taiwan*

57.5 Equivalence Among Stochastic Logic Circuits and Its Application (11:30)
Te-Hsuan Chen, John P. Hayes - *Univ. of Michigan, Ann Arbor, MI*

57.6 Randomness Meets Feedback: Stochastic Implementation of Logistic Map Dynamical Systems (11:45)
Zhiheng Wang, Naman Saraf, Kia Bazargan, Arnd Scheel - *Univ. of Minnesota, Twin Cities, Minneapolis, MN*

Q & A Poster Session
12:00 - 12:30pm - Esplanade Foyer

58 - MAKING DESIGNS BETTER: A HOLISTIC APPROACH

Time: 10:30am - 12:00pm || Room: 308 || Track: EDA || Topic Area: Digital Circuits

CHAIR:
Miguel Miranda - *Qualcomm Technologies, Inc., San Diego, CA*
CO-CHAIR:
Alberto Macii - *Politecnico di Torino, Italy*

Power delivery, performance, and high quality are key challenges in any design project. We propose multiple solutions across the design hierarchy, beginning with a method for recycling charge in a 3D die stack. Next we look at optimizing battery life on systems large and small. Then, we look at improving quality and testability. Finally, we explore asynchronous circuits as an option for power reduction and improved performance.

58.1 A Cross-Layer Design Exploration of Charge-Recycled Power-Delivery in Many-Layer 3D-IC (10:30)
Runjie Zhang, Kaushik Mazumdar - *Univ. of Virginia, Charlottesville, VA*
Brett Meyer - *McGill Univ., Montreal, QC, Canada*
Ke Wang, Kevin Skadron, Mircea Stan - *Univ. of Virginia, Charlottesville, VA*

58.2 Optimal Control of PEVs for Energy Cost Minimization and Frequency Regulation in the Smart Grid Accounting for Battery State-of-Health Degradation (10:45)
Tiansong Cui, Yanzhi Wang, Shuang Chen - *Univ. of Southern California, Los Angeles, CA*
Qi Zhu - *Univ. of California, Riverside, CA*
Shahin Nazarian, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

58.3 Evaluating Battery Aging on Mobile Devices (11:00)
Jaeseong Lee, Yohan Chon, Hojung Cha - *Yonsei Univ., Seoul, Republic of Korea*

58.4 Design for Low Test Pattern Counts (11:15)
Haluk Konuk - *Broadcom Corp., Santa Clara, CA*
Elham Moghaddam, Nilanjan Mukherjee, Janusz Rajski - *Mentor Graphics Corp., Wilsonville, OR*
Deepak Solanki - *Broadcom Corp., Irvine, CA*
Jerzy Tyszer, **Justyna Zawada** - *Poznan Univ. of Technology, Poznan, Poland*

58.5 Generation of Close-to-Functional Broadside Tests with Equal Primary Input Vectors (11:30)
Irith Pomeranz - *Purdue Univ., West Lafayette, IN*

58.6 A Lightweight Early Arbitration Method for Low-Latency Asynchronous 2D-Mesh NoC's (11:45)
Weiwei Jiang, Kshitij Bhardwaj - *Columbia Univ., New York, NY*
Geoffray Lacourba - *ARM Ltd., Sophia Antipolis, France*
Steven M. Nowick - *Columbia Univ., New York, NY*

Q & A Poster Session
12:00 - 12:30pm - Esplanade Foyer

59 - CHIPS, SPICES AND DRUGS!

Time: 10:30am - 12:00pm || Room: 310 || Track: EDA || Topic Area: Emerging Technologies

CHAIR:
Smita Krishnaswamy - *Columbia Univ., New York, NY*
CO-CHAIR:
Louis Scheffer - *Howard Hughes Medical Institute, Chevy Chase, MD*

This session will explore new chip architectures, SPICE models and EDA design-flows for micro-fluidic bio-chips, emerging transistor technologies including nanowire FETs, domain wall memories and transition metal devices.

59.1 Nanowire-Aware Routing Considering High Cut-Mask Complexity (10:30)
Yu-Hsuan Su, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

59.2 Optimizing Data Placement for Reducing Shift Operations on Domain Wall Memories (10:45)
Xianzhang Chen, Edwin H.-M. Sha, **Qingfeng Zhuge**, Penglin Dai, Weiwen Jiang - *Chongqing Univ., Chongqing, China*

59.3 A SPICE Model of Flexible Transition Metal Dichalcogenide Field-Effect Transistors (11:00)
Ying-Yu Chen, Zelei Sun, Deming Chen
- *Univ. of Illinois at Urbana-Champaign, IL*

59.4 Reliability-Aware Synthesis for Flow-based Microfluidic Biochips by Dynamic-device Mapping (11:15)
Tsun-Ming Tseng, Bing Li - *Technische Univ. München, Germany*
Tsung-Yi Ho - *National Chiao Tung Univ., Hsinchu, Taiwan*
Ulf Schlichtmann - *Technische Univ. München, Germany*

59.5 PACOR: Practical Control-Layer Routing Flow with Length-Matching Constraint for Flow-Based Microfluidic Biochips (11:30)
Hailong Yao - *Tsinghua Univ., Beijing, China*
Tsung-Yi Ho - *National Chiao Tung Univ., Hsinchu, Taiwan*
Yici Cai - *Tsinghua Univ., Beijing, China*

59.6 Monolayer Transition Metal Dichalcogenide and Black Phosphorous Transistors for Low Power Robust SRAM Design (11:45)
Joydeep Rakshit - *Univ. of Pittsburgh, PA*
Runlai Wan, Kai T. Lam, Jing Guo - *Univ. of Florida, Gainesville, FL*
Kartik Mohanram - *Univ. of Pittsburgh, PA*

Q & A Poster Session
12:00 - 12:30pm - Esplanade Foyer

SKY TALK: FPGA'S AND INCREASING SECURITY REQUIREMENTS

Time: 1:00 - 1:30pm || Room: 303 || Track: Security || Topic Area: Security

CHAIR:
Chuck Alpert - *Cadence Design Systems, Inc., Austin, TX*

There is a major transition in the market: Many customers who only peripherally understand security are now discovering that they have deep security requirements. The old paradigm of here are some bricks and the coordinates of a lime quarry, now go build yourself a wall, no longer works. Complete systems solutions that consider specific use models and threats along with requirements from manufacturing, ecosystem, tools, licensing, etc, must be provided on top of a rock solid silicon and software foundation. This talk will focus on the technical challenges associated with these security solutions which are both unique to FPGA's and common with other silicon providers.

SPEAKER:
Sean Atsatt - *Altera Corp., San Jose, CA*

61 - SPECIAL SESSION: VALIDATION, VALIDATION, AND VALIDATION: THE 1-2-3 OF SECURE SOC

Time: 1:30 - 3:00pm || Room: 300 || Track: Security || Topic Area: Security

CHAIR:
Mark Tehranipoor - *Univ. of Connecticut, Storrs, CT*
ORGANIZERS:
Vikas Chandra - *ARM Ltd., San Jose, CA*
Saibal Mukhopadhyay - *Georgia Institute of Technology, Atlanta, GA*

Modern system-on-chip (SoC) designs contain a number of critical security assets, including keys, firmware, cryptographic modules, fuses, which are sprinkled across multiple intellectual property (IP) blocks often cross-cutting hardware and software boundaries. Consequently, developing an SoC design critically requires: (1) specifying, implementing, and validating security policies to govern the interaction of these assets in field, and (2) developing on-chip security architectures to enable effective validation of SoC resiliency against diverse security attacks and vulnerabilities.

This special session will include three talks that examine the state of the research and practice in this important area from the perspective of validation techniques - both pre-silicon and post-silicon - and SoC security architectures, and in particular emphasize the cooperation and trade-offs between the two areas.

61.1 SoC Security Architecture: Current Practices and Emerging Needs (1:30)
Eric Peeters - *Texas Instruments, Inc., Dallas, TX*

61.2 Pre-Silicon Security Verification and Validation: A Formal Perspective (2:00)
Xiaolong Guo, Raj Gautam Dutta, **Yier Jin** - *Univ. of Central Florida, Orlando, FL*
Farimah Farahmandi, Prabhat Mishra - *Univ. of Florida, Gainesville, FL*

61.3 Correctness and Security at Odds: Post-Silicon Validation of Modern SoC Designs (2:30)
Sandip Ray, Jin Yang - *Intel Corp., Hillsboro, OR*
Abhishek Basak, Swarup Bhunia - *Case Western Reserve Univ., Cleveland, OH*

62 - SPECIAL SESSION: DISRUPTIVE TECHNOLOGIES? AUTONOMOUS DRIVING AND ELECTROMOBILITY

Time: 1:30 - 3:00pm || Room: 303 || Track: Automotive || Topic Area: Automotive Systems

CHAIR:
Sebastian Steinhorst - *TUM CREATE Ltd., Singapore, Singapore*
ORGANIZERS:
Samarjit Chakraborty - *Technische Univ. München, Germany*
Anthony Cooprider - *Ford Motor Co., Dearborn, MI*

Autonomous driving and electromobility are probably the two most disruptive technologies that are currently within the automotive domain. While there is no doubt that eventually both of these are going to become mainstream, there are a wide range of engineering obstacles on the way. This session is going to discuss some important research directions within the areas of electromobility and autonomous driving and points out the opportunities that exist for engineers and researchers.

62.1 Joint Automatic Control of the Powertrain and Auxiliary Systems to Enhance the Electromobility in Hybrid Electric Vehicles (1:30)
Yanzhi Wang, Xue Lin - *Univ. of Southern California, Los Angeles, CA*
Naehyuck Chang - *KAIST, Yuseong-gu, Republic of Korea*
Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

62.2 Formal Methods for Semi-Autonomous Driving (2:00)
Sanjit A. Seshia, Dorsa Sadigh, S. Shankar Sastry - *Univ. of California, Berkeley, CA*

62.3 RACE: Robust and Reliable Automotive Computing Environment for Future e-Cars (2:30)
Cornel Klein - *Siemens Corp., Munich, Germany*

63 - SPECIAL SESSION: EMERGING TECHNOLOGIES FOR ENERGY AUTONOMOUS ELECTRONICS

Time: 1:30 - 3:00pm || Room: 304
Track: Embedded Systems || Topic Area: Emerging Technologies

CHAIR:
Sumeet Gupta - *Pennsylvania State Univ., University Park, PA*
ORGANIZER:
Suman Datta - *Pennsylvania State Univ., University Park, PA*

Battery-less, self-powered electronics are going to play an increasingly important role in our modern society. Their applications will range from personal health monitoring to home automation to enterprise applications like work place safety. This session will present an overview of recent advancements at the circuit, architecture and test-bed applications level that will play a key role in realizing that vision. The first paper will describe an efficient power delivery network utilizing novel circuit topologies and adaptive control techniques to provide power from energy harvesters to millions of transistors operating at very low voltages. The second paper will present the concept and implementation of a ferroelectric non-volatile processor that operates reliably and efficiently in an interrupted power environment. The third paper will describe a test-bed to deploy emerging technologies to demonstrate the feasibility of an energy autonomous personal health monitoring system.

63.1 Integrated Power Management in IoT Devices Under Wide Dynamic Ranges of Operation (1:30)
Samantak Gangopadhyay, Saad Bin Nasir, **Arijit Raychowdhury** - *Georgia Institute of Technology, Atlanta, GA*

63.2 Ambient Energy Harvesting Nonvolatile Processors: From Circuit to System (2:00)
Yongpan Liu, Zewei Li, Hehe Li, Yiqun Wang - *Tsinghua Univ., Beijing, China*
Xueqing Li, Kaisheng Ma - *Pennsylvania State Univ., University Park, PA*
Shuangchen Li - *Univ. of California, Santa Barbara, CA*
Meng-Fan Chang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Sampson John - *Pennsylvania State Univ., University Park, PA*
Yuan Xie - *Univ. of California, Santa Barbara, CA*
Jiwu Shu, Huazhong Yang - *Tsinghua Univ., Beijing, China*

63.3 Self-Powered Wearable Sensor Platforms for Health and Wellness Monitoring (2:30)
Veena Misra - *North Carolina State Univ., Raleigh, NC*

64 - VARIABILITY AND RELIABILITY CHALLENGES IN DESIGNING FUTURE EMBEDDED SYSTEMS

Time: 1:30 - 3:00pm || Room: 305
Track: Embedded Systems || Topic Area: Embedded System Architecture and Design

CHAIR:
Ed Nuckolls - *Freescale Semiconductor, Inc., Austin, TX*
CO-CHAIR:
Vijay Ragunathan - *Purdue Univ., West Lafayette, IN*

This session addresses the key problems of reliability, variability, and schedulability in embedded systems. We begin with a design in which core resources are dynamically scaled based on application needs. Next, we address the issue of variablility in hardware and physical models. We continue with techniques to help satisfy timing constraints in embedded software. The session concludes with a proposed dynamic scrubbing mechanism for FPGAs to recover from memory faults.

64.1 ElasticCore: Enabling Dynamic Heterogeneity With Joint Core and Voltage/Frequency Scaling (1:30)
Mohammad Khavari Tavana, Mohammad Hossein Hajkazemi - *George Mason Univ., Fairfax, VA*
Divya Pathak, Ioannis Savidis - *Drexel Univ., Philadelphia, PA*
Houman Homayoun - *George Mason Univ., Fairfax, VA*

64.2 Task Scheduling Strategies to Mitigate Hardware Variability in Embedded Shared Memory Clusters (1:45)
Abbas Rahimi - *Univ. of California at San Diego, La Jolla, CA*
Daniele Cesarini - *Univ. di Bologna, Italy*
Andrea Marongiu - *Eidgenössische Technische Hochschule Zürich, Switzerland*
Rajesh Gupta - *Univ. of California at San Diego, La Jolla, CA*
Luca Benini - *Eidgenössische Technische Hochschule Zürich, Switzerland*

64.3 Including Variability of Physical Models into the Design Automation of Cyber-Physical Systems (2:00)
Hamid Mirzaei Buini, **Steffen Peter**, Tony Givargis - *Univ. of California, Irvine, CA*

64.4 PASS: Priority Assignment of Real-Time Tasks with Dynamic Suspending Behavior under Fixed-Priority Scheduling (2:15)
Wen-Hung K. Huang, Jian-Jia Chen - *Technische Univ. Dortmund, Germany*
Husheng Zhou, Cong Liu - *Univ. of Texas at Dallas, TX*

64.5 Resource Usage Templates and Signatures for COTS Multicore Processors (2:30)
Gabriel A. Fernandez - *Barcelona Supercomputing Center and Univ. Politecnica de Catalunya, Barcelona, Spain*
Javier Jalle, Jaume Abella, Eduardo Quinones - *Barcelona Supercomputing Center, Barcelona, Spain*
Tullio Vardanega - *Univ. of Padova, Italy*
Francisco J. Cazorla - *Barcelona Supercomputing Center, Barcelona, Spain*

64.6 Dynamically Adaptive Scrubbing Mechanism for Improved Reliability in Reconfigurable Embedded Systems (2:45)
Rui Santos, Shyamsundar Venkataraman, Akash Kumar - *National Univ. of Singapore, Singapore*

Q & A Poster Session
3:00 - 3:30pm - Esplanade Foyer

65 - FROM ALGORITHMS TO BITS: HLS AND FPGAS

Time: 1:30 - 3:00pm || Room: 307 || Track: EDA || Topic Area: Synthesis and FPGAs

CHAIR:
Alex Kondratyev - *Cadence Design Systems, Inc., San Jose, CA*
CO-CHAIR:
Frederic Doucet - *Qualcomm, Inc., San Jose, CA*

High-level synthesis, which maps algorithms to architectures, has witnessed a resurgence of interest and use in recent years. Many success stories for HLS have come in the world of FPGAs. This session presents various advances in HLS for FPGAs, including area-efficient pipelining, near-instant re-configuration, memory partitioning, fault tolerance, and reducing routing congestion in synthesized designs.

65.1 Area-Efficient Pipelining for FPGA-Targeted High-Level Synthesis (1:30)
Ritchie Zhao, Mingxing Tan, Steve Dai, Zhiru Zhang - *Cornell Univ., Ithaca, NY*

65.2 CMOST: A System-Level FPGA Compilation Framework (1:45)
Peng Zhang, Muhuan Huang, Bingjun Xiao, Hui Huang, Jason Cong - *Univ. of California, Los Angeles, CA*

65.3 Avoiding Transitional Effects in Dynamic Circuit Specialisation on FPGAs (2:00)
Karel Heyse, **Dirk Stroobandt** - *Ghent Univ., Belgium*

65.4 Efficient Memory Partitioning for Parallel Data Access in Multidimensional Arrays (2:15)
Chenyue Meng, Shouyi Yin, Peng Ouyang, Leibo Liu, Shaojun Wei - *Tsinghua Univ., Beijing, China*

65.5 High-Level Synthesis of Error Detecting Cores through Low-Cost Modulo-3 Shadow Datapaths (2:30)
Keith A. Campbell, Pranay Vissa - *Univ. of Illinois at Urbana-Champaign, IL*
David Z. Pan - *Univ. of Texas at Austin, TX*
Deming Chen - *Univ. of Illinois at Urbana-Champaign, IL*

65.6 Physically Aware High Level Synthesis Design Flow (2:45)
Masato Tatsuoka, Ryosuke Watanabe, Tatsushi Otsuka, Takashi Hasegawa - *Socionext, Inc, Yokohama, Japan*
Qiang Zhu, Ryosuke Okamura, Xingri Li, Tsuyoshi Takabatake - *Cadence Design Systems, Inc., Yokohama, Japan*

Q & A Poster Session
3:00 - 3:30pm - Esplanade Foyer

66 - TIMING ANALYSIS AND CIRCUIT SIMULATION REVISITED

Time: 1:30 - 3:00pm || Room: 308 || Track: EDA || Topic Area: Digital Circuits

CHAIR:
Igor Keller - *Cadence Design Systems, Inc., Pleasanton, CA*
CO-CHAIR:
Florentin Dartu - *Taiwan Semiconductor Manufacturing Co., Ltd., Austin, TX*

This session offers practical solutions advancing the state of the art in both circuit simulation and timing analysis. We begin with an update to classical circuit simulation for tightly coupled circuits. Following is an accurate approach for noise analysis. Next we solve multiple input switching effects in functional timing simulation, and have a more efficient take on yield optimization. Finally, we add to classical static analysis accounting for modeling inaccuracies and enabling mode merging for faster analysis.

66.1 An Algorithmic Framework for Efficient Large-Scale Circuit Simulation Using Exponential Integrators (1:30)
Hao Zhuang - *Univ. of California at San Diego, La Jolla, CA*
Wenjian Yu - *Tsinghua Univ., Beijing, China*
Ilgweon Kang, Xinan Wang, Chung-Kuan Cheng - *Univ. of California at San Diego, La Jolla, CA*

66.2 Variation Aware Cross-Talk Aggressor Alignment by Mixed Integer Linear Programming (1:45)
Vladimir Zolotov - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Peter Feldmann - *D. E. Shaw Research, New York, NY*

66.3 TA-FTA: Transition-Aware Functional Timing Analysis with A Four-Valued Encoding (2:00)
Che-Chen Chang, Hsuan-Ming Huang, **Louis Y.-Z. Lin**, Charles H.-P. Wen - *National Chiao Tung Univ., Hsinchu, Taiwan*

66.4 An Efficient Algorithm for Statistical Timing Yield Optimization (2:15)
S Ramprasath - *Indian Institute of Technology Madras, Chennai, India*
Vinita Vasudevan - *Indian Institute of Technology, Chennai, India*

66.5 Criticality-Dependency-Aware Timing Characterization and Analysis (2:30)
Yu-Ming Yang - *National Chiao Tung Univ., Hsinchu, Taiwan*
King Ho Tam - *Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan*
Iris Hui-Ru Jiang - *National Chiao Tung Univ., Hsinchu, Taiwan*

66.6 A Timing Graph Based Approach to Mode Merging (2:45)
Subramanyam Sripada - *Synopsys, Inc., Hillsboro, OR*
Murthy Palla - *Synopsys India Pvt. Ltd., Bangalore, India*

Q & A Poster Session
3:00 - 3:30pm - Esplanade Foyer

67 - ANALOG VERIFICATION AND BRAIN INTERFACE CIRCUITS

Time: 1:30 - 3:00pm || Room: 310 || Track: EDA || Topic Area: Analog Circuits

CHAIR:
Radu Zlatanovici - *Intel Corp., Santa Clara, CA*
CO-CHAIR:
Mandy Pant - *Intel Corp., Boston, MA*

This session is focused on methods for analog verification as well as Brain-Computer Interface (BCI) signal processing. The session begins with a paper about the application of Bayesian methods for evaluation of post-layout circuits. Next is a presentation about a method of post-silicon tuning with Markov methods. The application of SMT techniques to analog circuit synthesis is presented afterwards. The fourth paper presents a method for verification of inevitability of phase-locked loop (PLL) circuits. The last two papers concern different aspects of BCI signal processing.

67.1 Efficient Multivariate Moment Estimation via Bayesian Model Fusion for Analog and Mixed-Signal Circuits (1:30)
Qicheng Huang, Chenlei Fang, Fan Yang, Xuan Zeng - *Fudan Univ., Shanghai, China*
Xin Li - *Carnegie Mellon Univ. and Fudan Univ., Pittsburgh, PA*

67.2 mTunes: Efficient Post-Silicon Tuning of Mixed-Signal/RF Integrated Circuits Based on Markov Decision Process (1:45) **Manzil Zaheer**, Fa Wang - *Carnegie Mellon Univ., Pittsburgh, PA*
Chenjie Gu - *Intel Corp., Hillsboro, OR*
Xin Li - *Carnegie Mellon Univ. and Fudan Univ., Pittsburgh, PA*

67.3 Towards Enhancing Analog Circuits Sizing Using SMT-based Techniques (2:00)
Ons Lahiouel, Sofiène Tahar, Mohamed H. Zaki - *Concordia Univ., Montreal, QC Canada*

67.4 Verifying Inevitability of Phase-locking in a Charge Pump Phase Lock Loop using Sum of Squares Programming (2:15)
Hafiz ul Asad - *City Univ., London, United Kingdom*
Kevin D. Jones - *Plymouth Univ., Plymouth, United Kingdom*

67.5 Adaptive Compressed Sensing Architecture in Wireless Brain-Computer Interface (2:30)
Aosen Wang, Chen Song, Zhanpeng Jin, Wenyao Xu - *SUNY Buffalo, NY*

67.6 A Low Power Unsupervised Spike Sorting Accelerator Insensitive to Clustering Initialization in Sub-optimal Feature Space (2:45)
Zhewei Jiang, Qi Wang, Mingoo Seok - *Columbia Univ., New York, NY*

Q & A Poster Session
3:00 - 3:30pm - Esplanade Foyer

SKY TALK: "ON THE MATTER OF TRUST"

Time: 3:30 - 4:00pm || Room: 303 || Track: Security || Topic Area: Security

CHAIR:
Ramesh Karri - *New York Univ., Brooklyn, NY*

Virtually every endeavor in the human experience has been thoroughly penetrated by digital computer technologies. Along with the unprecedented capabilities they provide our civilization, they also present new threats to our personal and national economics, security, and health. The manner by which we bestow trust on the technologies through which we conduct our daily affairs has never been more important, yet evolution has not equipped us to effectively recognize them. Our visual media can be manipulated with Photoshop; our software and networks may be hacked; and the hardware hosting these capabilities is known to often be counterfeited and compromised. Trust is essential to our way of life; it allows us to work and live together.

Given that the human "OS" going forward will be expressed in venues such as Facebook, Google, Apple, and Microsoft which run on these electronic platforms, it is essential that we supplant our own innate sixth sense with a means to accurately assess technical trustworthiness. This talk will provide an overview of the electronic threat space and some of the ideas DARPA is developing to mitigate them. By trading security for convenience, expense, and privacy, the biggest threat to our own security may be within us.

SPEAKER:
Kerry Bernstein - *Defense Advanced Research Projects Agency, Arlington, VA*

69 - SPECIAL SESSION: THE LIFECYCLE OF SECURE CHIP DESIGN

Time: 4:00 - 5:30pm || Room: 300 || Track: Security || Topic Area: Security

CHAIR:
Ingrid Verbauwhede - *Katholieke Univ. Leuven, Belgium*
ORGANIZERS:
Patrick Schaumont - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*
Kazuo Sakiyama - *Univ. of Electro-Communications, Tokyo, Japan*

This session collects three talks that, taken together, describe the design lifecycle of a cryptographic chip. They highlight the unique requirements faced by chip designers when designing secure chips that are subject to physical and logical threats, in particular when those chips may be physically reverse engineered. The first talk gives a cryptographer's view on the chip design process, and discusses a novel lightweight block cipher family, optimized for low-cost implementations in pervasive computing applications. The second talk describes the state of the art in circuit-level countermeasures and its methodologies required to protect chip against powerful semi-invasive adversaries that use sensitive very-near-field EM measurement. The last talk evaluates the challenges of secure chip integration, and assessment of a secure design against known threats. The talks will appeal to a broad audience interested in Secure Chip Design.

69.1 The SIMON and SPECK Lightweight Block Ciphers (4:00)
Ray Beaulieu, Douglas Shors, Jason Smith, Stefan Treatman-Clark, Bryan Weeks, Louis Wingers - *National Security Agency, Fort Meade, MD*

69.2 EM Attack Sensor: Concept, Circuit, and Design-Automation Methodology (4:30)
Noriyuki Miura - *Kobe Univ., Kobe, Japan*
Naofumi Homma, Yuichi Hayashi, Takafumi Aoki - *Tohoku Univ., Sendai, Japan*
Dasuke Fujimoto, Makoto Nagata - *Kobe Univ., Kobe, Japan*

69.3 Design and Integration Challenges of Building Security Hardware IP (5:00)
Megan Wachs, Daniel Ip - *Rambus Cryptography Research Division, San Francisco, CA*

70 - SPECIAL SESSION: DEVELOPING SAFE AND RELIABLE AUTOMOTIVE ELECTRONICS SYSTEM

Time: 4:00 - 5:30pm || Room: 303 || Track: Automotive || Topic Area: Automotive Systems

CHAIR:
Arvind Shanmugavel - *ANSYS, Inc., San Jose, CA*
ORGANIZER:
Ravi Ravikumar - *ANSYS, Inc., San Jose, CA*

The influence of electronics in automobiles is rapidly growing. The key attributes enabling the growth are product differentiation, utility value, driver assistance and government mandated safety requirements. Safety and reliability are two critical attributes of every automotive sub-system. With more electronics content in an automobile, the power efficiency of the electronics is important to ensure longer battery life, especially for an electric car. At the same time, preventing power induced noise failures is required for building a safe and reliable vehicle. Knowing this, what does it take to develop a safe, reliable, power-efficient and cost-effective automotive?

This session will include presentations by semiconductor and system companies developing and delivering various electronics sub-systems present in today's automobiles. Presenters will look at electronics that provide safety, performance, infotainment and motor control. They will discuss their main challenges and requirements, and illustrate their best practices in designing safe, reliable, power-efficient and cost-effective automotive.

70.1 Achieving Power and Reliability Sign-Off for Automotive Semiconductor Designs (4:00)
Ajay Kashyap, Sönke Grimpen, Shyam Sundaramoorthy - *Infineon Technologies India Pvt. Ltd, Bangalore, India*

70.2 Thermal Integrity and Thermal-Aware EM Reliability Check for 3D Stacked Dies in Automotive Application (4:30)
Jehoda Refaeli - *Freescale Semiconductor, Inc., Austin, TX*

70.3 High-Frequency, High-Power Magnetic Design with Maxwell 3D - from Geometry Creation to Component Optimization (5:00)
Jenna Pollock - *Tesla Motors, Inc., Palo Alto, CA*

71 - PANEL: THE LONG AND WINDING ROAD TO IOT CONNECTIVITY: ARE WE THERE YET?

Time: 4:00 - 5:30pm || Room: 304 || Track: EDA || Topic Area: General Interest

MODERATOR:
Nick Sargologos - *Freescale Semiconductor, Inc., Austin, TX*

The anticipated vast growth of IoT devices and applications will be demanding for current network operators: this large scale deployment of potentially inefficient, insecure and even defective IoT devices can lead to critical challenges that impair connectivity for all users, or even worse, bring the network down completely. The way forward is like a winding road: What is the best IoT connectivity solution to address the key challenges of signaling, security, presence detection, power consumption and bandwidth? Will WiFi or low-power radio interfaces suffice, or will we need something new?

PANELISTS:
Aveek Sarkar - *ANSYS, Inc., San Jose, CA*
Alex Jinsung Choi - *SK Telecom Co., Ltd., Seoul, Republic of Korea*
Oleg Logvinov - *IEEE & STMicroelectronics, New York, NY*
Chris Rowen - *Cadence Design Systems, Inc., San Jose, CA*
Dave Flynn - *ARM Ltd., Cambridge, United Kingdom*

72 - COMPILE- AND RUN-TIME OPTIMIZATION METHODS FOR EMBEDDED SOFTWARE

Time: 4:00 - 5:30pm || Room: 305
Track: Embedded Systems || Topic Area: Embedded Software

CHAIR:
Rainer Doemer - *Univ. of California, Irvine, CA*
CO-CHAIR:
Steffen Peter - *Univ. of California, Irvine, CA*

Optimizing the use of resources is a mandatory prerequisite for the design of viable complex embedded systems. The session contains recent approaches that make use of offline and online methods to reduce resource interference, minimize execution time and latency, reduce the power consumption and increase the lifetime of dark silicon devices, and optimize memory footprint and check-pointing in non-volatile processors.

72.1 Thermal Constrained Resource Management for Mixed ILP-TLP Workloads in Dark Silicon Chips (4:00)
Heba Khdr, Santiago Pagani, Muhammad Shafique, Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

72.2 Hayat: Harnessing Dark Silicon and Variability for Aging Deceleration and Balancing (4:15)
Dennis Gnad, **Muhammad Shafique**, Florian Kriebel, Semeen Rehman, Duo Sun, Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

72.3 Network Footprint Reduction through Data Access and Computation Placement In NoC-Based Manycores (4:30)
Jun Liu, **Jagadish B. Kotra**, Wei Ding, Mahmut Kandemir - *Pennsylvania State Univ., State College, PA*

72.4 Designing Time Partitions for Real-Time Hypervisor with Sufficient Temporal Independence (4:45)
Matthias Beckert, Rolf Ernst - *Technische Univ. Braunschweig, Germany*

72.5 Compiler Directed Automatic Stack Trimming for Efficient Non-Volatile Processors (5:00)
Qingan Li - *Wuhan Univ., Wuhan, China*
Mengying Zhao - - *City Univ. of Hong Kong, Hong Kong*
Jingtong Hu - *Oklahoma State Univ., Stillwater, OK*
Yongpan Liu - *Tsinghua Univ., Beijing, China*
Yanxiang He - *Wuhan Univ., Wuhan, China*
Chun Jason Xue - *City Univ. of Hong Kong, Hong Kong*

72.6 Fixing the Broken Time Machine: Consistency-Aware Checkpointing for Energy Harvesting Powered Non-Volatile Processor (5:15)
Mimi Xie - *Oklahoma State Univ., Stillwater, OK*
Mengying Zhao - *City Univ. of Hong Kong, Hong Kong*
Chen Pan, Jingtong Hu - *Oklahoma State Univ., Stillwater, OK*
Yongpan Liu - *Tsinghua Univ., Beijing, China*
Chun Jason Xue - *City Univ. of Hong Kong, Hong Kong*

Q & A Poster Session
5:30 - 6:00pm - Esplanade Foyer

73 - ANALOG SIMULATION AND PLACEMENT

Time: 4:00 - 5:30pm || Room: 307 || Track: EDA || Topic Area: Analog Circuits

CHAIR:
Eli Chiprout - *Intel Corp., Hillsboro, OR*
CO-CHAIR:
Eric Keiter - *Sandia National Laboratories, Albuqerque, NM*

This session concerns new developments in the areas of analog simulation and placement. The first two papers present methods for analog simulation in parallel heterogeneous platforms. The third paper is about a new variant of Balanced Truncation methods for model order reduction. The fourth paper concerns design tools for phase-based logic circuits. The last two papers of the session concern methods for analog placement.

73.1 Transient-Simulation Guided Graph Sparsification Approach to Scalable Harmonic Balance (HB) Analysis of Post-Layout RF Circuits Leveraging Heterogeneous CPU-GPU Computing Systems (4:00)
Lengfei Han, Zhuo Feng - *Michigan Technological Univ., Houghton, MI*

73.2 Parallel Circuit Simulation using the Direct Method on a Heterogeneous Cloud (4:15)
Ahmed E. Helal - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*
Amr M. Bayoumi - *Arab Academy for Science and Technology, Cairo, Egypt*
Yasser Y. Hanafy - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*

73.3 An Efficient Algorithm for Frequency-Weighted Balanced Truncation of VLSI Interconnects in Descriptor Form (4:30)
Vinita Vasudevan, Ramakrishna Mokkapati - *Indian Institute of Technology Madras, Chennai, India*

73.4 Design Tools for Oscillator-Based Computing Systems (4:45)
Tianshi Wang, Jaijeet Roychowdhury - *Univ. of California, Berkeley, CA*

73.5 Layout-Dependent-Effects-Aware Analytical Analog Placement (5:00)
Hung-Chih Ou, Kai-Han Tseng - *National Taiwan Univ., Taipei, Taiwan*
Jhao-Yan Liu - *National Tsing Hua Univ., Hsinchu, Taiwan*
I-Peng Wu, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

73.6 Cutting Structure-Aware Analog Placement Based on Self-Aligned Double Patterning with E-Beam Lithography (5:15)
Hung-Chih Ou, Kai-Han Tseng, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

Q & A Poster Session
5:30 - 6:00pm - Esplanade Foyer

74 - FRONTIERS OF STORAGE AND MEMORY SYSTEMS

Time: 4:00 - 5:30pm || Room: 308
Track: Embedded Systems || Topic Area: Emerging Technologies

CHAIR:
Xiangyu Dong - *Google, Inc., Mountain View, CA*
CO-CHAIR:
H. Howie Huang - *George Washington Univ., Washington, DC*

Continued advances in the performance and capacity of storage systems are increasingly limited by fundamental technological challenges. Device, circuit, and system level solutions are needed to surmount this problem. The Frontiers of Storage and Memory Systems session brings together innovative ideas that push the boundaries of storage systems.

74.1 To Collect or Not to Collect: Just-in-Time Garbage Collection for High-Performance SSDs with Long Lifetimes (4:00)
Sangwook Shane Hahn - *Seoul National Univ., Seoul, Republic of Korea*
Sungjin Lee - *Massachusetts Institute of Technology, Cambridge, MA*
Jihong Kim - *Seoul National Univ., Seoul, Republic of Korea*

74.2 Achieving SLC Performance with MLC Flash Memory (4:15)
Yu-Ming Chang - *Macronix International Co., Ltd., Hsinchu, Taiwan*
Yuan-Hao Chang - *Academia Sinica, Taipei, Taiwan*
Tei-Wei Kuo - *Academia Sinica and National Taiwan Univ., Taipei, Taiwan*
Yung-Chun Li, Hsiang-Pang Li - *Macronix International Co., Ltd., Hsinchu, Taiwan*

74.3 Virtual Flash Chips: Rethinking the Layer Design of Flash Devices to Improve Data Recoverability (4:30)
Ming-Chang Yang - *Academia Sinica and National Taiwan Univ., Taipei, Taiwan*
Yuan-Hao Chang - *Academia Sinica, Taipei, Taiwan*
Tei-Wei Kuo - *Academia Sinica and National Taiwan Univ., Taipei, Taiwan*

74.4 FlexLevel: a Novel NAND Flash Storage System Design for LDPC Latency Reduction (4:45)
Jie Guo, Wujie Wen - *Univ. of Pittsburgh, PA*
Jingtong Hu - *Oklahoma State Univ., Stillwater, OK*
Danghui Wang - *Northwestern Polytechnical Univ., Xi'an, China*
Hai Li, Yiran Chen - *Univ. of Pittsburgh, PA*

74.5 Approximate Storage for Energy Efficient Spintronic Memories (5:00)
Ashish Ranjan - *Purdue Univ., West Lafayette, IN*
Swagath Venkataramani - *Purdue Univ., West Lafayette, IN*
Xuanyao Fong, Kaushik Roy, Anand Raghunathan - *Purdue Univ., West Lafayette, IN*

74.6 A Synthesis Methodology for Application-Specific Logic-in-Memory Designs (5:15)
H. Ekin Sumbul, Kaushik Vaidyanathan, Qiuling Zhu, Franz Franchetti, Larry Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

Q & A Poster Session
5:30 - 6:00pm - Esplanade Foyer

75 - SPECIAL SESSION: DESIGN FOR MANUFACTURABILITY FOR SUB-10NM TECHNOLOGIES: CHALLENGES AND SOLUTIONS

Time: 4:00 - 5:30pm || Room: 310 || Track: EDA || Topic Area: Design for Manufacturability

CHAIR:
Luigi Capodieci - *GLOBALFOUNDRIES, Milpitas, CA*
ORGANIZERS:
Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
David Z. Pan - *Univ. of Texas at Austin, TX*

As process nodes continue to shrink to 10nm and below, the semiconductor industry faces severe manufacturing challenges with conventional optical and next-generation lithography technologies. Four most expected patterning technologies may push the limits of lithography: multiple patterning lithography (MPL), extreme ultraviolet lithography (EUVL), electron beam lithography (EBL), and directed self-assembly (DSA). Each of which, however, encounters different design difficulties and requires solutions for breakthroughs. We investigate critical design challenges of these technologies and provide solutions to handle them. Specifically, we explore the layout decomposition and design problems in MPL, flare and shadowing effects in EUV, the accumulated heating problem and proximity and fogging effects in EBL, the layout optimization and verification for DSA, and the combination of MPL with EUV, e-beam, and DSA to provide hybrid solutions for cost-effective patterning.

These technologies not only can enhance process manufacturability, but can also contribute to the continued scaling of the CMOS technology.

75.1 Pushing Multiple Patterning in Sub-10nm: Are We Ready? (4:00)
David Z. Pan - *Univ. of Texas at Austin, TX*
Lars Liebmann - *IBM Research - East Fishkill, NY*
Bei Yu, Xiaoqing Xu, Yibo Lin - *Univ. of Texas at Austin, TX*

75.2 EUV and E-Beam Manufacturability: Challenges and Solutions (4:30)
Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
R.G. Liu - *Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan*
Shao-Yun Fang - *National Taiwan Univ. of Science and Technology, Taipei, Taiwan*

75.3 Layout Optimization and Template Pattern Verification for DSA (5:00)
Martin D. F. Wong - *Univ. of Illinois at Urbana-Champaign, IL*
H.-S. Philip Wong - *Stanford Univ., Stanford, CA*
Zigang Xiao - *Univ. of Illinois at Urbana-Champaign, IL*
He Yi - *Stanford Univ., Stanford, CA*
Daifeng Guo - *Univ. of Illinois at Urbana-Champaign, IL*
Maryann Tung - *Stanford Univ., Stanford, CA*

TRACK 1, PART I - SYSTEMVERILOG VERIFICATION: HARDCORE SYSTEMVERILOG FOR CLASS-BASED VERIFICATION

Time: 10:15am - 1:15pm || Room: 220 || Track: EDA || Topic Area: Test and Verification

This session will teach the hardcore object-oriented programming constructs of SystemVerilog as used by methodologies such as UVM (note: understanding Class-Based SystemVerilog is an essential prerequisite to learning UVM). This session is aimed at engineers who have already had some exposure to the SystemVerilog language but are less familiar with object-oriented programming and constrained random verification, and will be a great preparation for the afternoon session on UVM.

Topics to be taught include classes, objects and inheritance, virtual interfaces, functional coverage, randomization and constraints, and more particularly how to use these language features to build a constrained random verification environment that includes a component hierarchy and transaction-level communication.

This track is taught by Doulos CTO John Aynsley, winner of the Accellera Systems Initiative 2012 Technical Excellence Award for his contribution to the development of language standards.

SPEAKER:
John Aynsley - *Doulos, Ringwood, United Kingdom*

TRACK 2, PART I - SYSTEMVERILOG DESIGN: SYNTHESIS-FRIENDLY SYSTEMVERILOG

Time: 10:15am - 1:15pm || Room: 232-234 || Track: EDA || Topic Area: Synthesis and FPGAs

Over the past few years SystemVerilog has risen to become the dominant language for constrained random hardware verification, but at the same time SystemVerilog has a lot to offer the hardware designer. SystemVerilog includes a number of significant improvements over Verilog which can be exploited by hardware designers to make their code more concise and readable.

This session will teach you how to use the SystemVerilog language for hardware design by focusing on the parts of the SystemVerilog language that are widely supported by commercial RTL synthesis tools.

This session is aimed at engineers who are currently using Verilog or VHDL for RTL design, and who want to start taking advantage of the power of SystemVerilog to better express their hardware design intent.

This track is taught by Doug Perry, Doulos Senior Member, Technical Staff.

SPEAKER:
Doug Perry - *Doulos, San Jose, CA*

TRACK 3, PART I - ESL AND SYSTEMC - THE DEFINITIVE GUIDE TO SYSTEMC: THE SYSTEMC LANGUAGE

Time: 10:15am - 1:15pm || Room: 236-238 || Track: EDA || Topic Area: Test and Verification

SystemC has become well-established as the language of choice for system modeling and virtual platform creation and integration, and is now being applied successfully for high level synthesis. SystemC models also frequently appear as reference models in the hardware verification flow.

This session will provide a solid introduction to the fundamental elements of the SystemC class library, aimed at hands-on hardware or software engineers who might know Verilog or C but have no previous experience of SystemC. This session will also present an overview of how SystemC is being used today in the contexts of system modeling, hardware synthesis, and hardware verification.

This track is taught by David C. Black, Doulos Senior Member, Technical Staff, who is co-author of the book, "SystemC: From the Ground Up."

SPEAKER:
David C. Black - *Doulos, Austin, TX*

TRACK 1, PART II - SYSTEMVERILOG VERIFICATION: EASIER UVM

Time: 2:15 - 5:15pm || Room: 220 || Track: EDA || Topic Area: Test and Verification

This session will get you started with UVM, the Universal Verification Methodology for SystemVerilog. UVM is an Accellera standard SystemVerilog class library that enables verification code reuse and encourages best practice when building constrained random verification environments.

This session will take a very practical approach to UVM, teaching some of the most common and important features of UVM by presenting a series of fully detailed code examples. It will introduce attendees the Easier™ UVM Coding Guidelines and Code Generator to speed the learning ramp.

The session is aimed at hands-on engineers who want to start writing UVM code themselves and are looking for some specific advice on the best place to start, the right UVM features and coding idiom to use, and the pitfalls to avoid.

This track is taught by Doulos CTO John Aynsley, winner of the Accellera Systems Initiative 2012 Technical Excellence Award for his contribution to the development of language standards.

SPEAKER:
John Aynsley - *Doulos, Ringwood, United Kingdom*

TRACK 2, PART II - BEYOND THE GUI: USING TCL TO ENHANCE YOUR EDA EXPERIENCE

Time: 2:15 - 5:15pm || Room: 232-234 || Track: EDA || Topic Area: General Interest

Tcl is a popular and widely used cross-platform script programming language that achieves significant productivity gains when used by skilled engineers. Its combination of text processing, file manipulation and system control features make it ideal for this purpose. Almost every industry-leading EDA tool uses it to provide a powerful and platform-independent command language. The session presents specific examples of the use of Tcl in an EDA context.

The course covers an introduction to the essential subset of the Tcl scripting language. Whenever you use the command-line prompt in EDA tools you are probably issuing commands to Tcl. Fully integrated with the EDA tool, Tcl deals with your commands, decides which internal functions of the tool to execute, and passes your command-line arguments to those functions.

This track is taught by Doug Perry, Doulos Senior Member, Technical Staff.

SPEAKER:
Doug Perry - *Doulos, San Jose, CA*

TRACK 3, PART II - ESL AND SYSTEMC - THE DEFINITIVE GUIDE TO SYSTEMC: TLM-2.0 AND THE IEEE 1666-2011 STANDARD

Time: 2:15 - 5:15pm || Room: 236-238 || Track: EDA || Topic Area: Test and Verification

The TLM-2.0 standard has become important in any context that requires communication between transaction-level models, such as within virtual platforms or hardware verification environments. The latest revision of the SystemC standard, IEEE 1666-2011, incorporates the whole of the TLM-2.0 standard as well as adding several significant new features to SystemC.

This session will provide an overview of the TLM-2.0 standard and will explain its significance for anyone interested in transaction-level modeling. This session will also teach some of the new features introduced into SystemC, such as the ability to suspend and resume processes, and to create vectors of SystemC objects.

This track is taught by David C. Black, Doulos Senior Member, Technical Staff, who is co-author of the book, “SystemC: From the Ground Up.”

SPEAKER:
David C. Black - *Doulos, Austin, TX*

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Have fun and meet people as you make your way towards becoming one of this year's big winners! This year's prizes include a new Apple Watch, Beats Solo Headphones, Bose Mini Bluetooth Speaker, and more! See page 121 for more information.

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COLOCATED CONFERENCES

ACM/IEEE SYSTEM LEVEL INTERCONNECT PREDICTION (SLIP)

Saturday, June 6 || Time: 8:00am - 5:00pm || Room: 300
Track: EDA || Topic Area: System-on-Chip Design

ORGANIZERS:
Rasit Topaloglu - *IBM Corp., Fishkill, NY*
Baris Taskin - *Drexel Univ., Philadelphia, PA*

The general technical scope of the workshop is the design, analysis, prediction, and optimization of interconnect and communication fabrics in electronic systems. The contributions include papers, tutorials, panels, special sessions, and posters.

Technical topics include but are not limited to:
1. Interconnect prediction and optimization at various IC and system design stages
2. System-level design for FPGAs, NOCs and reconfigurable systems
3. Design, analysis, and optimization of power and clock networks
4. Interconnect reliability
5. Interconnect topologies and fabrics of multi- and many-core architectures
6. Design-for-manufacturing (DFM) and yield techniques for interconnects
7. High speed chip-to-chip interconnect design
8. Design and analysis of chip-package interfaces
9. Power consumption of interconnects
10. 3D interconnect design and prediction
11. Emerging interconnect technologies
12. Applications of interconnects to social, genetic, and biological systems
13. Co-optimization of interconnect technology and chip design

The workshop includes keynotes, regular paper sessions, interactive panels, tutorials, invited talks, and interactive poster sessions. Our program also includes lunch, refreshments, and a traditional social dinner with fun elements.

PANELISTS:
Mircea Stan - *Univ. of Virginia, Charlottesville, VA*
Wei-Kai Shih - *Intel Corp., Portland, OR*

SPEAKERS:
Umit Ogras - *Arizona State Univ., Tempe, AZ*
Tsung-Yi Ho - *National Cheng Kung Univ., Tainan, Taiwan*
Joseph Zambreno - *Iowa State Univ., Ames, IA*
Cheng Zhuo - *Intel Corp., Portland, OR*

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EMBEDDED TECHCON

Monday, June 8 - Wednesday, June 10: 9:00am - 5:30pm || Room: 307 & 308
Track: Embedded Systems || Topic Area: Embedded System Architecture and Design

ORGANIZER:
Monique DeVoe - *OpenSystems Media, LLC, Fountain Hills, AZ*

Embedded TechCon is designed to educate today's design engineers in the most critical embedded product and technologies. The classes, which will be taught by leading industry experts, will cover key embedded topics like IoT, automotive, and security, while drawing from the industry's roots with topics like firmware development, debugging, and open-source hardware and software.

Confirmed classes:

- The Intel IoT Platform, taught by Kevin Williams, Solutions Architect, and Victor Webb, Solutions Architect, Intel
- How to secure the Industrial Internet of Things, taught by Alan Grau, President/Co-founder, Icon Labs
- Rethinking embedded Linux, taught by Bill Gatliff, expert consultant
- Hands-On Lab: Use Bluetooth Smart to control your embedded device with a mobile device, taught by Vijay Parmar, Business Development Manager, Connectivity Group, Anaren (Note: the first 50 registered attendees will receive an Anaren Bluetooth Smart development kit, A20737A-MSDK1)
- Panel Session: Identify and secure your IoT weak links, moderated by Patrick Mannion.
  Panelists include:
  - David Kleidermacher, Senior Vice President, Head of Product Security, Blackberry
  - Skip Ashton, VP of Software Engineering, Silicon Laboratories
  - Dr. Jakob Engblom, Product Line Manager, Wind River
  - Eran Briman, VP of Marketing, CEVA
  - Additional panelists to be announced
- Understanding and dealing with security in the automotive sector, taught by David Kleidermacher, Chief Security Officer, Blackberry
- Hands-on Lab: Bring up an RTOS, taught by Jean Labrosse, CEO, Micrium (Note: the first 50 registered attendees will receive a free Renesas evaluation board and a one-month free access to the uC/Probe visual tool)
- Making continuous integration a reality using simulation, taught by Dr. Jakob Engblom, Product Line Manager, Wind River Systems
- Build vs. buy when it comes to IoT platforms, taught by Stefan Milnor, Technical Fellow, Kontron
- Best practices for efficient and effective FPGA design, taught by RC Cofer, Field Applications Engineer, Avnet
- Synchronizing mechatronic systems in real-time using FPGAs and Industrial Ethernet, taught by Sari Germanos, Ethernet Powerlink Standardization Group
- Connecting your IoT devices to the infrastructure, taught by Philippe Chevalier, Director, Technology Platforms, Kontron
- Finding low-level security vulnerabilities with static analysis, taught by Paul Anderson, VP of Engineering, GrammaTech
- Making sense of sensors for IoT applications, taught by Prem Kumar, VP, Technology Platforms, Kontron
- How to keep your IoT platform secure, taught by Eric Sivertson, EVP, Head of Avionics, Trans., and Defense BU, Kontron
- Remote management, configuration, and diagnostics of embedded systems and devices, taught by Matthias Huber, Vice President, ADLINK
- A survey of performance, memory, and power optimization techniques for embedded system software, taught by Rob Oshana, Director, Global Software R&D and Enablement, Digital Networking, Freescale Semiconductor
- Developing IPs and subsystems for automotive infotainment and ADAS applications, taught by Charles Qi, System Solutions Architect, Cadence
- The era of machines that see: Opportunities and challenges in embedded vision, taught by Jeff Bier, President, BDTI
- How (and why) to make the IoT trusted, presented by The Trusted Computing Group, taught by Stefan Thom, Sr. Security Architect/Software Development Engineer, Microsoft
- Hands-On Lab: Getting started with a Cortex-M3 board, taught by Steven Guan, Applications Engineer, and Joe Hale, Senior Software Engineer, NXP Semiconductor (Note: the first 50 registered attendees will receive an LPCXpresso1549 development board)

Embedded TechCon, produced by OpenSystems Media, is chaired by Rich Nass, OSM's Executive Vice President. Nass will coordinate three days of technical, hands-on, practical educational sessions. Nass has extensive experience in developing technical conferences for the benefit of embedded developers, having served as the Conference Chairman of the Embedded Systems Conference during its most successful years.

SPEAKERS:
Alan Grau - *Icon Labs, West Des Moines, IA*
Bill Gatliff - *Gatliff Consulting, Peoria, IL*
Vijay Parmar - *Anaren, East Syracuse, NY*
Patrick Mannion - *ClariTek, LLC, Commack, NY*
Skip Ashton - *Silicon Laboratories, Inc., Austin, TX*
David Kleidermacher - *BlackBerry, Santa Barbara, CA*
Jean Labrosse - *Micrium, Inc., Fort Lauderdale, FL*
Dr. Jakob Engblom - *Wind River Systems, Inc., Alameda, CA*
Philippe Chevalier, Stefan Milnor - *Kontron AG, Fremont, CA*
RC Cofer - *Avnet, Inc., Melbourne, FL*
Sari Germanos - *EPSG, Roswell, GA*
Paul Anderson - *GrammaTech, Inc., Ithica, NY*
Prem Kumar, Eric Sivertson - *Kontron AG, Poway, CA*
Matthias Huber - *ADLINK Technology Inc., San Jose, CA*
Rob Oshana - *Freescale Semiconductor, Inc., Austin, TX*
Jeff Bier - *Berkeley Design Technology, Inc., Walnut Creek, CA*
Gary Davis - *McAfee, Inc., Santa Clara, CA*
Charles Qi - *Cadence Design Systems, Inc., San Jose, CA*
Kevin Williams, Victor Webb - *Intel Corp., Chandler, AZ*
Stefan Thom - *Microsoft Corporation, Redmond, WA*
Steven Guan - *NXP Semiconductors, San Jose, CA*
Joe Hale - *NXP Semiconductors, Cambridge, United Kingdom*
Eran Briman - *CEVA Logistics, Herzelia, Israel*

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DESIGN AUTOMATION (DA) PERSPECTIVE CHALLENGE

Sponsored by: CEDA IEEE Council on Electronic Design Automation

Monday, June 8: 7:00 - 8:00pm || Room: 300
Track: EDA || Topic Area: General Interest

Electronic Design Automation (EDA) has had a profound impact on the development of modern computing and information technology which in turn has transformed our lives and society. Over the past 5 decades, the vision and efforts of the EDA community have been primarily focused on supporting the successful scaling of the Moore's law. Despite its dominant focus on electronics, EDA is one of the first fields in engineering that has taken a truly interdisciplinary route: several abstractions, computational models, algorithms, methodologies, and tools have been jointly developed by the chemists, device physicists, electrical engineers, computer scientists, applied math, and optimization experts.

Not only are the EDA tools able to take the high level functional description and automatically synthesize and optimize it to a physical entity, but also they can perform the complex tasks of simulation and verification. The growth in traditional EDA industry and development is however, limited due to the physical limits of manufacturing technology and the field's maturity.

The Design Automation (DA) Perspective Challenge aims to seek visionary proposals describing key long-term research problems in DA of emerging domains that can benefit and further evolve the practices and methodologies developed by the EDA researchers and industry over the past few decades.

The perspective proposals shall indicate the challenges in addressing the suggested long-term problems and how addressing the problems could potentially lead to a big scientific or industrial impact. The committee will carefully review the proposals; The proposals with long-term prospects will be included in the DA Challenge Archive on IEEE CEDA web-portal.

A limited set of proposals will be selected for presentation at the competition event, to take place in San Francisco at the Moscone Center on June 8 at 7pm. The program committee will rank the competing teams and award the 3 best submissions. The submitted perspective proposals shall address the following questions:
What is the long-term problem?
Why is the problem important and challenging?
What is the state-of-the-art?
What is the problem's relevance to the existing Design Automation (DA) tools and methods? Or, how could Design Automation (DA) help in addressing the challenge(s)?
What knowledge, skills, and/or tools are needed for addressing the challenge(s)?

Is the problem inter-disciplinary. i.e., requires expertise in both DA and in other domain(s)?What are the broader impacts?

IBM ANNUAL HPC SEMINAR AND LSF TECHNICAL WORKSHOP

Wednesday, June 10: 10:30am - 6:00pm || Room: 236-238 || Track: EDA || Topic Area: Business

ORGANIZERS:
Peter Basmajian - *IBM Corp., Foster City, CA*
Meghan Smith - *IBM Corp., Austin, TX*

Learn new ways to accelerate time to results with IBM Platform Computing, software-defined storage and HPC cloud. High performance computing (HPC) technologies are evolving in exciting new ways. Businesses that can harness these advancements in resource and cluster management, workload scheduling, software-defined storage and cloud computing can gain competitive advantage as never before possible.

IBM invites the following IT and technical professionals to our annual conference in Silicon Valley:

- IT Directors and Managers
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- Auto/Aero and Petroleum Engineers
- Structural and Software Engineers
- CAD/CAE and EDA Engineers Academic Researchers

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- How to design and bring products to market faster using advanced HPC software technologies
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- Get the most out of your IT investment

Managing today's compute-intensive workloads can be challenging. You need to run more simulations, iterations and analytics to accelerate your time to market, extract insight, and make better decisions faster. From compute infrastructure to software licenses, IBM Platform Computing can help you get the most out of your IT investment by optimizing and managing your organization's resources. Not only that, we can also help you identify the right cloud model to quickly and economically add computing and storage capacity.

The Technical Workshop will include a deep dive into the features and functionality of the most recent release of Platform LSF, version 9.1.3, including support of Hadoop MapReduce. In addition, IBM developers and product managers will discuss the IBM Platform Computing product strategy, roadmaps and ways to deploy our solutions in the cloud.

Please join us for this valuable networking opportunity with our leading experts.

SPEAKERS:
Louise Westoby - *IBM Corp., San Jose, CA*
Peter Basmajian - *IBM Corp., Foster City, CA*

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CELUG/EDAC ENTERPRISE LICENSING CONFERENCE

Wednesday, June 10 - Thursday, June 11: 9:00am - 5:00pm || Room: 309
Track: EDA || Topic Area: General Interest

ORGANIZER:

Derek Magill - *Qualcomm, Inc., Austin, TX*

EDA Licensing providers, ISVs, and Enterprise Customers will come together at an event colocated with the 52nd ACM/EDAC/IEEE Design Automation Conference (DAC), June 8 - 12, 2015, at the Moscone Center in San Francisco, CA.

CELUG (Centralized Enterprise Licensing Users Group) and EDAC (EDA Consortium) are co-hosting this three-day event colocated at DAC 2015. This interactive event will focus on Enterprise Licensing, with presentations and panels addressing current and future challenges to making high technology tools and users more productive. This colocated event will bring Licensing Solution Providers and Independent Software Vendors together with Enterprise Customers from key industries for interactive, face-to-face meetings.

Planned Agenda Overview

Tuesday, June 9

Complimentary access to the DAC Exhibits, Pavilion Theater, and DAC Keynote presentations.

Wednesday, June 10

Enterprise Licensing Presentations:

- CELUG Member Priorities Survey/CELUG Roadmap and Vision
  - Derek Magill - *CELUG Chair*
- FlexNet Publisher Roadmap
  Tu Le - *Product Manager, FlexNet Publisher, Flexera Software LLC*
- FNMEA Roadmap
  Daniel Galecki - *Product Manager, FlexNet Manager for Engineering Applications, Flexera Software LLC*
- EDA Platform/OS Roadmap
  Richard Paw - EDAC/Synopsys Inc.
- Accelerating Innovation: EDA Scalability, Security and Governance in the Cloud
  David Pellerin - Amazon Web Services, Inc.
- High Availability
  Bob Van der Kloot - Teradyne Inc.
- EDAC License Management and Antipiracy Report/HostID Duplication
  John Harms - EDAC/Mentor Graphics Corp.
- High Availability Without HostID Duplication
  Breakout Session - All Conference Participants

Thursday, June 11

Enterprise Licensing Presentations (Continued):

- SCL Roadmap
  Rajendra Kundapur - Synopsys, Inc.
- Cadence Licensing Roadmap
  Sashi Subramanian - Cadence Design Systems, Inc.
- Mentor Licensing Roadmap
  Bela Kirchberger - Mentor Graphics Corp.
- ANSYS Licensing Roadmap
  Julie Lesko/Steve Del - ANSYS, Inc.
- Mathwork's Licensing Roadmap
  Eric Raffi - The Mathworks, Inc.
- Member Presentation
  Joshua Jauta - Qualcomm Technologies, Inc.
- Open Member Presentation Slot
  Rachel Stanley - Honeywell International Inc.
- Members Only Wrap-Up/Discussion
  CELUG Members - CELUG

SPEAKER:
Derek Magill - *Qualcomm, Inc., Austin, TX*

CELUG Centralized Enterprise Licensing User Group

EDA CONSORTIUM

ELECTRONIC SYSTEM LEVEL SYNTHESIS CONFERENCE (ESLSYN)

Wednesday, June 10: 12:00 - 6:00pm || Thursday, June 11: 9:00am - 5:00pm
Room: 206 || Track: Embedded Systems || Topic Area: Synthesis and FPGAs

ORGANIZER:
Adam Morawiec - *ECSI, Belmont, France*

The ever-increasing need for enhanced productivity in designing highly complex electronic systems drives the evolution of design methods beyond traditional approaches. Virtual prototyping, design space exploration and system synthesis are needed to design optimized systems, comprising hardware and software implementations.

Electronic system-level (ESL) design promises to provide system architects with the right tools to make the right decisions about the system architecture at early stages of the design process. This includes methodologies and synthesis techniques that are supported by appropriate ESL models. Furthermore, a well-connected ESL-to-implementation design flow is needed. Overall, designing at higher levels of abstraction coupled with the right tool support is a viable way to better cope with the system design complexity, by increasing code reuse and allowing components to be verified earlier in the design process.

The Electronic System Level Synthesis Conference (ESLsyn) focuses on automated system design methods that enable efficient modelling, synthesis, exploration and verification of systems from high-level specifications down to lower level implementations.

Topics that ESLsyn will focus on are the five key tasks related to the design and verification of complex, programmable electronic products:

- The development of product architectures and specifications, including the incorporation and configuration of IP
- The mapping of applications onto a product platform, including hardware/software partitioning and processor optimization (High-Level Synthesis)
- The creation of pre-silicon, virtual hardware platforms for software development
- The automated synthesis of hardware and software implementations for a given architecture
- The development of formal methods for verifying hardware and software

Within this scope, ESLsyn addresses:

- Cyber-Physical and Embedded Systems/Platforms related to ESL design flows
- High-Level/Behavioral/Architectural Synthesis for hardware design in cooperation with ESL design flows
- Embedded Hardware and Software Synthesis that is used as part of ESL design flows

SPEAKERS:
Forrest Brewer - *Univ. of California, Santa Barbara, CA*
Kazutoshi Wakabayashi - *NEC Corp., Tokyo, Japan*

GENERAL CHAIR:
Jörn Janneck - *Lund Univ., Sweden*

CO-CHAIR:
Achim Rettberg - *HELLA KGaA Hueck & Co., Paderborn, Germany*

INDUSTRIAL CHAIR:
Andres Takach - *Calypto Design Systems, Inc., Wilsonville, OR*

PROGRAM CHAIR:
Zhiru Zhang - *Cornell Univ., NY, USA*

IWLS - INTERNATIONAL WORKSHOP ON LOGIC AND SYNTHESIS

Friday, June 12 - Saturday, June 13: 8:00am - 9:00pm
Room: Computer History Museum — Mountain View, CA
Track: EDA || Topic Area: Synthesis and FPGAs

ORGANIZER:
Andre Reis - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*

The International Workshop on Logic and Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits and systems. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged.

The workshop encourages early dissemination of ideas and results. The workshop accepts complete papers highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor.

Topics of interest include, but are not limited to: hardware synthesis and optimization; software synthesis; hardware/software co-synthesis; power and timing analysis; testing, validation and verification; synthesis for reconfigurable architectures; hardware compilation for domain-specific languages; design experiences.

Submissions on modeling, analysis and synthesis for emerging technologies and platforms are particularly encouraged. The workshop format includes paper presentations, posters, invited talks, social lunch and dinner gatherings, and recreational activities. Accepted papers are distributed exclusively to IWLS participants.

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ADDITIONAL MEETINGS

NEWTON YOUNG FELLOW PROGRAM WELCOME BREAKFAST & ORIENTATION

Sunday, June 7: 7:30 - 9:00am || Room: 307 || Track: EDA || Topic Area: General Interest

The Newton Young Fellow Program is designed to assist young students at the beginning of a career in Electronic Design Automation and Embedded Systems. Each Newton Young Fellow will actively engage in DAC through a number of events including meetings with design automation luminaries, attendance at technical sessions and exhibits, participation in student-related events at DAC.

In addition, Newton Young Fellows will participate in a welcome orientation breakfast on Sunday morning, attend the Design Automation Summer School program, present posters of their academic/research work on Tuesday evening (colocated with the SIGDA Ph.D. Forum), and participate in a closing award ceremony for Young Fellows on Thursday evening.

Following a 50-year tradition, DAC strives to foster a vibrant and worldwide community of electronic design and embedded systems professionals; the fellowship actively supports and attempts to build an active cohort of the next generation of EDA and Embedded Systems professionals.

Welcome Breakfast and Orientation
Sunday, June 7
7:30 - 8:30am
Room: 307

Poster Presentation (colocated with the Ph.D. Forum)
Tuesday, June 9
7:00 - 8:30pm
Room: 306

Closing Session and Award Ceremony
Thursday, June 11
6:00 - 7:00pm
Room: 300

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DESIGN AUTOMATION SUMMER SCHOOL (DASS)

Sunday, June 7: 9:00am - 6:00pm || Room: 307 || Track: EDA || Topic Area: General Interest

The Design Automation Summer School (DASS) is a one-day intensive course on research and development in design automation (DA). Each topic in this course will be covered by a distinguished speaker who will define the topic, describe recent accomplishments, and indicate remaining challenges. This program is intended to introduce and outline emerging challenges, and to foster creative thinking in the next generation of EDA engineers.

The 2015 SIGDA Design Automation Summer School is co-hosted by A. Richard Newton Young Fellowship Program at DAC.
All the students receiving the fellowship (excluding the mentors) are required to attend DASS event.

GARY SMITH EDA AT EDAC KICKOFF SUNDAY NIGHT

Sunday, June 07, 5:00pm - 5:30pm || Intercontinental Hotel - Grand Ballroom A
Track: EDA || Topic Area: General Interest

Gary kicks off the annual EDAC reception.

Come hear the 26th annual update on the state of EDA by Gary.

How Connected Systems Are Impacting EDA
Gary Smith

This year's talk will focus on how the challenges facing EDA vendors. How is the Connected Systems market impacting the growth path of the major EDA players? How can EDA vendors prepare for the changes? The annual EDA forecast also will be shared.

DAC reception immediately follows.

SPEAKER:
Gary Smith - *Gary Smith EDA, Santa Clara, CA*

Benefits of EDAC Membership

The EDA Consortium provides a proven forum to network and learn from other members in the broad EDA and IP Communities.

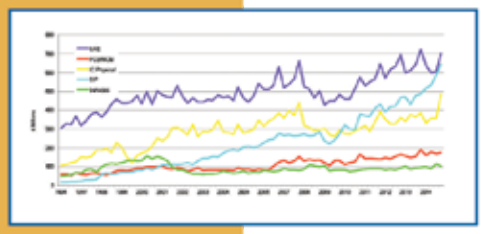
EDAC MEMBERS 10% DAC BOOTH DISCOUNT

License Management and Anti-Piracy (LMA):

Stay abreast of current license management and anti-piracy issues and best practices

Interoperability:

Participate in the EDA industry OS roadmap – minimize your costs in supporting multiple operating systems



Market Statistics Service (MSS):

Get industry insight with accurate and timely quarterly EDA market numbers.

Emerging Companies:

Learn and network with knowledgeable industry leaders at informative seminars.

Export Compliance:

Understand the complex and changing export compliance issues.

DAC Management Day Export Seminar
Tuesday Afternoon, Room 309

Join EDAC! For more information about the benefits of membership, visit edac.org or call (408) 287-EDAC

EDA CONSORTIUM

SYNOPSYS BREAKFAST: TSMC, ARM AND SYNOPSYS COLLABORATE TO ENABLE DESIGN WITH 16NM AND 10NM FINFET TECHNOLOGY

Monday, June 8: 7:30 - 8:45am || Room: Park Central Hotel San Francisco
Track: EDA || Topic Area: System-on-Chip Design

Attend this breakfast panel to learn how TSMC, ARM and Synopsys are working together to optimize ARM-based designs on TSMC's latest process technology.

Visit www.synopsys.com for more information and to register.

ADVANCING PERFORMANCE TO ACCELERATE CIRCUIT SIMULATION FOR COMPLEX IC DESIGNS

Monday, June 8: 10:30am - 1:30pm || Room: Park Central Hotel San Francisco
Track: EDA || Topic Area: Test and Verification

The increasing complexity of mixed-signal SoCs and post-layout simulation for advanced-node designs requires significant improvements in circuit simulation performance. Join us for this AMS circuit simulation luncheon event to hear how industry leaders use the latest advancements in Synopsys' circuit simulation solution to tackle tough circuit simulation challenges for designs ranging from FinFET SRAM to automotive/industry ICs.

WINNING THE CUSTOM IC DESIGN RACE AT NANOMETER & LOW POWER PROCESSES

Monday, June 8: 10:30 - 11:30am || Room: 310 || Track: EDA || Topic Area: Analog Circuits

Opening by Amit Gupta (CEO, Solido) on custom IC design market data.

Companies must carefully navigate the tradeoff between reducing underdesign to improve yield, and reducing overdesign to improve power, performance and area. Designers on this panel will share techniques to accelerate high performance, low power custom IC design, while reducing risk of re-spins due to increased variation at nanometer and low power process nodes.

With nearly 4 in 10 companies planning to implement or evaluate variation tools in 2015, topics will include variation analysis technologies and techniques. Memory, standard cell, custom digital and analog/RF design applications will be discussed.

PANELISTS:
Sifuei Ku - *Microsemi Corp., Irvine, CA*
Dragomir Nikolic - *Cypress Semiconductor Corp., Lexington, KY*
Jeff Dyck - *Solido Design Automation, Inc., Saskatoon, SK, Canada*
Alfred Yeung - *Applied Micro Circuits Corp., Sunnyvale, CA*

ACCELERATING SOCS TO MARKET WITH THE POWER OF 10X

Monday, June 8: 11:30am - 1:30pm || Room: Park Central Hotel San Francisco
Track: EDA || Topic Area: Physical Design

In its first year since introduction, IC Compiler II has proven to be a game-changer in physical design, accelerating silicon success for designers of the world's most advanced ICs.

Join us for this luncheon event where industry leaders discuss how 10X faster throughput has transformed the way they think about product development, opening up a world of new opportunities.

HOW TO MAKE NEXT-GENERATION VERIFICATION SMARTER

Monday, June 8: 12:00 - 1:30pm || Room: 104 || Track: EDA || Topic Area: Test and Verification

Experts seem to agree that traditional, block-oriented dynamic verification techniques no longer scale to the next level of challenges. What's next from here? This panel will discuss the key technologies needed to address the next level of verification challenges. What role will hardware-assisted development play in the context of other verification engines?

How can verification become smarter? Will the next level of abstraction save the day and move verification to the transaction level? What changes when verification extends from the block and sub-system level to the SoC and system level? How will system-level scenarios be captured and applied to verification?
For more information, visit:
http://www.cadence.com/dac2015/Pages/luncheons.aspx.

THE NEXT WAVE OF DESIGN & IP MANAGEMENT

Monday, June 8: 1:30 - 2:30pm || Room: 310 || Track: EDA || Topic Area: General Interest

MODERATOR:
Dean Drako - *IC Manage, Inc., Campbell, CA*

Speakers will reveal the next wave in Design & IP Management. Keep up with the latest market data, technology advances, and users methodologies. Includes audience Q&A.

SPEAKERS:
Shiv Sikand - *IC Manage, Inc., Campbell, CA*
Simon Burke - *Xilinx, Inc., San Jose, CA*

COOLEY'S DAC TROUBLEMAKER PANEL

Monday, June 8: 3:00 - 4:00pm || Room: 310 || Track: EDA || Topic Area: General Interest

MODERATOR:
John Cooley - *Deepchip, Holliston, MA*

Come watch the EDA troublemakers answer the edgy, user-submitted questions about this year's most controversial issues! It's an old style open Q&A from the days before corporate marketing took over every aspect of EDA company images.

PANELISTS:
Jim Hogan - *Vista Ventures, Los Gatos, CA*
Dean Drako - *IC Manage, Inc., Campbell, CA*
Sanjiv Kaul - *Calypto Design Systems, Inc., San Jose, CA*
Anirudh Devgan - *Cadence Design Systems, Inc., San Jose, CA*
Amit Gupta - *Solido Design Automation, Inc., San Jose, CA*
Joe Sawicki - *Mentor Graphics Corp., Wilsonville, OR*
Gary Smith - *Gary Smith EDA, Santa Clara, CA*

ANNUAL SI2 OPEN RECEPTION

Monday, June 8: 4:30 - 6:00pm || Room: 202/204/206 || Track: EDA || Topic Area: Business

Si2 is holding the Annual Si2 Open Reception at the Design Automation Conference, Monday, June 8, from 4:30 - 6pm. John Ellis, president and CEO of Si2, will introduce the newly-elected Board of Directors and will summarize Si2's activities and major changes.

Refreshments and hors d'oeuvres will be provided. This event is free of charge.

PRIMETIME SPECIAL INTEREST GROUP (SIG) DINNER - MAXIMIZE DESIGN PRODUCTIVITY WITH ADVANCED SIGNOFF TECHNOLOGIES

Monday, June 8: 7:00 - 8:30pm || Room: Park Central Hotel San Francisco
Track: EDA || Topic Area: System-on-Chip Design

Synopsys hosts an annual event for the PrimeTime Special Interest Group at DAC, providing an opportunity for users to stay connected with the latest developments in timing analysis.

We are pleased to host this PrimeTime SIG event at DAC 2015.

SYNOPSYS BREAKFAST: SAMSUNG, ARM AND SYNOPSYS COLLABORATE TO ENABLE NETWORK COMPUTING DESIGN WITH 14NM LPP FINFET

Tuesday, June 9: 7:30 - 8:45am || Room: Park Central Hotel San Francisco
Track: EDA || Topic Area: System-on-Chip Design

Attend this breakfast panel to learn how Samsung, ARM and Synopsys are utilizing Samsung's 14nm LPP technology to meet the added functionality needs of network computing ARM-based SoC designs.

Visit www.synopsys.com for more details about the event and to register.

ACCELLERA BREAKFAST AND PANEL DISCUSSION

Tuesday, June 09, 7:30am - 9:00am | Room 220 || Track: EDA || Topic Area: General Interest

Design and Verification Standards in the Era of IoT

The era of Internet of Things (IoT) will usher increased use of communication and other protocols for rapid development and interconnect of new devices. These projects will be run on shrinking timelines with more globalized teams, increasing the need for design and verification standards. I2C, MIPI, WiFi and other protocols are already implemented using SystemC, SystemVerilog, UPF, UVM and other standards originated by Accellera and globalized in the IEEE. By working more closely together, the protocol working groups and the design and verification working groups can provide key technology to accelerate development in the era of IoT.

The Accellera breakfast panel brings together senior technologists from the IoT community to discuss the current status and future needs for standards cooperation. We welcome you to join this lively discussion and get your creative minds running before you head into your IoT, automotive, and other sessions at DAC 2015.

This event is free to all DAC attendees. Registration is required.

CROSSING THE GREAT DIVIDE: HOW TO SAFELY NAVIGATE THE MOVE FROM 28NM TO 16FF+

Tuesday, June 9: 7:30 - 9:00am || Room: 104 || Track: EDA || Topic Area: System-on-Chip Design

What are the biggest challenges at 16nm? When do you make the decision to move from 28nm? How does the use of FinFETs change the design flow? What do designers need to learn about double patterning, tools, flows and process rules? How do you manage analog/mixed-signal design at 16nm?

Hear from SoC designers who crossed the great divide from 28nm to 16FF+ and emerged on the other side safely, seasoned and successful. And listen to design ecosystem experts' insights and guidance for crossing the divide smoothly.
For more information, visit:
http://www.cadence.com/dac2015/Pages/luncheons.aspx

AGILE IC METHODOLOGY FORUM

Tuesday, June 9: 10:30am - 12:00pm || Room: 306
Track: Silicon Design || Topic Area: System-on-Chip Design

ORGANIZER:
Randy Smith - *Sonics, Inc., Milpitas, CA*

The old waterfall design methodologies are breaking down. Come learn about Agile IC Methodology – What is it? How it relates to Agile software design? To Shift Left? Hear from designers who have actually used Agile methods in their production projects.

This forum will feature several presentations with plenty of opportunities for Q&A with each presenter. The two LinkedIn groups discussing this topics have more than 800 members combined – what are you missing? This is your chance to understand, and influence, the shape of future IC design methodologies.

ADOPTING SYNOPSYS CUSTOM DESIGN TOOLS TO SPEED ADVANCED-NODE LAYOUT

Tuesday, June 9: 11:30am - 1:30pm || Room: Park Central Hotel San Francisco
Track: Silicon Design || Topic Area: System-on-Chip Design

Because FinFET devices have added significant complexity to custom layout, many companies are seeking new solutions for custom design.

During this luncheon event, users will present their experiences meeting the challenges of FinFET custom design, and will discuss how they have deployed Synopsys' custom design tools to improve their custom design productivity.

SOC LEADERS VERIFY WITH SYNOPSYS

Tuesday, June 9: 11:30am - 1:30pm || Room: Park Central Hotel San Francisco
Track: EDA || Topic Area: Test and Verification

Synopsys will highlight next-generation verification technologies as well as discussions about the latest developments in the verification landscape and advanced technology trends.

In addition, a panel of industry experts will share their viewpoints on what is driving SoC complexity, how their teams have achieved success and how you can apply their insights on your next project.

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DESIGN, AUTOMATION AND TEST IN EUROPE

The european event for electronic system design & test

ICC, DRESDEN, GERMANY

DATE 2016 — CALL FOR PAPERS

Scope of the Event

The 19th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organization of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community. Special space will also be allocated for EU-funded projects to show their results. More details are given on the DATE website (www.date-conference.com).

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Topics of interest include, but are not restricted to:

- System Specification and Modeling
- System Design, Synthesis and Optimization
- Simulation and Validation
- Design of Low Power Systems
- Temperature-Aware Design
- Power Estimation and Optimization
- Temperature Modeling and Management
- Emerging Technologies, Systems and Applications
- Formal Methods and Verification
- Network on Chip
- Architectural and Microarchitectural Design
- Architectural and High-Level Synthesis
- Reconfigurable Computing
- Logic and Technology Dependent Synthesis for Deep-Submicron Circuits
- Physical Design and Verification
- Analogue and Mixed-Signal Circuits and Systems
- Interconnect, EMC, EMD and Packaging Modeling
- Multiprocessor System-on-Chip and Computing Systems
- Communication, Consumer and Multimedia Systems
- Transportation Systems
- Medical, Healthcare and Assistive Technology Systems
- Energy Generation, Recovery and Management Systems
- Secure, Dependable and Adaptive Systems
- Test for Defects, Variability, and Reliability
- Test Generation, Simulation and Diagnosis
- Test for Mixed-Signal, Analog, RF, MEMS
- Test Access, Design-for-Test, Test Compression, System Test
- On-Line Testing and Fault Tolerance
- Real-time, Networked and Dependable Systems
- Compilers and Code Generation for Embedded Systems; Software-centric System Design Exploration
- Model-based Design and Verification for Embedded Systems
- Embedded Software Architectures and Principles; Software for MPSoC, Multi/many-core and GPU-based Systems

Submission of Papers

All papers have to be submitted electronically by Sunday September 13, 2015 via: **www.date-conference.com**

Papers can be submitted either for standard oral presentation or for interactive presentation. **The Programme Committee also encourages proposals for Special Sessions, Tutorials, Friday Workshops, University Booth, PhD Forum and Exhibition Theatre.**

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CEDA DISTINGUISHED SPEAKER LUNCHEON: BACK TO THE FUTURE INTERNET OF THINGS

Sponsored by: CEDA IEEE Council on Electronic Design Automation

Tuesday, June 9: 12:00pm - 1:30pm || Room: 220
Track: EDA || Topic Area: General Interest

Back in 1999, we forecasted that in 15 years we would have connected essentially all the people on the planet, and have the technology to connect all the things. That future is here and busy being reinvented. In this talk we will look at key research contributions and interactions with the industrial ecosystem that brought us here.

We will explore synergies among embedded wireless networks, the maker movement, wearables, and phones that are likely to shape a new renaissance of research and innovation, as we interconnect people, the physical world, and our societal infrastructures.

SPEAKER:
David E. Culler - *Univ. of California, Berkeley, CA*

THE FUTURE OF DIGITAL IS HERE

Tuesday June 09, 12:00pm - 1:30pm | Room 104
Track: EDA || Topic Area: System-on-Chip Design

If you're designing SoCs for high-end applications, your success depends on getting the best performing, lowest power chip to market before your competitors. Yet, new design challenges have emerged as process nodes shrink. In this panel, Cadence will discuss an integrated digital implementation solution based on their RTL synthesis, digital implementation (Innovus™ Implementation System), and signoff (Tempus™, Voltus™, Quantus™ QRC) design tools and flows.

These tools help in implementing large, high-performance, advanced SoCs at 16/14/10nm FinFET processes and at established nodes. Also, customers will describe how they successfully leveraged the new Cadence digital design tools in their system designs.
For more information, visit:
http://www.cadence.com/dac2015/Pages/luncheons.aspx.

SYSTEM LEVEL POWER WORKSHOP: WHAT YOU NEED TO KNOW

Tuesday June 09, 1:15pm - 4:30pm | Room 206
Track: EDA || Topic Area: General Interest

Low power remains a hot topic for designers, verification engineers, IP developers and tool providers. In particular, interoperability among tools and IP remains a big concern for the engineers dealing with low power issues. In the past decade, standards have played an important role in building design and verification environment that address interoperability issues. Collectively, as the industry learns how to solve current issues, it uncovers that there are more issues to solve at system level in order to keep up with the growing complexity of designs and processes. Besides agreeing on the definition of system level, creation of power models and their suitability at different levels of abstraction for appropriate analysis remains a challenge.

With this in mind, a System Level Low Power workshop will be held at the 52nd Design Automation Conference (DAC). The workshop is co-organized and sponsored by the IEEE Design Automation Standards Committee (DASC), Si2 and Accellera Systems Initiative.

This workshop is free to all DAC attendees. Registration is required.

BIRDS-OF-A-FEATHER MEETINGS

Tuesday, June 9: 7:00pm - 8:30pm || Room: Various
Track: EDA || Topic Area: General Interest

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal, non-commercial meetings, held after hours, are referred to as "Birds-Of-A-Feather" (BOF).

All BOF meetings are held at the Moscone Center, Tuesday, June 9 from 7:00 - 8:30pm.

To arrange a BOF Meeting, please contact Lisa Roby at lisa@dac.com.

BOF MEETING - OSVVM - OPEN SOURCE VHDL VERIFICATION METHODOLOGY

Tuesday, June 9: 7:00 - 8:30pm || Room: 300 || Track: EDA || Topic Area: Test and Verification

User community meeting for Open Source VHDL Verification Methodology (OSVVM).

It will provide the opportunity for learning more and discussing future directions of OSVVM.

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Visit us at http://ieee-ceda.org/.

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ACM SIGDA PH.D. FORUM

Tuesday, June 9: 7:00 - 8:30pm || Room: 306 || Track: EDA || Topic Area: General Interest

ORGANIZERS:
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*
Zhuo Li - *Cadence Design Systems, Inc., Austin, TX*
Swaroop Ghosh - *Univ. of South Florida, Tampa, FL*

The Ph.D. Forum at the Design Automation Conference is a poster session hosted by ACM SIGDA for senior Ph.D. students to present and discuss their dissertation research with people in the EDA community.

Participation in the forum is highly competitive with an acceptance rate of around 30%. The forum is open to all members of the design automation community and is free-of-charge.

Co-Sponsored by:

METHODOLOGY AND METRICS FOR ANALOG/MIXED-SIGNAL VERIFICATION: MADNESS OR MARRIAGE?

Wednesday, June 10: 12:00 - 1:30pm || Room: 104 || Track: EDA || Topic Area: Digital Circuits

The trends are clear: more chip designs have a greater blend of analog and digital behavior. Often, both of these are being controlled by increasingly complex software. Hear the experts weigh in on the idea of applying the rigors of metric-driven verification planning and management from the digital realm to analog and mixed-signal design. Is this a natural progression of managing skyrocketing verification complexity, or is this a really bad idea because of skill sets, organizational boundaries, and the principles of divide and conquer? Enjoy a lively debate.
For more information, visit:
http://www.cadence.com/dac2015/Pages/luncheons.aspx

DECODING FORMAL TRAINING DAY: TAKE A DAY TRIP TO FORMAL SIGN-OFF

Thursday, June 11: 10:30am - 5:30pm || Room: 270 || Track: EDA || Topic Area: Business

Formal Sign-off is possible with today's technology and methodology. To get there, it takes knowledge and practice. This training day is hosted by Oski Technology and aims to impart our decades of knowledge about formal technology development and formal methodology application, to help you gain incredible insight on what it takes to achieve Formal Sign-off.

You will learn a lot and enjoy your day trip with us to Formal Sign-off!

SPEAKERS:
Vigyan Singhal - *Oski Technology, Inc., Mountain View, CA*
Prashant Aggarwal - *Oski Technology, Inc., Gurgaon, India*

NEWTON YOUNG FELLOW PROGRAM CLOSING SESSION & AWARD CEREMONY

Thursday, June 11: 6:00 - 7:00pm || Room: 300 || Track: EDA || Topic Area: General Interest

The Newton Young Fellow Program is designed to assist young students at the beginning of a career in Electronic Design Automation and Embedded Systems. Each Newton Young Fellow will actively engage in DAC through a number of events including meetings with design automation luminaries, attendance at technical sessions and exhibits, participation in student-related events at DAC. In addition, Newton Young Fellows will participate in a welcome orientation breakfast on Sunday morning, attend the Design Automation Summer School program, present posters of their academic/research work on Tuesday evening (colocated with the SIGDA Ph.D. Forum), and participate in a closing award ceremony for Young Fellows on Thursday evening.

Following a 50-year tradition, DAC strives to foster a vibrant and worldwide community of electronic design and embedded systems professionals; the fellowship actively supports and attempts to build an active cohort of the next generation of EDA and Embedded Systems professionals.

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The **ACM Special Interest Group on Design Automation** specializes in applications of computing to all phases of the electrical and electronics design fields, including techniques, algorithms, and computer programs for computer-aided design and testing systems, structure and software. **www.acm.org/sigda**

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TRENDS AND WHAT'S HOT AT DAC

Monday, June 8: 10:30 - 11:00am || Room: Booth 311
Track: EDA || Topic Area: General Interest

ORGANIZERS:
Anne Cirkel - *Mentor Graphics Corp., Wilsonville, OR*
Bob Gardner - *EDA Consortium, San Jose, CA*

Longtime EDA analyst Gary Smith of Gary Smith EDA will give us his take on the EDA's hottest technology trends. How will the dramatic changes in EDA, the semiconductor market and the design community affect you?

What are the hot 'must sees' at this year's conference? That plus a rundown of his annual Sunday night talk. Find out here!

SPEAKER:
Gary Smith - *Gary Smith EDA, San Jose, CA*

FIRESIDE CHAT WITH WALLY RHINES

Monday, June 8: 11:30am - 12:15pm || Room: Booth 311
Track: EDA || Topic Area: General Interest

MODERATOR:
Dan Nenni - *SemiWiki, San Jose, CA*
ORGANIZER:
Laura Parker - *Mentor Graphics Corp., Wilsonville, OR*

Join us for a more informal interaction with Wally Rhines, CEO of Mentor Graphics. Come to the pavilion to be part of an onstage chat where Semiwiki blogger Dan Nenni engages him in a wide ranging conversation spanning his career, the path he sees for the industry, and the changing role of design automation. Be prepared to ask your own questions.

SPEAKER:
Wally Rhines - *Mentor Graphics Corp., Wilsonville, OR*

SKY TALK: WOMEN, LEADERSHIP AND TECHNOLOGY: WHY TECHNOLOGY NEEDS MORE WOMEN

Monday, June 8: 1:00 - 1:30pm || Room: Booth 311 || Track: EDA || Topic Area: Business

CHAIR:
Donatella Sciuto - *Politecnico di Milano, Italy*

Technology innovation is at the heart of the world's positive future, and there is no question that innovation and business success benefit when women and men are together at the table creating technology. Today, women make up about 25% of the technical workforce and earn 18% of computer science degrees.

Dr. Whitney will draw on her experience in this area to frame the discussion of where women are today in technology, and present strategies that work both for women to succeed and for organizations that are committed to creating inclusive environments where women thrive.

SPEAKER:
Telle Whitney - *Anita Borg Institute, Palo Alto, CA*

TEAR-DOWN: A PEEK INSIDE THE DJI'S PHANTOM DRONE AND APPLE'S FIRST WEARABLE ELECTRONIC DEVICE - THE APPLE WATCH

Monday, June 8: 2:00 - 2:45pm || Room: Booth 311
Track: Embedded Systems || Topic Area: Emerging Technologies

ORGANIZERS:
Michael McNamara - *Adapt-IP, Campbell, CA*
Tom Anderson - *Breker Verification Systems, Inc., Fremont, CA*

Join iFixit's tear-down experts for an in-depth tour inside DJI's Phantom Drone. These modern day Drones are more than toys; they are phenomenal pieces of engineering which solve a complex set of very difficult physical problems in real time order to take flight. The Phantom Quadcopter comes pre-assembled in a sleek, white, plastic frame; but contains much of the same hardware as other hobbyist drones, in a more condensed package.

The iFixit team will take us for a detailed look at the propulsion, control, power, and video systems of this amazing device.

In addition to with the Drone tear-down, iFixit's experts will give attendees a treat as they also tear-down Apple's first foray into wearable electronics, the Apple Watch, in all of its high-fashion glory.

SKY TALK: IoT SECURITY: SOLUTIONS AND CHALLENGES AHEAD

Monday, June 8: 3:30 - 4:00pm || Room: Booth 311 || Track: Security || Topic Area: Security

CHAIR:
Mark Tehranipoor - *Univ. of Connecticut, Storrs, CT*

Large and small enterprises have long focused on security issues in their network, and those come from bugs, phishing, and viruses. However, they will soon be faced with a new and more formidable foe in Internet of Things. Cisco has predicted that by 2020, there will be more than 50 billions of IoT devices connected to network. Authentication, traceability, tamper resistance, and encryption are few example challenge to address.

SPEAKER:
Charles Hudson Jr. - *Comcast Corporation, Philadelphia, PA*

COMPARE FLOOR NOTES WITH COOLEY

Monday, June 8: 4:30 - 5:00pm || Room: Booth 311
Track: EDA || Topic Area: General Interest

ORGANIZER:
Carole Dunn - *Mentor Graphics Corp., Wilsonville, OR*

At the end of DAC Monday through DAC Wednesday -- a *small* unscripted interactive 30 minute gathering where John Cooley of DeepChip and the EDA users in the audience compare notes on what they saw on the DAC Exhibit Floor during that day.

Join us and share or just listen! Starts every day at 4:30 in the DAC Pavilion.

SPEAKER:
John Cooley - *Deepchip, Holliston, MA*

SDA, IoT, OR CS - IT'S HERE! WHAT DOES IT MEAN FOR YOU?

Tuesday, June 9: 10:30 - 11:00am || Room: Booth 311
Track: Embedded Systems || Topic Area: General Interest

ORGANIZERS:
Anne Cirkel - *Mentor Graphics Corp., Wilsonville, OR*
Bob Gardner - *EDA Consortium, San Jose, CA*

Whether you call it System Design Automation, IoT, or Connected Systems - IT's HERE !!! Come and see what "IT" is and how it will impact your growth. Longtime EDA analyst Gary Smith of Gary Smith EDA will give us his take on the technology trends in the system design domain, how the driving force of connectivity impacts what we do in EDA and his prediction on the growth path moving forward.

SPEAKER:
Gary Smith - *Gary Smith EDA, San Jose, CA*

FIRESIDE CHAT WITH LIP-BU TAN

Tuesday, June 9: 11:30am - 12:15pm || Room: Booth 311
Track: EDA || Topic Area: General Interest

MODERATOR:
Ed Sperling - *Semiconductor Engineering, San Jose, CA*
ORGANIZER:
Qi Wang - *Cadence Design Systems, Inc., San Jose, CA*

Please join us at the pavilion for a special one-on-one conversation with Lip-Bu Tan, president and CEO of Cadence and one of the foremost international venture capitalists in high tech, who will talk about the trends in design, where the challenges are, and why EDA is evolving to address complete end-product development.

Ed Sperling, editor in chief of Semiconductor Engineering, will guide this discussion, which will include questions taken from the audience.

SPEAKER:
Lip-Bu Tan - *Cadence Design Systems, Inc., San Jose, CA*

SKY TALK: VIRTUAL TO THE (NEAR) END - USING VIRTUAL PLATFORMS FOR CONTINUOUS INTEGRATION

Tuesday, June 9: 1:00 - 1:30pm || Room: Booth 311
Track: Embedded Systems || Topic Area: Embedded Software

CHAIR:
Rob Oshana - *Freescale Semiconductor, Inc., Austin, TX*

Continuous integration (CI) is a hot topic in software development. CI make sure code is tested quickly and integrated incrementally, enabling Agile methods, higher quality software, and higher development velocity. Using virtual platforms along with other simulators, it is possible to broadly enable CI for both new hardware designs and existing embedded systems that would otherwise be considered difficult targets for CI. In this talk, we will cover how to enable CI using simulation, and some examples of how simulation-based CI has been used in the telecom and aerospace industries.

SPEAKER:
Jakob Engblom - *Wind River Systems, Inc., Kista, Sweden*

THE STATE OF THE INTERNET OF THINGS: PROMISES, OPPORTUNITIES AND ROADBLOCKS

Tuesday, June 9: 2:00 - 2:45pm || Room: Booth 311
Track: Embedded Systems || Topic Area: Emerging Technologies

MODERATOR:
James Hogan - *Vista Ventures, Los Gatos, CA*
ORGANIZERS:
James Hogan - *Vista Ventures, Los Gatos, CA*
Michael McNamara - *Adapt-IP, Campbell, CA*
Tom Anderson - *Breker Verification Systems, Inc., Fremont, CA*

The Internet of Things (IoT) has become a mainstream term but much of the attention is focused on the latest gadgets rather than IoT's potential in super-charging efficiencies of every industry sector. Whether it's using connected devices to monitor the health of a patient or an elderly relative in their homes; deploying smart jet engines that transmit terabytes of data on its condition in-flight or ensuring miners' safety and productivity with integrated communications, tracking and real-time analytics, the Internet of Things can have a monumental impact on global economy, with the forecast of over $14 trillion in the next two decades, according to latest research by Accenture.

But what does this all mean for design professionals? Beyond the trade show gadgets, IoT initiatives require immense support from all IT functions. Collecting, storing and analyzing immense amounts of data, which can be easily accessed in the cloud at any time and securely shared across connected devices is no easy feat. With this information can we also apply machine learning to investigate opportunities like never before. More so, a standardized set of guiding principles is essential for governance and proper implementation of every supported initiative.

PANELISTS:
Amit Gupta - *Solido Design Automation, Inc., Saskatoon, SK, Canada*
Karim Arabi - *Qualcomm Technologies, Inc., San Diego, CA*
Ken Wagner - *PMC-Sierra, Inc., Ottowa, ON, Canada*

SKY TALK: THE PERFECT STORM: TRENDS IN FUNCTIONAL VERIFICATION

Tuesday, June 9: 3:30 - 4:00pm || Room: Booth 311 || Track: EDA || Test and Verification

CHAIR:
Kevin Morris - *EE Journal, Portland, OR*

Technical publications often make either subjective or unsubstantiated claims about today's functional verification process—such as, 70 percent of a project's overall effort is spent in verification. Yet, there are very few credible industry studies that quantitatively provide insight into the functional verification process in terms of verification technology adoption, effort, and effectiveness.

To address this dearth of knowledge, a recent world-wide, double-blind, functional verification study was conducted, covering all electronic industry market segments. To our knowledge, this is the largest independent functional verification study ever conducted. This keynote presents the findings from our 2014 study and provides invaluable insight into the state of the electronic industry today in terms of both design and verification trends.

SPEAKER:
Harry D. Foster - *Mentor Graphics Corp., Wilsonville, OR*

COMPARE FLOOR NOTES WITH COOLEY

Tuesday, June 9: 4:30 - 5:00pm || Room: Booth 311
Track: EDA || Topic Area: General Interest

ORGANIZER:
Carole Dunn - *Mentor Graphics Corp., Wilsonville, OR*

At the end of DAC Monday through DAC Wednesday -- a *small* unscripted interactive 30 minute gathering where John Cooley of DeepChip and the EDA users in the audience compare notes on what they saw on the DAC Exhibit Floor during that day.

Join us and share or just listen! Starts every day at 4:30 in the DAC Pavilion.

SPEAKER:
John Cooley - *Deepchip, Holliston, MA*

HOW OPEN COLLABORATION IS FOSTERING THE "NEW MOBILITY" (R)EVOLUTION

Wednesday June 10: 10:30 - 11:00am || Room: Booth 311
Track: Automotive || Topic Area: General Interest

CHAIR:
Michelle Clancy -*Cayenne Communication, Sunnyvale, CA*

Corey Clothier, Project Manager in Advanced Vehicle Technologies, of Local Motors, a technology company that designs, builds, and sells vehicles. Founded in 2007, Local Motors is the first automotive co-creation community, and the first company to produce an open source vehicle. Local Motors is working towards the release of a highway legal car produced solely by Direct Digital Manufacturing in 2016. Corey will provide a glimpse into the future of co-created, 3D printed mobility systems.

Corey Clothier joined Local Motors in 2015 to lead the charge to self-driving vehicles and the future of direct digital manufacturing. For 10 years, Corey served in the U.S. Marines. After the Corps, Corey joined the Detroit automotive engineering legion working with Cosworth, Lear Automotive, GM test labs and Ford. For the past 6+ years Corey has been focused on strategic development consulting for the U.S. Army Ground Vehicle Robotics R&D center where he co-developed the US Army program, ARIBO (Autonomous Robotics for Installation and Base Operations), which was a featured White House Smart America Challenge project with U.S. Departments of Defense, Energy and Transportation working together.

SPEAKER:
Corey Clothier - *Local Motors, Chandler, AZ*

FIRESIDE CHAT WITH AART DE GEUS

Wednesday June 10: 11:30am - 12:15pm || Room: Booth 311
Track: EDA || Topic Area: General Interest

MODERATOR:
Ed Sperling - *Semiconductor Engineering, San Jose, CA*
ORGANIZER:
Sabina Burns - *Synopsys, Inc., Mountain View, CA*

Join us for a lively and insightful interview with Aart de Geus, Chairman and co-CEO of Synopsys, on the future of design, the challenges of 10nm and beyond, and why the industry must 'shift left' on verification.

We'll also look ahead to where the future opportunities will be in the next one to five years. Come prepared to ask your questions. Ed Sperling, editor-in-chief of Semiconductor Engineering, will moderate the discussion.

SPEAKER:
Aart de Geus - *Synopsys, Inc., Mountain View, CA*

SKY TALK: BUILDING INFINITE SERVICE OPPORTUNITIES WITH IoT

Wednesday, June 10: 1:00 - 1:30pm || Room: Booth 311
Track: Embedded Systems || Topic Area: Business

CHAIR:
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

The IoT revolution will transform many markets from a 'sale of goods' to a 'sale of goods and services' economy. Embedded vendors have an opportunity to leverage IoT capabilities to stay relevant and grow. Intelligent and connected platforms will emerge, enabling new platform- or associated ecosystem- based value chains. Many will attempt to capitalize on the vast IoT opportunity – some will be traditional embedded designers, others experts in application development and software design with imaginative ideas they need to get to market quickly. We will discuss how forward-thinking semiconductor vendors can serve customers through system solutions that let them focus on efficiently designing unique IoT applications.

SPEAKER:
Ali Sebt - *Renesas Electronics America, Inc., Santa Clara, CA*

THE INTERNET OF THINGS: CAN WE CREATE A VIRTUAL SILICON VALLEY?

Wednesday, June 10: 2:00 - 2:45pm || Room: Booth 311
Track: Embedded Systems || Topic Area: Emerging Technologies

MODERATOR:
Lucio Lanza - *Lanza TechVentures, Palo Alto, CA*
ORGANIZERS:
Lucio Lanza - *Lanza TechVentures, Palo Alto, CA*
Michael McNamara - *Adapt-IP, Campbell, CA*
Tom Anderson - *Breker Verification Systems, Inc., Fremont, CA*

In this panel, Lucio Lanza and leading business experts will attempt to determine whether the semiconductor industry is at the point where it can export Silicon Valley to the rest of the world. They will take a thought-provoking look at how the Internet of Things has the potential to empower social cultures in foreign countries and remote societies while minimizing social disruption. Telepresence is only part of it. Vast numbers of people will be able to live and work where they want — and not live where their jobs require them to live — maintaining the lifestyle, culture and community they're accustomed to. In the world of the future, the Internet will be the highway that people use to commute to their jobs outside of Silicon Valley and the semiconductor industry has the tools to make this happen.

PANELISTS:
Alessandro Cremonesi - *STMicroelectronics, Milan, Italy*
Chris Rowen - *Cadence Design Systems, Inc., San Jose, CA*
Louise Kehoe - *Eastman Kodak, San Francisco, CA*

SKY TALK: CHIPS FOR AUTOMOTIVE - IC ROBUSTNESS VERIFICATION IN THE BRAVE NEW WORLD OF ISO 26262

Wednesday, June 10: 3:30 - 4:00pm || Room: Booth 311
Track: Automotive || Topic Area: Physical Design

CHAIR:
Anthony Cooprider - *Ford Motor Co., Dearborn, MI*

Electronics are playing an expanding role in automotive platforms. Their application is no longer tied to traditional systems such as airbag controllers or engine control but also expanding rapidly into advanced driver assistance systems. Reliable design of robust semiconductors for such systems, including compliance to industry standards like ISO 26262, became a critical success factor in this market. Meeting such standards - especially in the physical layout domain - requires advanced verification tool functionality and frameworks to ensure a reliable and traceable flow of requirements from the specification down to the layout development.

SPEAKER:
Maik Herzog - *Infineon Technologies AG, Munich, Germany*

COMPARE FLOOR NOTES WITH COOLEY

Wednesday, June 10: 4:30 - 5:00pm || Room: Booth 311
Track: EDA || Topic Area: General Interest

ORGANIZER:
Carole Dunn - *Mentor Graphics Corp., Wilsonville, OR*

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Company	Booth
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Mentor Graphics Corporation.	1432
Methodics, Inc.	1114
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Mixel, Inc.	2811
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ARM CONNECTED COMMUNITY PAVILION
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ADVANCED ELECTRONICS IN AUTOMOTIVE PAVILION
Booth 1303

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Dassault Systemes
Mentor Graphics Corporation
Synopsys, Inc.

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Brite Semiconductor
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CAST, Inc.
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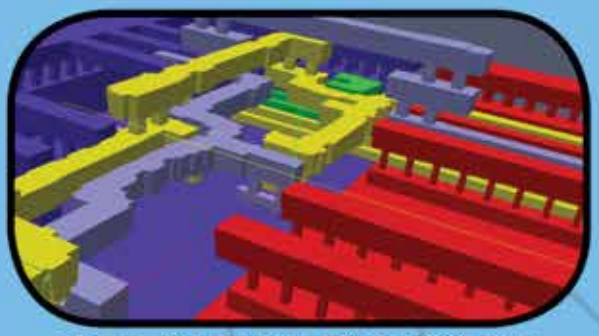
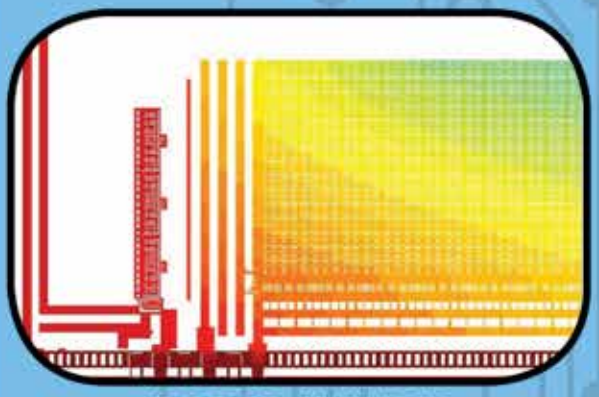


FULL CHIP EXTRACTION OF 28NM SOC



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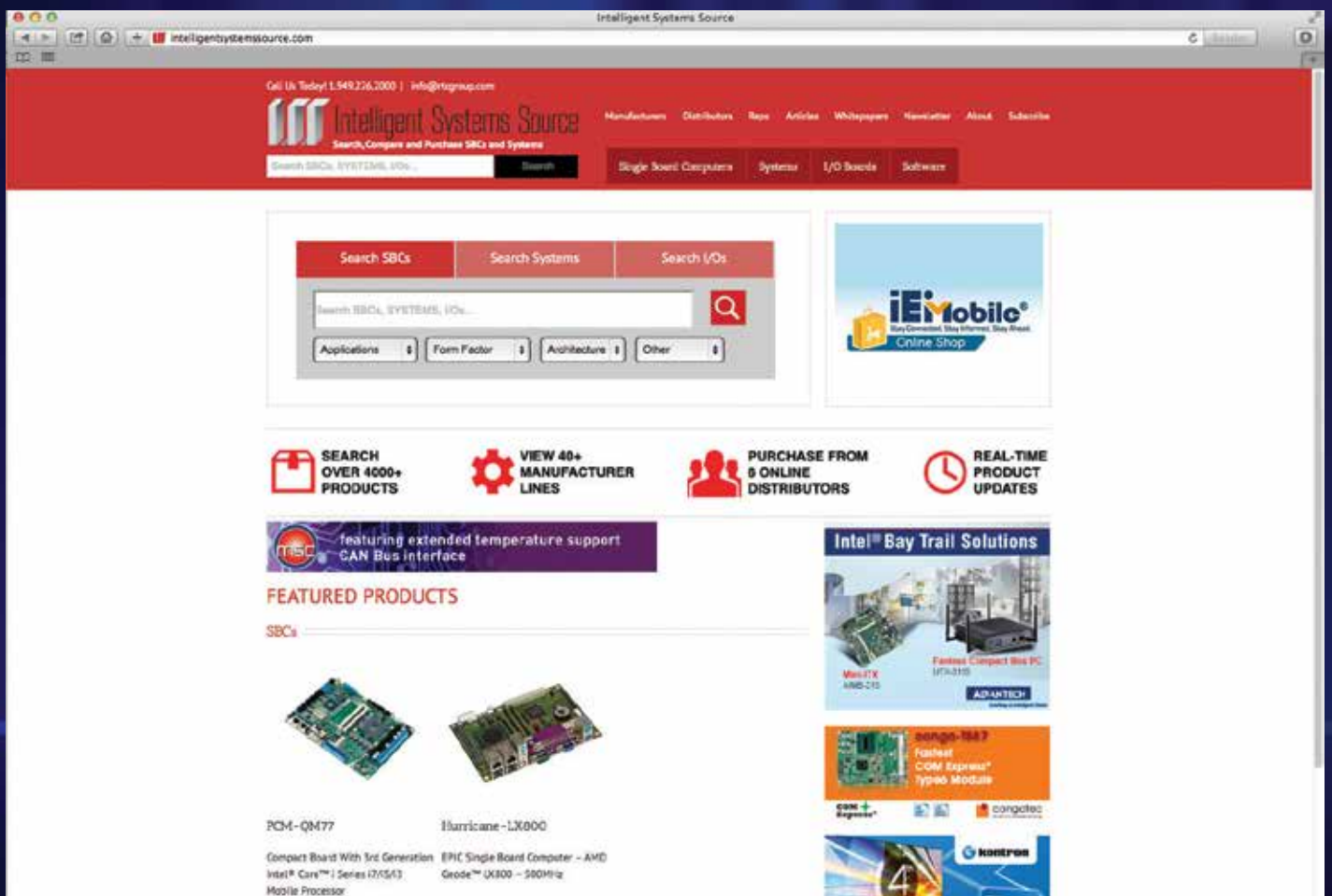

DAC ATTACK GAMING RULES/ACHIEVEMENTS:

Game BEGINS AT 10:00am ON JUNE 8 and ENDS AT 4:00pm ON JUNE 10

On your DAC Mobile App, check out the Leaderboard on the home page or the Social Media boards at the show to see everyone's scores in real time (points update immediately).

HOW DO I GET POINTS?

There are four ways to obtain points:

1. **Scan the QR Code at each participating exhibitor booth located on the DAC Exhibit Floor**
   There are different point categories for the exhibitors:

All Exhibitors	50 points
Silver sponsors	75 points
Gold Sponsors	100 points
Platinum Sponsors	125 points

2. **Tweet about DAC 25 points**
   Get points if you tweet about DAC, what you see at the conference, what you are learning etc. For each tweet with #52DAC you will receive points. You must post from Chatter inside the App or website and push out to Twitter, Facebook, or LinkedIn. Once you post in Chatter and push out, you will get the points.
3. **Find the missing treasure hidden around the show each day 150 points**
   This gets you the most points! Each day of the exhibit (Monday, Tuesday and Wednesday) DAC will hide the stuffed action figure: Elliott, the Engineering Superhero. Elliott will have a QR code on him, scan the code and earn the points. Please take a picture of the QR code but do not move Elliott so the next person can find him.
4. **Find a member of the DAC Executive Committee 100pts**
   Each member of the committee will be wearing a button with a QR code to scan. Scan the code and earn the points.

DAC ATTACK ENDS AT 4:00pm ON JUNE 10th. Winners will be announced by broadcast message within the App. Raffle prizes and the grand prize will be given out at the DAC Pavilion at 4:30pm. If you are a winner and have already departed by 4:30pm, your prize will be shipped to the address you entered when you registered for DAC.

PRIZES

There are two types of prizes: raffle prizes and the grand prize. Raffle winners will be selected from the top 50% of the participants in the game. The Grand Prize winner will be the attendee with the most points.

Raffle prizes:

- $150 Gift Card to the Apple Store
- $150 Gift Card to Amazon
- Bose Mini Bluetooth Speaker
- Beats Solo Headphones

Grand Prize:
New Apple Watch

RULES AND HELPFUL INFORMATION

- As some prizes may be shipped to winning contestants, you do not need to be present to win.
- Ties will be broken with a lottery.
- Only DAC registered attendees are eligible to win.
- Those holding an exhibitor badge are not eligible to win.
- Please play fair! We reserve the right to remove points that were obtained in a fraudulent manner.
- How to scan a QR code: Go to the menu screen on your App (the 3 horizontal lines on the top left hand corner of your screen) and touch the 'Scanner' tab. Place the QR code inside your screen and wait until your screen says: 'Achievement Unlocked' or 'Success'.
  No need to touch a button like on a camera, it will do all the work for you.

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