47th DESIGN AUTOMATION CONFERENCE®
Anaheim Convention Center
Anaheim, CA - June 13 - 18, 2010
FOR INFORMATION CALL: +1-303-530-4333

With a heritage of excellence for almost half a century, DAC continues to be the premier conference devoted to Electronic Design Automation (EDA) and the application of EDA tools in designing advanced electronic systems. DAC 2010 is seeking papers that deal with tools, algorithms, and design techniques for all aspects of electronic circuit and system design. We invite submissions in the following categories: research papers, User Track papers, "Wild and Crazy Ideas" (WACI) topic papers, suggestions for special sessions, panels, and tutorials, and proposals for workshops and colocated events. Submissions must be made electronically at the DAC website. Detailed guidelines for all categories are available on the DAC website.
Focus Areas: Apart from the core Electronic Design Automation topics, DAC specifically solicits papers in the areas of design automation for many-core architectures, system prototyping technology, embedded software design and debug, and design automation in a cloud computing environment.

RESEARCH PAPERS
DUE BEFORE 5:00pm MT, November 19, 2009

Research paper submissions MUST (1) be in PDF format only, (2) contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission, (3) be no more than six pages (including the abstract, figures, tables, and references), double columned, 9-pt or 10-pt font, and (4) MUST NOT identify the author(s) by their name(s) or affiliation(s) anywhere on the manuscript or abstract, with all references to the author(s)'s own previous work or affiliations in the bibliographic citations being in the third person. Preliminary submissions will be at a disadvantage. Format templates are available on the DAC website. Submissions not adhering to these rules will be rejected. DAC will compare each submission against a vast database and any paper with significant similarity to previously published works or with papers that are simultaneously under review with other conferences and symposia, will be rejected. All research papers will be reviewed as finished papers. Authors of accepted papers must sign a copyright release form for their paper.
Acceptance notices will be available by logging in to the DAC website after Feb. 25, 2010.
Complete author kits will be available on the DAC website by March 9, 2010.
All conference presenters will be required to register at the time of final paper submission.

USER TRACK PAPERS - EXTENDED ABSTRACTS
DUE BEFORE 5:00pm MT, November 9, 2009

DAC's User Track addresses the real-life issues facing IC designers, application engineers, and design flow developers. It provides valuable insights and experiences with in-house or commercial EDA tool flows. User Track papers may describe the application of EDA tools to the design of a novel electronic system, or the integration of EDA tools within a design flow or methodology to produce such systems. A User Track paper may be problem-specific in scope (e.g., analyzing substrate coupling during floorplanning) or may address a specific application domain (e.g., designing wireless handsets). Submissions are in the form of an extended abstract. For more details, please see the separate User Track Call for Papers on the DAC website:
http://www.dac.com/47th/UTinfo.html

WILD AND CRAZY IDEAS (WACI) PAPERS
DUE BEFORE 5:00pm MT, November 19, 2009

The "Wild and Crazy Ideas" sessions cover interesting activities on a wide variety of topics that do not fit in the conventional mold. The WACI track features novel (and even preliminary or unproven) technical ideas. The aim of WACI is to promote revolutionary and way-out ideas that inspire discussion among conference attendees, create a buzz, and get people talking. Submissions to the "Wild and

Crazy Ideas" track should not exceed two pages, but must otherwise follow the above rules and deadlines for the research papers. Unlike a DAC research paper that explores a specific technology problem and proposes a complete solution to it, with a full table of results, a WACI paper could present less developed but highly innovative ideas related to areas relevant to DAC. All WACI accepted papers will be required to post a two-minute video describing the work as part of the acceptance process.

SPECIAL SESSION SUGGESTIONS DUE BEFORE 5:00pm MT, November 2, 2009

Special session suggestions must include descriptions of the proposed papers and speakers, and the importance of the special session to the DAC audience. As the term implies, a special session is devoted to a topic of strong contemporary or future interest. The topic must represent an emerging area that does not yet receive sufficient focus from research papers. A submission must list at least three inspiring speakers who address the topic from different angles. DAC reserves the right to restructure all special session suggestions.

PANEL and TUTORIAL SUGGESTIONS DUE BEFORE 5:00pm MT, November 2, 2009

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panel and tutorial suggestions.
Please see the website for further details, or call Kevin Lepine, Conference Manager at +1-303-530-4333.

WORKSHOP SUBMISSIONS DUE BEFORE 5:00pm MT, January 29, 2010

DAC invites you to organize a workshop on topics related to design, design methodologies, and design automation. DAC provides the financial and organizational support, including attendee registration, rooms at the conference center and audio visual equipment. Please see the website for further details, or call Kevin Lepine, Conference Manager at +1-303-530-4333.

COLOCATED EVENT PROPOSALS DUE BEFORE 5:00pm MT, January 29, 2010

DAC invites you to colocate your conference, meeting or other special event with DAC. We will provide you with meeting rooms at the conference center at no cost. Your event will be financed and otherwise organized by you. Please see the website for further details, or call Kevin Lepine, Conference Manager, at +1-303-530-4333.

STUDENT DESIGN CONTEST SUBMISSIONS DUE BEFORE 5:00pm MT, November 25, 2009

ISSCC and DAC will jointly sponsor of the 2010 ISSCC/DAC Student Design Contest. The contest promotes excellence in the design of electronic systems within an academic environment and provides a forum in which undergraduate/graduate students' ingenuity can be shared with an audience of academic/industrial technical experts. The winners will present their designs through a poster at ISSCC 2010 and DAC 2010.
Designs can be for analog, digital, MEMS, optics, biological, or programmable circuits and embedded
systems/platforms in any of the three categories: operational, system level, or conceptual.
Please visit the DAC website for more details.

SUBMISSION CATEGORIES FOR RESEARCH PAPERS

Authors of research papers are required to specify a category from the following list:

1. System-Level Design and Codesign

1.1 System specification, modeling, simulation, verification, and performance analysis

1.2 Scheduling, HW/SW partitioning, HW/SW interface synthesis

1.3 IP and platform-based design, IP protection

1.4 System-On-Chip (SOC) and multiprocessor System-On-Chip (MPSOC)

1.5 Application-specific processor design tools

2. System-Level Communication and Networks-On-Chip

2.1 Modeling and performance analysis

2.2 Communications-based design, communication and network synthesis

2.3 Optimization for energy, fault tolerance, reliability

2.4 Interfacing and software issues, beyond-the-die communication

2.5 NOC design methodologies, case studies and prototyping

3. Embedded Hardware Design and Applications

3.1 Case studies of embedded system design

3.2 Flows and methods for specific applications and design domains

4. Embedded Software Tools and Design

4.1 Retargetable compilation

4.2 Memory/cache optimization

4.3 Software for single-/multiprocessor, multicore, GPU systems

4.4 Real-time operating systems

4.5 Verification of embedded software

5. Power Analysis and Low-Power Design

5.1 System-level power design and thermal management

5.2 Embedded low-power approaches: partitioning, scheduling, and resource management

5.3 High-level power estimation and optimization

5.4 Gate-level power analysis and optimization

5.5 Device and circuit techniques for low-power design

5.6 Power-aware and energy-efficient wireless protocols, algorithms and associated design techniques and methodologies

6. Verification

6.1 Functional, transaction-level, RTL, and gate-level modeling and verification of hardware design

6.2 Dynamic simulation, equivalence checking, formal (and semiformal) verification model and property checking

6.3 Emulation and hardware simulators or accelerator engines

6.4 Modeling languages and related formalisms, verification plan development and implementation

6.5 Assertion-based verification, coverage analysis, constrained random testbench generation

6.6 Verification techniques for software correctness

7. High-Level Synthesis, Logic Synthesis and Circuit Optimization

7.1 Combinational, sequential, and asynchronous logic synthesis

7.2 Library mapping, cell-based design and optimization

7.3 Transistor and gate sizing, resynthesis

7.4 Interactions between logic design and layout or physical synthesis

7.5 High-level, behavioral, algorithmic, and architectural synthesis, “C” to gates tools and methods

7.6 Resource scheduling, allocation, and synthesis

8. Circuit, Interconnect and Manufacturing Simulation and Analysis

8.1 Electrical-level circuit simulation

8.2 Model order reduction methods for linear systems
8.3 Interconnect and substrate modeling and extraction
8.4 High-frequency and electromagnetic simulation of circuits
8.5 Thermal and electrothermal simulation
8.6 Technology CAD and fab automation

9. Timing Analysis

9.1 Process technology characterization, and modeling
9.2 Deterministic static timing analysis and verification
9.3 Statistical performance analysis and optimization

10. Physical Design and Manufacturability

10.1 Floorplanning, partitioning, placement
10.2 Buffer insertion, routing, interconnect planning
10.3 Physical verification and design rule checking
10.4 Automated synthesis of clock networks
10.5 Reticle enhancement, lithography-related design optimizations
10.6 Design for manufacturability, yield, defect tolerance, cost issues, and DFM impact
10.7 Physical design of 3-D integrated circuits
10.8 System-in-package design, package-board codesign
10.9 Design for resilience under manufacturing variations

11. Signal Integrity and Design Reliability

11.1 Signal integrity, capacitive and inductive crosstalk
11.2 Reliability modeling and analysis
11.3 Novel clocking and power delivery schemes
11.4 Power grid robustness analysis and optimization
11.5 Soft errors
11.6 Thermal reliability

12. Analog, Mixed-Signal, and RF

12.1 Analog, mixed-signal, and RF design methodologies
12.2 Automated synthesis
12.3 Analog, mixed-signal, and RF simulation
12.4 High-frequency design and advanced antenna design for wireless design

13. FPGA Design Tools and Applications

13.1 Rapid prototyping
13.2 Logic synthesis and physical design techniques for FPGAs
13.3 Configurable and reconfigurable computing

14. Testing

14.1 Test quality/reliability, current based test, delay test, low-power test
14.2 Digital fault modeling, automatic test generation, fault simulation
14.3 Digital design for test, test data compression, built-in self test
14.4 Memory test and repair, FPGA testing
14.5 Fault-tolerance and online testing
14.6 Analog/mixed-signal/RF testing, system-in-package (SIP) testing
14.7 Board- and system-level test, system-on-chip (SOC) testing
14.8 Silicon debug and diagnosis, post-silicon design validation

15. New and Emerging Design Technologies (including but not restricted to)

15.1 MEMS, sensors, actuators, imaging devices
15.2 Nanotechnologies, nanowires, nanotubes
15.3 Quantum computing
15.4 Synthetic and systems biology, biologically-based or biologically-inspired systems
15.5 Non-CMOS 3-D design, new transistor structures and devices, design in new or radical process technologies
15.6 Optical devices and communication

ALL SUBMISSIONS MUST BE MADE ELECTRONICALLY AT THE DAC WEBSITE: WWW.DAC.COM.

ACM and IEEE reserve the right to exclude a paper from archival distribution after the conference if the paper is not presented by one of the co-authors at the conference, or in other exceptional cases. DAC will support the IEEE Prohibited Authors List.