



**46th DAC Best Paper Candidates** Seven papers were nominated by the Technical Program Committee as DAC Best Paper Candidates. Final decisions will be made after the papers are presented at the conference. The awards for the best paper will be presented at 12:00pm on Thursday, July 30, in Gateway Ballroom, prior to the Special Plenary Panel.

#### 10.3 Generating Test Programs to Cover Pipeline Interactions Thanh Nga Dang – National Univ. of Singapore, Singapore Abbit Durbardhum, National Univ. of Singapore

Abhik Roychoudhury – National Univ. of Singapore, Singapore Tulika Mitra – National Univ. of Singapore, Singapore Prabhat Mishra – Univ. of Florida, Gainesville, FL

12.1 GPU Friendly Fast Poisson Solver for Structured Power Grid Network Analysis

Jin Shi – Tsinghua Univ., Beijing, China Yici Cai – Tsinghua Univ., Beijing, China Wenting Hou – Synopsys, Inc., Beijing, China Liwei Ma – Synopsys, Inc., Beijing, China Sheldon X.-D. Tan – Univ. of California, Riverside, CA Pei-Hsin Ho – Synopsys, Inc., Hillsboro, OR Xiaoyi Wang – Tsinghua Univ., Beijing, China

15.1 An Efficient Approach for System-Level Timing Simulation of Compiler-Optimized Embedded Software Zhonglei Wang – Technische Univ. München, Munich, Germany Andreas Herkersdorf – Technische Univ. München, Munich, Germany

18.2 A Computing Origami: Folding Streams in FPGAs Andrei Hagiescu – National Univ. of Singapore, Singapore Weng-Fai Wong – National Univ. of Singapore, Singapore David Bacon – IBM Corp., Hawthorne, NY Rodric Rabbah – IBM Corp., Hawthorne, NY

### 22.1 Statistical Multi-Layer Process Space Coverage for At-Speed Test

Jinjun Xiong – IBM Corp., Yorktown Hts., NY Yiyu Shi – Univ. of California, Los Angeles, CA Vladimir Zolotov – IBM Corp., Yorktown Hts., NY Chandu Visweswariah – IBM Corp., Yorktown Hts., NY

23.2 A Robust and Efficient Harmonic Balance (HB) Using Direct Solution of HB Jacobian

Amit Mehrotra – Berkeley Design Automation, Santa Clara, CA Abhishek Somani – Berkeley Design Automation, Bangalore, India

### 24.3 New Spare Cell Design for IR Drop Minimization in Engineering Change Order

Hsien-Te Chen – National Tsing-Hua Univ., Hsinchu, Taiwan Chieh-Chun Chang – National Tsing-Hua Univ., Hsinchu, Taiwan TingTing Hwang – National Tsing-Hua Univ., Hsinchu, Taiwan

## DAC 2009 Best Paper Award

## A Robust and Efficient Harmonic Balance (HB) Using Direct Solution of HB Jacobian

Amit Mehrotra - Berkeley Design Automation, Santa Clara, CA Abhishek Somani - Berkeley Design Automation, Bangalore, India

## DAC Best User Track Poster Award

### Attacking Constraint Complexity in Large Scale Random Verification Environment

Ben Chen, Srinath Atluri, Harish Krishnamoorthy - Cisco Systems, Inc., San Jose, CA

Alex Wakefield, Balamurugan Veluchamy - Synopsys Inc., Mountain View, CA

# DAC Best User Track Poster Award Honorable Mention

Timing Closure in 65-Nanometer ASICs using Statistical Static Timing Analysis Design Methodology

Llewellyn Marshall, Eric Foreman - IBM Corp., Essex Jct, VT

Visualizing Debugging using Transaction Explorer in SOC System Verification

Alicia Strang, Robert Carden IV - Marvell Semiconductor Inc., Aliso Viejo, CA

