DESIGN AUTOMATION CONFERENCE

Call For Papers

DAC is the premier conference devoted to Electronic Design Automation and the application of Electronic Design Automation tools in designing electronic systems. DAC 2009 is seeking papers that deal with tools, algorithms, and design techniques for all aspects of electronic circuit and system design. We invite submissions in the following categories: regular papers, User Track papers, "Wild and Crazy Ideas" (WACI) topic papers, special sessions, panels, tutorials, workshops, colocated events, and the student design contest. Submissions must be made electronically at www.dac.com. The submissions are due on different dates for the various categories as described below. Detailed submission guidelines for all categories are now available on the DAC website.

Focus Areas: Apart from the core Electronic Design Automation topics, DAC specifically solicits papers in several focus areas. These include multi-core applications in design automation, high-level design, virtual-hardware platform design, IP design, new technologies, technology CAD, fab automation, as well as packaging and beyond-the-die design.

NEW THIS YEAR! *User Track:* For 2009, we introduce a new dedicated User Track that addresses the issues facing designers, application engineers, and design-flow developers. User Track papers describe the use of EDA tools to design a novel electronic system, or the integration of EDA tools within a design flow or methodology to produce such systems. A paper may be problem-specific in scope (e.g., analyzing substrate coupling during floorplanning) or may address a specific application domain (e.g., designing wireless handsets), with applications to other types of designs and design flows being inferred. This User Track will provide educational opportunities for audience members interested in both tool use and associated limitations and potential improvements. Please see the separate User Track Call for Papers on the DAC website for more details: *http://www.dac.com/46th/PDFs/UTcfp.pdf*

Authors are required to specify a category from the following list:

1. System-level Design and Co-design
- 1.1 System specification, modeling, simulation, verification, and performance analysis
- 1.2 Scheduling, HW-SW partitioning, HW-SW interface synthesis
- 1.3 IP and platform-based design, IP protection
- 1.4 System-on-Chip (SoC) and Multiprocessor SoC (MPSoC)
- 1.5 Application-specific processor design tools

2. System-level Communication and Networks on Chip
- 2.1 Modeling and performance analysis
- 2.2 Communications-based design, communication and network synthesis
- 2.3 Architectural synthesis, mapping, routing, scheduling
- 2.4 Optimization for energy, fault-tolerance, reliability
- 2.5 Interfacing and software issues, beyond-the-die communication
- 2.6 NoC Design methodologies, case studies and prototyping

3. Embedded Hardware Design and Applications
- 3.1 Case studies of embedded-system design
- 3.2 Flows and methods for specific applications and design domains

4. Embedded Software Tools and Design
- 4.1 Retargetable compilation
- 4.2 Memory/cache optimization
- 4.3 Software for single/multi-processor, multi-core, GPU
- 4.4 Real-time operating systems
- 4.5 Verification of embedded software

5. Power Analysis and Low-power Design
- 5.1 System-level power design and thermal management
- 5.2 Embedded low-power approaches: partitioning, scheduling, and resource management
- 5.3 High-level power estimation and optimization
- 5.4 Gate-level power analysis and optimization
- 5.5 Device and circuit techniques for low-power design
- 5.6 Power-aware and energy-efficient wireless protocols, algorithms and associated design techniques and methodologies

6. Verification
- 6.1 Functional, transaction-level, RTL, and gate-level modeling and verification of hardware design
- 6.2 Dynamic simulation, equivalence checking, formal (and semi-formal) verification model and property checking
- 6.3 Emulation and hardware simulators or accelerator engines
- 6.4 Modeling languages and related formalisms, verification plan development and implementation
- 6.5 Assertion-based verification, coverage analysis, constrained-random testbench generation
- 6.6 Verification techniques for software correctness

7. High-level Synthesis, Logic synthesis and Circuit Optimization
- 7.1 Combinational, sequential, and asynchronous logic synthesis
- 7.2 Library mapping, cell-based design and optimization
- 7.3 Transistor and gate sizing, and resynthesis
- 7.4 Interactions between logic design and layout or physical synthesis
- 7.5 High-level, behavioral, algorithmic, and architectural synthesis, "C" to gates tools and methods
- 7.6 Resource scheduling, allocation, and synthesis

8. Circuit, Interconnect and Manufacturing Simulation and Analysis
- 8.1 Electrical-level circuit simulation
- 8.2 Model order reduction methods for linear systems
- 8.3 Interconnect and substrate modeling and extraction
- 8.4 High-frequency and electromagnetic simulation of circuits
- 8.5 Thermal and electrothermal simulation
- 8.6 Technology CAD and fab automation

9. Timing Analysis
- 9.1 Process technology characterization, and modeling
- 9.2 Deterministic static timing analysis and verification
- 9.3 Statistical performance analysis and optimization

10. Physical Design and Manufacturability
- 10.1 Physical floorplanning, partitioning, placement
- 10.2 Buffer insertion, routing, interconnect planning
- 10.3 Physical verification and design rule checking
- 10.4 Automated synthesis of clock networks
- 10.5 Reticle enhancement, lithography-related design optimizations
- 10.6 Design for manufacturability, yield, defect tolerance, cost issues, and impacts of DFM
- 10.7 Physical design of 3-D integrated circuits
- 10.8 System-in-Package design, package-board codesign
- 10.9 Design for resilience under manufacturing variations

11. Signal Integrity and Design Reliability
- 11.1 Signal integrity, capacitive and inductive crosstalk
- 11.2 Reliability modeling and analysis
- 11.3 Novel clocking and power delivery schemes
- 11.4 Power grid robustness analysis and optimization
- 11.5 Soft errors (single-event upsets)
- 11.6 Thermal reliability

12. Analog/Mixed-signal and RF
- 12.1 Analog, mixed-signal, and RF design methodologies
- 12.2 Automated synthesis
- 12.3 Analog, mixed-signal, and RF simulation
- 12.4 High-frequency design and advanced antenna design for wireless

13. FPGA Design Tools and Applications
- 13.1 Rapid prototyping
- 13.2 Logic synthesis and physical design techniques for FPGAs
- 13.3 Configurable and reconfigurable computing

14. Testing
- 14.1 Test quality/reliability, current-based test, delay test, low-power test
- 14.2 Digital fault modeling, automatic test generation, fault simulation
- 14.3 Digital design-for-test, test data compression, built-in self test
- 14.4 Memory test and repair, FPGA testing
- 14.5 Fault-tolerance and on-line testing
- 14.6 Analog/mixed-signal/RF testing, System-in-Package (SiP) testing
- 14.7 Board - and system-level test, System-on-Chip (SoC) testing
- 14.8 Silicon debug and diagnosis, post-silicon design validation

15. New and Emerging Design Technologies (including but not restricted to)
- 15.1 MEMS, sensors, actuators, imaging devices
- 15.2 Nanotechnologies, nanowires, nanotubes
- 15.3 Quantum computing
- 15.4 Biologically-based or biologically-inspired systems
- 15.5 Stacked devices for 3-D design, new transistor structures and devices, new or radical process technologies and optimization
- 15.6 Optical devices and communication

WACI

16. Wild and Crazy Ideas

We invite papers with genuinely forward-looking, radical, and innovative ideas in the area of electronic design or electronic design automation. Concepts that stimulate discussion are welcome. Research that incrementally improves on prior work is not suited for this category.

ALL SUBMISSIONS MUST BE MADE ELECTRONICALLY AT THE DAC WEBSITE: WWW.DAC.COM

REGULAR PAPERS DUE BEFORE 5:00pm MT, December 19, 2008

Regular paper submissions MUST (1) be in PDF format only, (2) contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission, (3) be no more than six pages (including the abstract, figures, tables, and references), double columned, 9-pt or 10-pt font, and (4) MUST NOT include name(s) or affiliation(s) of the author(s) anywhere on the manuscript or abstract, and with any references to the author(s)'s own previous work or affiliations in the bibliographic citations being in the third person. Format templates are available on the DAC website for your convenience. Submissions not adhering to these rules, or those previously published or simultaneously under review by another conference, will be rejected. DAC will compare each submission against a vast database. Any paper with significant similarity to previously published works or with papers that are under review with other conferences and symposia will be rejected. All regular papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage, except for submissions to WACI. Authors of accepted papers must sign a copyright release form for their paper. Acceptance notices will be available by logging in to the DAC website after March 26, 2009. Complete author kits will be sent via email by April 6, 2009.

USER TRACK SUBMISSIONS DUE BEFORE 5:00pm MT, December 19, 2008

NEW! User Track submissions contain an innovative or educational contribution in the area of design and the usage of EDA tools. Please see the separate User Track Call for Papers on the DAC website for details on this exciting NEW program: *http://www.dac.com/46th/PDFs/UTcfp.pdf*

WILD AND CRAZY IDEAS (WACI) SESSION PAPERS DUE BEFORE 5:00pm MT, December 19, 2008

The "Wild and Crazy Ideas" sessions cover interesting activities on a wide variety of topics that do not fit in the conventional mold. The WACI track features novel (and even unproven) technical ideas that create a buzz and get people talking. The aim of WACI is to promote revolutionary and way-out ideas that inspire discussion among conference attendees. Submissions to the "Wild and Crazy Ideas" track should not exceed two pages. Otherwise, they must follow the above rules and deadlines for the regular papers. A regular DAC paper explores a specific technology problem and proposes a complete solution to it, with a full table of results. In contrast, a WACI paper could present less developed, but highly innovative ideas related to areas relevant to DAC.

SPECIAL SESSION SUBMISSIONS DUE BEFORE 5:00pm MT, November 3, 2008

Special session submissions must include descriptions of suggested papers and speakers, and the importance of the special session to the DAC audience. As the term implies, a special session covers an entire session on a topic of strong contemporary or future interest. A submission must list at least three inspiring speakers who address the topic from different angles. The topic must represent an emerging area that does not yet receive sufficient focus from regular papers. DAC reserves the right to restructure all special session proposals.

PANEL AND TUTORIAL SUBMISSIONS DUE BEFORE 5:00pm MT, November 3, 2008

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panel and tutorial proposals.

STUDENT DESIGN CONTEST SUBMISSIONS DUE BEFORE 5:00pm MT, December 8, 2008

Students are invited to submit descriptions of original electronic designs, either circuit-level or system-level. Accepted contributions will be published in the proceedings and presented at DAC 2009. Therefore, this is an excellent opportunity for students to showcase their design work to the world. Student Design Contest paper submissions must (1) be in PDF format only, (2) contain the title of the project, (3) contain an abstract of approximately 60 words, (4) provide a complete description of the project, and (5) be no more than six pages (including the abstract, maximum of 10 figures/tables, and references), double columned, 9-pt or 10-pt font. The submission should clarify the originality, distinguishing features, and measured performance of the design. Three categories of designs - operational, system and conceptual - are eligible for awards. For operational designs, proof of implementation is required, while for conceptual designs a complete simulation and test plan is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2007. Submitted designs should not have received awards in other contests. Detailed rules and guidelines for all submissions are available on the DAC website.

WORKSHOP SUBMISSIONS DUE BEFORE 5:00pm MT, Friday, February 2, 2009

DAC invites you to organize a workshop on topics related to design, design methodologies, and design automation. DAC provides the financial and organizational support, including attendee registration, rooms at the conference center and audio visual equipment. Please see the website for further details, or call Kevin Lepine, Conference Manager at +1 303-530-4333.

COLOCATED EVENT SUBMISSIONS DUE BEFORE 5:00pm MT, Friday, February 2, 2009

DAC invites you to colocate your event – conference, meeting or some other special event – at DAC. We will provide you with rooms at the Moscone Center at no cost. Your event will be financed and otherwise organized by you. Please see the website for further details, or call Kevin Lepine, Conference Manager at +1 303-530-4333.

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