46 YEARS

DESIGN AUTOMATION CONFERENCE

Moscone Center

July 26 - 31, 2009

San Francisco

- *Keynotes*
- *Technical Sessions*
- *Special Sessions*
- *WACI*
- *Technical Panels*
- *Pavilion Panels*
- *Tutorials*
- *Student Design Contest*
- ***NEW! User Track***
- *Workshops*
- *Colocated Events*
- *Exhibitor Forum*
- ***NEW! IC Design Central Partner Pavilion***
- *Management Day*
- *Exhibitor Listing*

Sponsored by: acm, EDA CONSORTIUM, IEEE

Supported by: sigda, CEDA, IEEE CIRCUITS & SYSTEMS SOCIETY, CANDE

In Technical Cooperation with: SSCS

www.dac.com

Advance Program

DAC: Where The Electronic Design Community Meets…

Dear Colleague:

I look forward to welcoming you to San Francisco and the 46th Design Automation Conference!

For thousands of us across the electronic design and design automation fields, DAC will be a week of intense networking and learning. DAC is the one event each year where the entire life cycle of IC design technology is on display: new challenges in panels and special sessions; new technologies in research papers; new solutions in the exhibit suites of EDA startups; new insights into tools and methodologies at the Exhibitor Forum and the new User Track; new integrated reference flows from leading foundries and IP providers; continuing education in the form of full-day tutorials; … The opportunities for professional growth and new connections are truly endless. This is why business leaders, market leaders, technical leaders and thought leaders all converge at DAC.

The technical conference introduces DAC's new User Track – a three-day track of over 80 papers and posters that are written by, selected by, and targeted at users of design tools. In the User Track, attendees will learn from their colleagues in leading-edge design organizations about the latest solutions to critical design and methodology challenges.

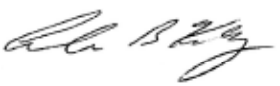
DAC's exhibition will again showcase approximately 200 companies, including all of the largest EDA vendors. The Exhibitor Forum theater returns with a full three-day schedule of focused technical presentations from exhibitors. The Best of DAC Contest also returns with additional Attendees' Choice categories: this year, you can vote on the web for your favorite vendors and new products. New this year in the exhibition is IC Design Central – a cluster of exhibitors and a presentation theater that brings together the entire ecosystem for SOC enablement. IP providers, design service providers, and foundry service providers can all be found in the ICDC.

DAC is also the meeting place for many EDA- and design-related organizations, workshops and events. Who meets at DAC? Standards bodies, such as Accellera and Si2. Road mapping efforts, such as the ITRS Design Technology working group. Established symposia, such as SASP, NANOARCH, MSE, SLIP, DFM&Y, and HOST. Workshops on topics ranging from UML to low-power design to bio-design automation. A total of 18 workshops and colocated events will take place at DAC.

DAC 2009 is proud to present a stellar lineup of keynote and plenary sessions. In response to the recent upheavals in the macro economy as well as in the IC design and design automation industries, DAC will open its program with a special Monday afternoon panel that brings together the CEOs of the leading EDA companies. Attendees will hear our industry leaders' views on market, business and technology futures, as well as the overall outlook for the EDA industry. DAC is also proud to present keynote presentations from outstanding industry leaders: Fu-Chieh Hsu, Vice President, Design and Technology Platform, TSMC; and William Dally, Chief Scientist, NVIDIA and Willard R. and Inez Kerr Bell Professor of Computer Science at Stanford University. Finally, a plenary panel on Thursday, moderated by Walden C. Rhines of Mentor Graphics Corp. will address the questions of "How Green is My Silicon Valley" and what 'green' means for our industry.

On behalf of DAC's sponsoring organizations and the many hundreds of volunteers who make DAC happen each year, I warmly invite you to join us in San Francisco this coming July.

Best regards,



Andrew B. Kahng

General Chair, 46th DAC

DESIGN **AUTOMATION** CONFERENCE

NEW to DAC: User Track

Tuesday, Wednesday, and Thursday

The presentations in the all-new User Track focus on problems that design practitioners face every day. The presentations run in parallel with the regular paper sessions. The User Track program includes front-end sessions, back-end sessions, and a poster session.

The front-end sessions have 16 presentations that focus on a number of themes that enhance system-level design productivity. Specific topics include power management modeling and simulation techniques, verification of power management techniques and embedded device drivers, several perspectives on the use of high-level languages, loosely- and approximately-timed switchable models and methodologies for architecture-level prototyping and design space exploration. The speakers include users from Infineon Technologies AG, Cisco Systems, Inc., Texas Instruments, Inc., Xilinx, Inc., STMicroelectronics, Intel Corp., Virtutech, ClueLogic, and other companies.

The back-end sessions have 26 presentations addressing the following questions: How do I stitch last week's ECOs back into my design? How do I analyze power supply and substrate noise effectively for large chips? How do I mix transistor- and gate-level timing analyses, and add statistical timing to this? How do I bring more automation to the analog and mixed-signal domain? Can I improve productivity by designing portable libraries and advanced analog verification methodologies? Answers to these questions and many more will be presented by users from STMicroelectronics, Samsung, Qualcomm, Inc., Intel Corp., Fujitsu Labs, IBM Corp., Sun Microsystems, Inc., and other companies.

The poster session includes approximately 40 posters on topics that span both front-end and back-end design. The posters will offer an opportunity for personal interaction with EDA tool users from many leading companies. An Ice Cream Social will be held in conjunction with the poster session on Wednesday from 1:30 - 3:00pm on the Concourse Level.

Sponsored by: cadence™

User Track Sessions

Robust Design and Test
Tuesday, July 28, 10:30am - 12:00pm

Practical Physical Design
Tuesday, July 28, 2:00 - 4:00pm

Verification: A Front-End Perspective
Tuesday, July 28, 4:30 - 6:00pm

Timing Analysis in the Real World
Wednesday, July 29, 9:00 - 11:00am

Towards Front-End Design Productivity
Wednesday, July 29, 3:00 - 4:00pm

Front-End Development: Embedded Software and Design Exploration
Wednesday, July 29, 4:30 - 6:00pm

Power Analysis and IP Reuse
Thursday, July 30, 9:00 - 11:00am

Front-End Power Planning and Analysis
Thursday, July 30, 2:00 - 4:00pm

Advances in Analog and Mixed-Signal Design
Thursday, July 30, 4:30 - 6:00pm

Keynote Panel: Futures for EDA: The CEO View

Monday, July 27, 4:30 - 5:45pm

Aart de Geus
CEO and Chairman of the Board Synopsys, Inc.

Walden C. Rhines
CEO and Chairman of the Board Mentor Graphics Corp.

Lip-Bu Tan
President and CEO Cadence Design Systems, Inc.

The IC design and EDA ecosystem has witnessed a number of structural and financial upheavals in recent years. Perennial challenges—new technologies and markets, R&D investment levels, business and revenue models, and interoperability—are magnified by the current economic downturn. This year, DAC will open its program with a special Monday afternoon panel that brings together the CEOs of the leading EDA companies. The panelists will give their views on market, business and technology futures, as well as the overall outlook for the EDA industry.

Keynote: Overcoming the New Design Complexity Barrier: Alignment of Technology and Business Models

Tuesday, July 28, 8:30 - 10:15am

Fu-Chieh Hsu
Vice President, Design and Technology Platform, Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, Taiwan

The semiconductor industry today faces a new design complexity barrier. Convergence of product features brings unprecedented complexities on process technology, architectural and gate-count. Integration and cost drivers bring 3-D stacking with through-silicon vias. Heterogeneity brings high-voltage devices, image sensors, and MEMS into a single product design optimization. From IP migration, to variability modeling and mitigation, to NRE cost, the new paradigm is that these are no longer discrete issues addressable by point-tool solutions. Overcoming this new design complexity barrier requires breakthrough technologies and integrated EDA solutions.

Funding the development of new EDA solutions must make business sense. But while traditional ROI assessments are based on "one company-centric" business models, the next stage of the industry's evolution requires ROI and business models that acknowledge coexistence, and even collaboration, of multiple companies. This is especially true during this unprecedented worldwide financial earthquake. A win-win-win future will depend on the emergence of an innovative business model that is realized collaboratively by key players across the IC design and manufacturing ecosystem. Fortunately, recent initiatives have the promise to meet this need.

Keynote: The End of Denial Architecture and the Rise of Throughput Computing

Wednesday, July 29, 11:15am - 12:15pm

William J. Dally
Chief Scientist and Senior Vice President of Research, NVIDIA Corp., Santa Clara, CA,
Willard R. and Inez Kerr Bell Professor of Engineering, Stanford Univ., Palo Alto, CA

Throughput-optimized processors, such as graphics processing units (GPUs) have scaled at historic rates in recent years, and continue to do so along a design trajectory that is largely unhindered by conventional dogmas and legacies. These processors recognize that two critical aspects of machine organization are key to performance: parallel execution and hierarchical memory organization. Conventional processors, which present an illusion of sequential execution and uniform, flat memory, find their performance increasing only slowly over time, and their evolution is at an end. In contrast, throughput processors embrace, rather than deny, parallelism and memory hierarchy to realize large performance and efficiency advantages. Throughput processors have hundreds of cores today and will have thousands of cores by 2015. They will deliver most of the performance, and most of the user value, in future computer systems.

This talk will discuss some of the challenges and opportunities in the architecture and programming of future throughput processors, as it relates to the EDA world. First, CAD tools, flows, and methodologies are clearly crucial to the design of these processors, and these must adapt to support such designs. Second, in this changing landscape, CAD tools must need to evolve to run on throughput processors. In throughput processors, performance derives from the parallelism available from the plentiful arithmetic units, and efficiency derives from locality, overcoming restrictions stemming from communication bandwidth bottlenecks that dominate cost, performance, and power. This talk will discuss exploitation of parallelism and locality with examples drawn from the Imagine and Merrimac projects, from NVIDIA GPUs, and from three generations of stream programming systems.

Special Plenary Panel: How Green Is My Silicon Valley

Thursday, July 30, 12:00 - 1:45pm

There has been a lot of talk about 'green' technology, and how it can save our economy and the electronics industry. But what is really being done about it in Silicon Valley—the spawning ground for all things high-tech?

This panel of experts—drawn from technology heavyweights, governmental agencies, venture capitalists and start-ups—will give their views on what 'green' means for our industry. For some, it means low-power chip and system design. Others focus on completely new solutions that go well beyond traditional electronics to help lower our collective carbon footprint. Green also means leverage of existing technologies in new eco-friendly applications ranging from water management to smokestack emission monitoring.

Innovation is the only answer to this, the preeminent challenge of the 21st century. And innovation is what Silicon Valley and the global high-tech industry are all about. Come hear the best and brightest talk about their favorite new color and how it will take our industry and the larger economy into a brighter, more sustainable future.

Chair: **Walden C. Rhines**, EDA Consortium Chair - Mentor Graphics Corp.

Technical Program Highlights

Six hundred and eighty-two (682) regular papers were submitted (a seven percent jump from last year's 639 papers) and 22% were accepted. Areas with highest submission numbers are:

- System-level design and codesign (87 papers were submitted; accepted papers will be presented in five sessions)
- Power analysis and low-power design (83 papers were submitted; four sessions)
- Physical design and manufacturability (82 papers were submitted; four sessions)
- High-level and logic synthesis (54 papers were submitted; three sessions)

In addition to regular paper sessions, DAC's technical program consists of Special Sessions, Panels, Tutorials, Workshops, and Colocated Events. The introduction of the User Track, with its emphasis on design methodology and tool flows, is new this year. The User Track had 117 submissions, and the accepted papers will be presented in nine sessions (five for the front end, four for the back end) as well as in a new poster session on Wednesday afternoon.

Special Sessions will deal with a wide variety of themes such as preparing for design at 22nm, designing circuits in the face of uncertainty, verification of large, systems-on-chip, bug-tracking in complex designs, novel computation models, multicore computing and the impact of data centers on computing and EDA. The special sessions continue to include WACI (Wild and Crazy Ideas)—forward-looking and innovative ideas that are typically less developed than regular papers.

Technical Panels present the hottest issues of our industry and will cover:

- Technical discussions on system prototyping, embedded software design, mixed signal verification, system-level power challenges, design for manufacturability, emerging applications of EDA technology, and the previously-noted special plenary panel, "How Green is My Silicon Valley".
- Management-focused topics such as costs of scaling, careers in EDA, and the return of the CEO panel.

The program also features six Full-day Tutorials on timely subjects ranging from parallel programming and its application to CAD tools, high-level synthesis, post-silicon validation, functional verification, low-power design in the wireless space, and the future of circuits based on emerging nanodevices.

Panels

System Prototypes: Virtual, Hardware or Hybrid?
Tuesday, July 28, 10:30am - 12:00pm

EDA in Flux—Should I Stay or Should I Go?
Tuesday, July 28, 2:00pm - 4:00pm

Moore's Law: Another Casualty of the Financial Meltdown?
Tuesday, July 28, 4:30pm - 6:00pm

DFM—Band-Aid or Competitive Weapon?
Wednesday, July 29, 9:00am - 11:00am

Oil Fields, Hedge Funds and Drugs
Wednesday, July 29, 2:00pm - 4:00pm

Guess, Solder, Measure, Repeat—How Do I Get My Mixed-Signal Chip Right?
Wednesday, July 29, 4:30pm - 6:00pm

From Milliwatts to Megawatts: The System-Level Power Challenge
Thursday, July 30, 2:00pm - 4:00pm

The Wild West: Conquest of Complex Hardware-Dependent Software Design
Thursday, July 30, 4:30pm - 6:00pm

Management Day

Sponsored by: cadence™

Tuesday, July 28, 10:30am - 6:00pm

The DAC 2009 Management Day provides managers with timely information to help them make decisions where business and technology intersect. This is a unique opportunity for managers to gain insights from their peers in the industry.

Today's complex SOCs require different types of optimizations and the adoption of emerging solutions to meet stringent design requirements. Optimizing for volume production, low-power, and shrinking sizes necessitates accurate trade-off analysis and technical/business decision-making by management. Moreover, moving to new semiconductor technology nodes, such as 28nm or 40nm, can significantly affect the choices of suppliers.

The three sessions in this year's Management Day will discuss these changing needs and present corresponding management decision criteria that allow managers to make the right choices from a pool of alternate options for flows, methodologies and suppliers. The first two sessions will feature presentations by managers representing independent device manufacturers (IDMs), fab-light ASIC providers and fabless companies.

Senior managers of today's most complex nanometer chips—from Intel Corp., Advanced Micro Devices, Inc., STMicroelectronics, Freescale Semiconductor, Inc., and other leading companies—will discuss the latest and emerging solutions, along with their economic impact. The third session will be a panel that will involve the presenters and the audience in an open brainstorming discussion.

Special Sessions

Mechanisms for Surviving Uncertainty: Opportunities and Prospects
Tuesday, July 28, 10:30am - 12:00pm

Dawn of the 22nm Design Era - Yes We Can!
Tuesday, July 28, 2:00pm - 4:00pm

Verifying an SOC Monster: Whose Job Is It Anyway?
Tuesday, July 28, 4:30pm - 6:00pm

Emerging Technologies: Blue-Sky Research or CMOS Replacement?
Wednesday, July 29, 9:00am - 11:00am

Computation in the Post-Turing Era
Wednesday, July 29, 2:00pm - 4:00pm

Multicore Computing and EDA
Wednesday, July 29, 4:30pm - 6:00pm

WACI: Wild and Crazy Ideas
Thursday, July 30, 9:00am - 11:00am

The Tool Shows That My Design Is Wrong, But Where Is the Bug?
Thursday, July 30, 9:00am - 11:00am

Technologies for Green Data Centers
Thursday, July 30, 4:30pm - 6:00pm

Pavilion Panels

Gary Smith on EDA: Trends and What's Hot at DAC
Monday, July 27, 9:30 - 10:30am

EDA Heritage Series: Doug Fairbairn's Industry Retrospective
Monday, July 27, 10:45 - 11:45am

Hogan's Heroes: The Long Road to System-Level Sign-Off
Monday, July 27, 1:00 - 2:00pm

IP at Risk: Protecting the Company Jewels
Monday, July 27, 2:30 - 3:15pm

A Conversation with the 2009 Marie R. Pistilli Award Winner
Monday, July 27, 3:30 - 4:30pm

DAC/ISSCC Student Design Contest Awards Presentation
Monday, July 27, 5:00 - 6:00pm

Fighting Piracy on the High Seas: Offense vs. Defense
Tuesday, July 28, 10:30 - 11:15am

Low-Power: Consumer Electronics' Catch-22
Tuesday, July 28, 11:30am - 12:15pm

Town Hall Meeting: Can We Afford for Start-Ups to Wind Down?
Tuesday, July 28, 1:00 - 2:00pm

Will Interoperable PDKs Fly in a Stodgy Analog World?
Tuesday, July 28, 2:30 - 3:15pm

Embedded Multicore: Multi-Opportunities, Multi-Challenges
Tuesday, July 28, 3:30 - 4:15pm

EDA Ecosystem: In Sync or Out of Touch?
Tuesday, July 28, 4:30 - 5:15pm

Community-Directed Panel: It's All about U(ser)
Wednesday, July 29, 10:00 - 10:45am

Electronics Going Green: Future or Futile?
Wednesday, July 29, 12:30 - 1:30pm

Seeking the Holy Grail of Verification Coverage Closure
Wednesday, July 29, 2:00 - 2:45pm

The AMS Revival: Bipolar Thinking?
Wednesday, July 29, 3:00 - 3:45pm

Tweet, Blog or News: How Do I Stay Current?
Wednesday, July 29, 4:00 - 5:00pm

Reuse in an Enterprise: Myth or Reality?
Wednesday, July 29, 5:15 - 6:00pm

You Don't Know Jack—High Schoolers Tell You What's Up with Technology
Thursday, July 30, 10:00 - 11:15am

Exhibitor Forum

DAC is continuing the popular Exhibitor Forum again this year. The Exhibitor Forum provides a theatre on the exhibit floor where exhibitors present focused, practical technical content to attendees. The presentations are selected by an all-user Exhibitor Forum Committee chaired by Magdy Abadir of Freescale Semiconductor, Inc. Each session is devoted entirely to a specific domain (e.g. verification, system-level design, etc.), with three companies presenting per session, followed by a brief question and answer period. The Exhibitor Forum provides exhibitors and attendees with a great way to meet each other, and is yet another way that DAC adds opportunities to deliver practical "how-to" information and introductions to new technologies on the exhibit floor.

The IC Design Central Partner Pavilion—Putting More Design Into DAC

The IC Design Central Partner Pavilion brings together vendors supplying products and services that address many of the critical design functions necessary to produce working silicon on time and on budget. Companies from all areas of the design and product development process—EDA, Foundry, IP, Design Services, Assembly/Package, Test, and System Interconnect—must cooperate to offer integrated front-to-back solutions that ensure first-time-successful silicon and predictable time-to-market. Visit the ICDC Partner Pavilion and find design flows and solutions needed to create today's challenging designs.

The ICDC Partner Pavilion is a combination of exhibit booths and 30-minute presentations by each participating vendor. The combination of product displays in the exhibits and technical product presentations in the ICDC Theater offers attendees an in-depth look into flows and methodologies from vendors featuring a variety of products and services for the entire design ecosystem.

Current participating exhibitors include:

- Amiq Consulting S.R.L.
- Ateeda Limited
- Blue Pearl Software
- Cadence Design Systems, Inc.
- Cambridge Analog Technologies, Inc.
- Chipworks
- CSMC Technologies Corporation
- Epoch Microelectronics, Inc.
- Fidus Systems Inc.
- iNoCs
- Warthman Associates

DAC Workshops

6th UML - SOC at 46th DAC
Sunday, July 26, 9:00am - 5:00pm

Multiprocessor System-On-Chip: Current Trends and the Future
Sunday, July 26, 8:00am - 5:00pm

Moving from Traditional to Equation-Based DRC
Sunday, July 26, 2:00 - 5:30pm

Meeting the Challenges of ESD/ERC in a Mixed-Signal World
Sunday, July 26, 2:00 - 5:30pm

International Workshop on Bio-Design Automation
Monday, July 27, 8:00am - 6:00pm

Workshop for Women in Design Automation (WWINDA): Career Crossroads—Who Has the Map?
Monday, July 27, 9:00am - 1:45pm

Young Faculty Workshop
Monday, July 27, 9:00am - 5:00pm

Virtual Platform Workshop at DAC
Wednesday, July 29, 9:00am - 5:30pm

Monday Tutorials

8:30am - 4:30pm

Tutorial 1:
Low-Power SOC Design: State of the Art and Directions

Tutorial 2:
High-Level Synthesis for ESL Design: Fundamentals and Case Studies

Friday Tutorials

9:00am - 5:00pm

Tutorial 3:
Post-Silicon Validation and Runtime Verification: Ensuring Correctness after First Silicon

Tutorial 4:
CAD: Utilizing the State of the Art, and Beyond, in Parallel Programming

Tutorial 5:
From Nanodevices to Nanosystems: Promises and Challenges of IC Design with Nanomaterials

Tutorial 6:
Functional Verification Planning and Management: Navigating from Specification to Functional Closure

Colocated Events

The International Conference on Microelectronic Systems Education
Saturday, July 25 - Monday, July 27, San Francisco Marriott

Events held at the Moscone Convention Center:

Design Automation Summer School 2009
Saturday, July 25 and Sunday, July 26

3rd IEEE International Workshop on Design for Manufacturability and Yield (DFM&Y)
Sunday, July 26

SLIP 2009: International Workshop on System-Level Interconnect Prediction
Sunday, July 26

7th IEEE Symposium on Application Specific Processors
Monday, July 27 and Tuesday, July 28

2nd IEEE International Workshop on Hardware-Oriented Security and Trust (HOST 2009)
Monday, July 27

Design for Manufacturability Workshop: DFM Challenges at Sub-45nm Design
Monday, July 27

Low-Power Coalition Workshop: Advances in Low-Power Design Throughout the Design Flow
Sunday, July 26

North American SystemC Users Group 11th NASCUG Meeting
Monday, July 27

NASA/ESA Conference on Adaptive Hardware and Systems (AHS 2009)
Wednesday, July 29 - Saturday, August 1

IEEE/ACM Symposium on Nanoscale Architectures
Thursday, July 30 and Friday, July 31

Detailed conference and exhibition information is now available online: www.dac.com. Register today! QUESTIONS? Call +1-303-530-4333

Exhibition

The 46th DAC exhibition is located in the North and South Halls of the Moscone Center. Visit the DAC exhibition to learn in-depth about new products and services from nearly 200 vendors, spanning all aspects of the electronic design process including EDA tools, IP cores, embedded system and system-level tools, as well as silicon foundry and design services.

The DAC Exhibition Features:

The Best of DAC Exhibits contest! Vote for your favorite vendors, new products, and Pavilion Panel from your laptop or any DACnet terminal, at www.dac.com. When you cast your ballot, you will be entered in a drawing for an iPod Touch!

Exhibitor Forum Attendees are invited to the Exhibitor Forum, in the North Hall in Booth 4359, to hear a series of technical presentations from exhibitors on focused topics.

DAC Pavilion The popular DAC Pavilion is located in the South Hall in Booth 1928. This year, the Pavilion will feature 19 presentations on business and technical issues.

New! IC Design Central Partner Pavilion DAC's new and innovative feature for exhibit floor education is located in the North Hall. Come see presentations on how specific exhibitors are solving your design issues with their latest tools and methodologies.

Exhibit-Only Pass Register for an exhibits-only pass and receive admission to all days of the exhibition, all Keynotes, all DAC Pavilion and Exhibitor Forum sessions, plus the new IC Design Central Partner Pavilion—all for $50 when registered by June 29.

Exhibition Hours

Monday, July 27 - Wednesday, July 29 9:00am - 6:00pm

Thursday, July 30 9:00am - 1:00pm

EXHIBITING COMPANIES

Accelicon Technologies, Inc.
ACCIT - New Systems Research
ACE Associated Compiler Experts bv
*Achilles Test Systems, Inc.
*Agnisys Inc.
Altos Design Automation
Amiq Consulting S.R.L.
Analog Bits Inc.
Analog Rails
Apache Design Solutions, Inc.
Applied Simulation Technology
Artwork Conversion Software, Inc.
*Ateeda Limited
Atoptech
Atrenta Inc.
austriamicrosystems
AutoESL Design Technologies, Inc.
Avery Design Systems, Inc.
Axilica Ltd.
Axiom Design Automation
Berkeley Design Automation, Inc.
Blue Pearl Software
Bluespec, Inc.
Breker Verification Systems
Cadence Design Systems, Inc.
Cadence Design Systems, Inc.
Calypto Design Systems
*Cambridge Analog Technologies, Inc.
CAST, Inc.
ChipEstimate.com
ChipVision Design Systems
*Chipworks
Ciranova, Inc.
ClioSoft, Inc.
CLK Design Automation, Inc.
CMP
CoFluent Design
Concept Engineering GmbH
Coupling Wave Solutions
CoWare, Inc.
*CSMC Technologies Corporation
*CST of America, Inc.
DAC Pavilion
DAFCA, Inc.
Dassault Systemes ENOVIA Corp.
Dataram
DATE 2010
Denali Software, Inc.
*Desaut Inc.
Design and Reuse
Dini Group
*DOCEA Power
Dolphin Integration
Duolog Technologies Ltd.
Dynalith Systems Co., Ltd.
EDA Cafe-IB Systems
EDXACT SA
Elsevier
EMA Design Automation, Inc.
Entasys Design, Inc.
*Epoch Microelectronics, Inc.
EVE
Exhibitor Forum
Extension Media - Chip Design
Extreme DA
*Fidus Systems Inc.
FishTail Design Automation, Inc.
Forte Design Systems
FTL Systems, Inc.
GateRocket, Inc.
GiDEL
Gradient Design Automation
Helic S.A.
Hewlett-Packard Co.
IC Manage, Inc.
IMEC / Europractice
Imera Systems, Inc.
Incentia Design Systems, Inc.
Infiniscale
*Innovative Logic Inc.
iNoCs
Instigate
InternetCAD.com, Inc./Timberwolf Systems
Interra Systems, Inc.
Jasper Design Automation, Inc.
Jspeed Design Automation, Inc.
Kilopass Technology, Inc.
Laflin HOTSCOPE
Legend Design Technology, Inc.
Library Technologies, Inc.
LogicVision, Inc.
Lynguent, Inc.
Magillem Design Services
Magma Design Automation, Inc.
Magwel NV
MathWorks, Inc. (The)
McGraw-Hill Professional
Mentor Graphics Corp.
*Mephisto Design Automation
*Methodics LLC
Micro Magic, Inc.
Micrologic Design Automation
Mirabilis Design Inc.
Mixel, Inc.
MOSIS Service (The)
MunEDA GmbH
Nangate
Nusym Technology, Inc.
Oasys Design Systems, Inc.
OneSpin Solutions GmbH
OptEM Engineering Inc.
*Optiwave Systems Inc.
Orora Design Technologies, Inc.
*OVM World
Penton Media - Electronic Design Group
Pextra
Physware, Inc.
PLD Applications (PLDA)
POLYTEDA Software Corp.
Prentice Hall Prof. / Pearson Education
Prolific, Inc.
Pulsic Ltd.
QThink, Inc.
*R3 Logic Inc.
Real Intent, Inc.
Reed Business Information
Runtime Design Automation
Sagantec
Satin IP Technologies
Seloco, Inc.
Semifore, Inc.
Sequence Design, Inc.
Shearwater Group, Inc. (The)
Si2
SIGDA/DAC University Booth
Sigrity, Inc.
Silicon Design Solutions
Silicon Frontline Technology
Silicon Image
SoftJin Technologies
Sonnet Software, Inc.
Spatial
Springer
SpringSoft, Inc.
StarNet Communications
*Summit Exec, Inc.
Synapse Design Automation
Synchronicity - see Dassault Systèmes
Synopsys, Inc.
Synopsys, Inc. - Common Platform Partner
Synopsys, Inc. - Standards Booth
SynTest Technologies, Inc.
Takumi Technology Corp.
Tanner EDA
Target Compiler Technologies NV
TeamEDA
Tech Source Media, Inc./SCDSource
TechForce, Inc.
Teklatech
Tela Innovations
The RTC Group
Time To Market Inc.
TOOL Corp.
True Circuits, Inc.
TSMC
TSSI - Test Systems Strategies, Inc.
Tuscany Design Automation, Inc.
Uniquify, Inc.
Univa UD
Verific Design Automation
Veritools, Inc.
ViASIC Inc.
*Warthman Associates
*Weiguang Electronics Technology Co., Ltd.
WinterLogic Inc.
XYALIS
Z Circuit Automation, Inc.
Zeland Software, Inc.

(as of May 6, 2009)
* - indicates first time exhibitor

WORKSHOPS

Sunday, July 26

Moving from Traditional to Equation-Based DRC
2:00 - 5:30pm - $80 (Member), $110 (Non-Member)

Meeting the Challenges of ESD/ERC in a Mixed-Signal World
2:00 - 5:30pm - $80 (Member) $110 (Non-Member)

Multiprocessor System-On-Chip: Current Trends and the Future
8:00am - 5:00pm - $150 (Member), $195 (Non-Member)

6th UML-SOC at 46th DAC
9:00am - 5:00pm - $250 (Member), $295 (Non-Member)

Monday, July 27

Workshop for Women in Design Automation (WWINDA): Career Crossroads - Who Has the Map?
9:00am - 1:45pm - $75 (Member), $100 (Non-Member)

Young Faculty Workshop
9:00am - 5:00pm - $150 (Member), $195 (Non-Member)

International Workshop on Bio-Design Automation
8:00am - 6:00pm - $150 (Member), $195 (Non-Member)

Wednesday, July 29

Virtual Platform Workshop at DAC
9:00am - 5:30pm - $150 (Member), $195 (Non-Member)

COLOCATED EVENTS

3rd IEEE International Workshop on Design for Manufacturability and Yield (DFM&Y)
Sunday, July 26, 9:00am - 5:00pm

	By June 29, 2009	After June 29, 2009
Member, ACM or IEEE	$200	$250
Non-Member	$250	$300
Students with ACM or IEEE membership	$150	$180
Student Non-Member	$200	$250

Low-Power Coalition Workshop: Advances in Low-Power Design Throughout the Design Flow
Sunday, July 26, 1:00 - 3:30pm - FREE

SLIP 2009: International Workshop on System-Level Interconnect Prediction
Sunday, July 26, 8:45am - 6:30pm

	By June 29, 2009	After June 29, 2009
Member, ACM or IEEE	$250	$300
Non-Member	$320	$380
Students with ACM or IEEE membership	$200	$250
Student Non-Member	$250	$300

Design for Manufacturability Workshop - DFM Challenges at Sub-45nm Design
Monday, July 27, 1:00 - 3:00pm - FREE

2nd IEEE International Workshop on Hardware-Oriented Security and Trust (HOST 2009)
Monday, July 27, 7:30am - 6:00pm

	By June 29, 2009	After June 29, 2009
Member, ACM or IEEE	$200	$250
Non-Member	$250	$320
Students with ACM or IEEE membership	$150	$200
Student Non-Member	$200	$250

7th IEEE Symposium on Application Specific Processors (SASP)
Monday, July 27 8:30am - 5:00pm and Tuesday, July 28, 11:00am - 5:00pm

	By June 29, 2009	After June 29, 2009
Member, ACM or IEEE	$315	$420
Non-Member	$410	$530
Students with ACM or IEEE membership	$190	$245
Life/Retired Member Fees	$190	$245

NASA/ESA Conference on Adaptive Hardware and Systems (AHS 2009)
Wednesday, July 29 - Saturday, August 1, 8:00am - 7:00pm

	By June 29, 2009	After June 29, 2009
Full Conference	$740	$870
Student Registration	$590	$690

IEEE/ACM Symposium on Nanoscale Architectures
Thursday, July 30 and Friday, July 31, 8:00am - 6:00pm

	By June 29, 2009	After June 29, 2009
Member, ACM or IEEE	$250	$300
Non-Member	$330	$380
Student	$200	$220

Register Online by June 29 and Save!

Register online: Internet registration is open through July 31, 2009. Mail/Fax registrations not accepted after July 17. Register by June 29, 2009 and SAVE!

- **Exhibit-Only** registration includes access to all four days of the exhibition, all Keynotes, and all DAC Pavilion, Exhibitor Forum and ICDC Partner Pavilion presentations.
- **Full Conference** includes all three days of the Technical Conference, all Keynotes, User Track sessions, access to the Exhibition, Monday through Thursday, and the "46 Years of DAC" DVD Proceedings.
- **Student** includes all three days of the Technical Conference, all Keynotes, User Track sessions, access to the Exhibition, Monday through Thursday, and the "46 Years of DAC" DVD Proceedings.
- **One-Day or Two-Day** includes the day(s) you select for the Technical Conference, User Track sessions on the day(s) attending, all Keynotes, access to the Exhibition, Monday through Thursday, and the "46 Years of DAC" DVD Proceedings.
- **Full-Day Tutorials** are offered on Monday, July 27 and Friday, July 31. You must register for at least one day of the Technical Conference to attend tutorials. Tutorial registration fee includes: continental breakfast, lunch, coffee breaks, and tutorial notes.
- **Management Day:** Registration for this event includes entrance to the Exhibition, Monday through Thursday, and all Keynotes.
- **User Track:** Registration for this event includes entrance to the Exhibition, Monday through Thursday, and all Keynotes.

CONFERENCE	**Received by June 29, 2009**	**After June 29, 2009 or at the conference**
Member, ACM or IEEE	$410	$500
Non-Member	$510	$625
Students with ACM or IEEE membership	$225	$285
One-Day Only *(Tuesday, Wednesday, Thursday)*	$260	$260
Two-Day Only *(Tuesday, Wednesday, Thursday)*	$470	$470
EXHIBIT-ONLY Exhibit-Only (access all days)	$50	$95
MANAGEMENT DAY	$95	$95
USER TRACK Member	$175	$175
USER TRACK Non-Member	$225	$225

TUTORIALS	**Member, ACM or IEEE**	**Non-Member**	**Student**
Full-Day Tutorials	$300 (per tutorial)	$400 (per tutorial)	$200 (per tutorial)

Visit the DAC website for online registration, complete conference and exhibition details, travel and hotel reservations, and San Francisco information at www.dac.com.

Refund Policy: Written requests for cancellations must be received in the DAC office by June 29, 2009, and are subject to a $25 processing fee. Cancellations received after June 29, 2009, will NOT be honored and all registration fees will be forfeited. **No faxed or mailed registrations will be accepted after July 17, 2009.**

TELEPHONE REGISTRATIONS ARE NOT ACCEPTED!

Faxed or mailed registrations without payment will be discarded.

46th Design Automation Conference
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www.dac.com