REGISTER TODAY!

Register on-line: Internet registration is open through June 12. Mail/Fax registrations not accepted after May 28. Register by May 19 and Save!

- Exhibit-Only includes entrance to the Exhibition, Monday through Thursday, and all Keynotes. ***FREE with advance registration, until May 19.***
- Full Conference includes all three days of the Technical Conference, access to the Exhibition, Monday through Thursday, and the "45 Years of DAC" DVD Proceedings, plus a ticket to the Wednesday Night Party.
- Student includes all three days of the Technical Conference, access to the Exhibition, Monday through Thursday, and the "45 Years of DAC" DVD Proceedings, plus a ticket to the Wednesday Night Party.
- One-/Two-Day includes the day(s) you select for the Technical Conference, access to the Exhibition, Monday through Thursday, and the "45 Years of DAC" DVD Proceedings.
- Full-Day Tutorials are offered on Monday, June 9 and Friday, June 13. You must register for at least one day of the Technical Conference to attend tutorials. Tutorial registration fee includes continental breakfast, lunch, coffee breaks, and tutorial notes.
- Hands-on Tutorials are three-hour tutorials featuring hands-on software tools from DAC exhibitors. Attendees must register for a minimum of an Exhibit-Only registration in order to be eligible to attend Hands-on Tutorials. Due to the proprietary nature of the discussions, presenting companies have the right to refuse access to employees or contractors of competitors. Space is limited.
- Management Day: Registration for this event includes entrance to the Exhibition, Monday through Thursday, and all Keynotes.

Register on-line through June 12, 2008

CONFERENCE	Received by May 19, 2008	After May 19, 2008, or at the conference
Member, ACM or IEEE	$450	$565
Non-Member	$585	$735
Students with ACM or IEEE membership	$195	$195
One-Day Only *(Tues., Wed., Thur.)*	$260	$260
Two-Day Only *(Tues., Wed., Thur.)*	$470	$470
EXHIBIT-ONLY		
Exhibit-Only (access all days)	Free	$65

TUTORIALS	Member, ACM or IEEE	Non-Member	Student
Full-Day Tutorials	$310 (per tutorial)	$400 (per tutorial)	$125 (per tutorial)
Hands-on Tutorials	$75 (per tutorial)	$75 (per tutorial)	$75 (per tutorial)
MANAGEMENT DAY:	$95		$95

Visit the DAC website for on-line registration, complete conference and exhibition details, travel and hotel reservations, and Anaheim information at www.dac.com.

Refund Policy: Written requests for cancellations must be received on or before May 19, 2008, and are subject to a $25 processing fee. Cancellations after May 19, 2008, will NOT be honored and all registration fees will be forfeited. No faxed or mailed registrations will be accepted after May 28, 2008.

TELEPHONE REGISTRATIONS ARE NOT ACCEPTED!

Faxed or mailed registrations without payment will be discarded.

WORKSHOPS

Sunday, June 8

High-level Synthesis: Back to the Future - ***$100 (Member), $150 (Non-Member)***

5th International UML for SoC Design - UML in Application
$100 (Member) $150 (Non-Member)

Biochips to Interface and Monitor Human Biological Functions
$100 (Member), $150 (Non-Member)

System and SoC Debug Workshop - ***$100 (Member), $150 (Non-Member)***

Design and Verification of Low Power SoCs: An Application Oriented Approach
$75 (Member), $100 (Non-Member)

Low Power Coalition Workshop - Advances in Low Power Design for Circuits and Systems
$75 (Member), $100 (Non-Member)

Monday, June 9

Cross-layer Power and Thermal Management - ***$100 (Member), $150 (Non-Member)***

Diagnostic Services in Network-on-Chips (DSNOC) - ***$100 (Member), $150 (Non-Member)***

Introduction to Chips and EDA for a Non-technical Audience - ***$10***

Workshop for Women in Design Automation (WWINDA) – Networking, Negotiation, & Nonsense: Achieving Career Balance in an Unbalanced World - ***$50 (Member), $75 (Non-Member)***

4th Integrated Design Systems Workshop DAC 2008 - OpenAccess: A Platform for Continuous Evolution and Innovation- ***$100 (Member), $150 (Non-Member)***

Beyond Syntax and Semantics: Industry Experiences with OVL/SVA/PSL
$75 (Member), $100 (Non-Member)

Tuesday, June 10

Effective Technical Writing - ***$50 (Member), $75 (Non-Member)***

iDesign Track: Tuesday Keynote, Sessions 1, 7 and 13 - ***$95***

Thursday, June 12

Maximizing Efficiency in the Development Cycle
$50 (Member), $75 (Non-Member)

Collocated Events

MEMOCODE 2008: June 5-7, 2008, Anaheim Convention Center, 8:00am-5:00pm
Register at: http://svl1.cs.pdx.edu/memocode08/

6th IEEE Symposium on Application Specific Processors:
June 8-9, 2008, Anaheim Convention Center, 8:30am-6:30pm

	By May 19, 2008	After May 19, 2008
Member, ACM or IEEE	$325	$410
Non-Member	$410	$525
Students with ACM or IEEE membership	$195	$245

IEEE International Workshop on Hardware-oriented Security and Trust (HOST-2008):
June 9, 2008, Anaheim Convention Center, 8:30am-5:30pm
$100 (Member), $150 (Non-Member)

NANOARCH'08: 4th IEEE/ACM International Symposium on Nanoscale Architectures
June 12-13, 2008, Anaheim Convention Center, 9:00am-5:00pm

	By May 19, 2008	After May 19, 2008
Member, ACM or IEEE	$250	$300
Non-Member	$330	$380
Students with ACM or IEEE membership	$200	$220

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DAC: Where The Electronic Design Community Meets…

Dear Colleague:

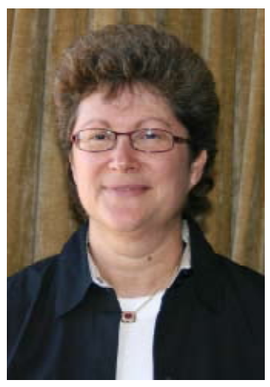
DAC is the premier event for the electronic design community. It offers the industry's most prestigious technical conference in combination with the biggest exhibition, and brings together design, design automation and manufacturing market influencers. Industry leaders, market leaders, technical leaders, business leaders and thought leaders all converge at DAC.

DAC is also the meeting place for many related organizations, such as standards bodies, including Accellera and Si2, and consortia that include SRC and Focus Centers such as GSRC. Each year more organizations associate themselves with DAC – the conference this year has attracted a record number of additional events. In particular, one adjunct event, five collocated events and fourteen workshops are taking place during DAC that include the Global STC Conference, GSRC, MEMOCODE, NANOARCH, SASP, and HOST.

This year, DAC's exhibition will include several new features: register before May 19 and attend all four days of the exhibition at no cost; visit the new Exhibitor Forum theater to see a series of focused technical presentation sessions from exhibitors; and look for the Best of DAC Contest kiosks on the exhibit floor where you can vote for your favorite vendors, enter to win a prize, and learn about winners' products.

We are privileged to have as guest speakers the ACM Turing Award winners who have been recognized with the highest honor in the area of computing for their role in developing Model-Checking into a highly effective verification technology, widely adopted in the hardware and software industries: Edmund M. Clarke, FORE Systems Professor, Carnegie Mellon University, E. Allen Emerson, Endowed Professor, University of Texas at Austin and Joseph Sifakis, CNRS Research Director, Verimag.

This year, DAC is also proud to present three keynote presentations from outstanding industry leaders: Justin R. Rattner, Intel Senior Fellow, Vice President, Director, Corporate Technology Group and Chief Technology Officer, Intel Corp.; Sanjay K. Jha, Chief Operating Officer, Qualcomm and President, Qualcomm CDMA Technologies; and Jack Little, President, CEO and Co-founder of The Mathworks, Inc.



Please join us for an informative and inspiring week.
Best regards,

Limor Fix
General Chair, 45th DAC

Keynote, Tuesday, June 10
8:30 - 10:15am • Ballroom ABC
EDA for Digital, Programmable, Multi-Radios

Justin R. Rattner
Intel Senior Fellow, Vice President, Director, Corporate Technology Group and Chief Technology Officer, Intel Corp.

New technology and innovative usage models are driving the industry towards the ubiquitous use of wireless communications. The result is an end-to-end reexamination of radio architecture from the front end module to the MAC and the expected shift from largely analog to nearly pure digital radio design. Even RF power amplifiers will be digital, rather than analog in nature. Most importantly, radios will enter an age where one physical radio acts as many logical radios all at the same time. Much in the way computers evolved decades ago, radios will become multi-programmable. The combination of new radio architectures and mostly digital implementations will drive a new generation of design tools and techniques will by necessity evolve to satisfy the demands of reconfigurable hardware and software programmability. Digital multi-radios will also accelerate the move from system-on-chip to platform-on-chip design as all the elements of the platform, including the radios, are built on one chip using a single semiconductor process.

Justin Rattner, 59, is vice president and chief technology officer (CTO). He is also an Intel Senior Fellow and head of the Corporate Technology Group. In the latter role, he directs Intel's global research efforts in microprocessors, systems, and communications including the company's disruptive research activity.

In 1989, Rattner was named Scientist of the Year by R&D Magazine for his leadership in parallel and distributed computer architecture. In December 1996, Rattner was featured as Person of the Week by ABC World News for his visionary work on the Department of Energy ASCI Red System, the first computer to sustain one trillion operations per second (one teraFLOPS) and the fastest computer in the world between 1996 and 2000. In 1997, Rattner was honored as one of the Computing 200, the 200 individuals having the greatest impact on the U.S. computer industry today, and subsequently profiled in the book Wizards and Their Wonders from ACM Press.

Rattner joined Intel in 1973. He was named its first Principal Engineer in 1979 and its fourth Intel Fellow in 1988. Prior to joining Intel, Rattner held positions with Hewlett-Packard Company and Xerox Corporation. He holds B.S. and M.S. degrees from Cornell University in electrical engineering and computer science.

Keynote, Wednesay, June 11
11:15am - 12:15pm • Ballroom ABC
Challenges on Design Complexities for Advanced Wireless Silicon Systems

Sanjay K. Jha
Chief Operating Officer, Qualcomm and President, Qualcomm CDMA Technologies

The global wireless landscape continues to change as demand for 3G technology accelerates. Qualcomm is meeting the challenge with its highly integrated SOC solutions that enable customers worldwide to bring more advanced consumer devices to market faster. Relationships and tight collaboration continue to play an integral role in product development, as it becomes more crucial than ever for partnering companies to tackle complex design issues through synergistic groups such as EDA partners, foundry partners and customers. Technology migration with the right approach is also key as chipset design continues to evolve rapidly, bringing a whole new set of design challenges to semiconductor companies. Dr. Sanjay K. Jha will elaborate on these present and future trends and reveal how collaborative business models are changing the game in chipset design.

Dr. Sanjay Jha is chief operating officer of Qualcomm and president of Qualcomm CDMA Technologies (QCT). QCT is the world's top wireless chipset provider and largest fabless semiconductor producer.

Dr. Jha began his career at Qualcomm in 1994. In 2002, Dr. Jha led the formation of Qualcomm Technologies & Ventures, where he managed both the technology investment portfolio and the new technology group as senior vice president and general manager. Dr. Jha became executive vice president of Qualcomm and president of QCT in 2003, and was promoted to chief operating officer of Qualcomm in 2006. He is also a member of the Qualcomm Ventures advisory committee.

Dr. Jha has also served as chairman of the Fabless Semiconductor Association, the voice of the fabless business model and a group with more than 450 corporate members, now known as the Global Semiconductor Alliance (GSA).

Prior to joining Qualcomm, Dr. Jha held lead design engineering roles with Brooktree Corporation in San Diego, and GEC Hirst Research Labs in London. He holds a Ph.D. in electronic and electrical engineering from the University of Strathclyde, Scotland and received his Bachelor of Science degree in engineering from the University of Liverpool, England.

Keynote, Thursday, June 12
12:45 - 1:45pm • Ballroom ABC
Idea to Implementation: A Different Perspective on System Design

Jack Little
President, CEO, and Co-founder of The Mathworks, Inc.

Today's electronic devices are multifaceted, software-intensive systems that interact with the real world. This complexity increases pressure on engineering teams that are inhibited by gaps between the different tools and workflows for system concept development, hardware design, and software development. This challenge has led to a significant movement to bridge math-based system modeling with established hardware and software implementation and verification flows. Central to this approach are multi-domain models that provide the basis for design elaboration, automatic code generation, and earlier detection and correction of design flaws. This approach, broadly adopted in aerospace and automotive, is rapidly extending into communications, electronics, industrial automation, and other industries. The solution to tomorrow's design challenges will come from interdisciplinary collaboration to deliver a complete tool chain that provides a flow from idea to system implementation. This will provide great value to companies that develop embedded systems and electronics, while creating growth opportunities for all tools that participate in the new workflow.

Jack Little is president and a co-founder of The MathWorks. He was a co-author and principal architect of early versions of the company's flagship MATLAB product as well as the Signal Processing Toolbox and the Control System Toolbox. Jack holds a B.S. degree in electrical engineering and computer science from MIT and an M.S.E.E. degree from Stanford University. A Fellow of the IEEE and Trustee of the Massachusetts Technology Leadership Council, he writes and speaks about technical computing, Model-Based Design, entrepreneurship, and software industry issues.

Technical Program Highlights

This year's technical program is especially strong, consisting of 147 papers selected from 639 submissions, with Wild and Crazy Ideas (WACIs) and the popular panels and special sessions to round it out. The program, intended for design engineers, management, researchers and developers, showcases the latest results and emerging trends in the design of electronic circuits and systems, and Electronic Design Automation (EDA).

On Tuesday, the "iDesign" Track has been added. The first session will address how to build a practical physical implementation flow, while the second offers hands-on aspects of SystemVerilog, the Verification Methodology Manual for SystemVerilog (VMM) and Universal Reuse Methodology (URM). This year's theme is wireless, highlighted by an all-day track of sessions on Wednesday, including a panel that will identify who's ready for next-generation wireless multimedia devices, and a special session titled "Business Meets Technology."

In the 36 technical paper sessions, topics range from system-level design and design for manufacturing (DFM) to verification and emerging technologies, with ample opportunity to discuss the emergence of multicore systems. Papers offer the latest in accelerating circuit simulation on multi-threaded processors to improved fault simulation on graphics processing units (GPUs).

A special session highlights issues related to the use of multicores for general-purpose as well as EDA applications. This is followed by a two-part panel; the first examines the outlook for EDA on multicores, providing the perspective of the major EDA vendors, while the second addresses the design of multicore systems. Other parts of the program will illustrate how embedded systems are going multicore as well, and present design tools to optimize embedded applications will be presented. A practical session for the verification engineer details how to achieve coverage convergence and verify multi-threaded processors.

DAC's embedded systems area continues to grow. A panel will determine whether electronic system level (ESL) signoff is imminent or impossible. Expect a debate about on-chip communication and its role in upcoming generations of on-chip systems. The importance of security, design validation and cache optimization in modern embedded system design will be analyzed. Emerging technologies such as magnetic RAM, die stacking and system in package (SiP) find their place in the "Beyond-the-Die" Track.

On-chip variability remains an important topic, as improvements in statistical timing analysis, statistical transistor models and methods to calculate on-chip capacitance sensitivity will be presented. Methods to avoid crosstalk and power delivery noise and to mitigate the effects of dynamic power gating will be discussed. A DFM session will address what effects need to be considered during the design phase to minimize post-tapeout issues and what circuit parameters need to be considered for more effective mask data preparation.

The technical program contains eight topical panels, including one that details how to verify large systems and another that assesses the current state of DFM from the vantage point of practitioners working with cutting-edge technologies. One panel taps the expertise of researchers who will discuss issues beyond the EDA domain. Yet another will review whether custom design offers a worthwhile benefit over synthesized logic, while another panel will look at on-chip thermal problems.

A slate of Pavilion panels, held on the exhibit floor, complements this list, addressing areas such as design methodology, advanced technologies and business, as well as some new additions.

The program features six tutorials on subjects that span modern software programming, DFM, system-level synthesis and verification, system-level design for embedded systems, low-power design, and practical mixed-signal design principles. All tutorials have an emphasis on the fundamentals of technology that can be used productively in the design process. In addition, each tutorial has one or more speakers who are practitioners and use the technology on real-life designs.

The theme for Hands-on Tutorials (HoTs) is "Embedding intellectual property (IP) in your design: challenges and solutions."

Monday Tutorials *9:00am - 5:00pm*

Tutorial 1: Bridging a Verification Gap: C++ to RTL for Practical Design

Tutorial 2: Programming Massively Parallel Processors: The NVIDIA Experience

Friday Tutorials *9:00am - 5:00pm*

Tutorial 3: Robust Analog Mixed-signal Design

Tutorial 4: DFM Revisited: A Comprehensive Analysis of Variability at all Levels of Abstraction

Tutorial 5: Low Power Techniques for SoC Design

Tutorial 6: System-level Design for Embedded Systems

45 YEARS
DESIGN AUTOMATION CONFERENCE

Hands-on Tutorials

Elevating Confidence in Creation and Re-use of Design IP Through Mutation-based Analysis Technology
Monday, June 9, 9:00am - 12:00pm

IP Validation for Macro and Embedded SoC
Monday, June 9, 2:00-5:00pm

Advanced Methodologies in Validating and Integrating High Speed Serial Interconnects in the Ultra Deep Sub-micron CMOS Era
Tuesday, June 10, 2:00-5:00pm

Integration, Test, Repair & Debug of Embedded -memory IP in an SoC
Wednesday, June 11, 8:00 -11:00am

What, Why and How: Using a Chip Prediction System to Find the Best IP Solution for Your Next Chip
Wednesday, June 11, 2:00-5:00pm

Hardened DDR PHY Integration
Thursday, June 12, 9:00am-12:00pm

45th Design Automation Conference / Anaheim, CA, June 8-13, 2008

Time ➡ 8:00 :15 :30 :45 9:00 10:00 11:00 12:00 1:00 2:00 3:00 4:00 5:00 6:00 7:00

Date ⬅ Room(s) ➘

Collocated MEMOCODE 2008 - Thursday, June 5 - Saturday, June 7 - Room 303B Meeting and 303C Lunch

Sunday, June 8

209A Workshop 5th International UML for SoC Design Workshop; UML in Application - Rooms: 209A Meeting, 209B Lunch

208A Workshop High-Level Synthesis: Back to the Future - Rooms: 208A Meeting, 208B Lunch

206B Workshop Low Power Coalition Workshop - Advances in Low Power Design for Circuits and Systems

204C Collocated 6th IEEE Symposium on Application Specific Processors - Rooms: 204C Meeting, 204B Lunch

Anaheim Hilton Collocated GSRC

303A Workshop System and SoC Debug - Rooms: 303A Meeting, 303B Lunch

210A Workshop Biochips to Interface and Monitor Human Biological Functions - Rooms: 210A Meeting, 210B Lunch

303C Workshop Design and Verification of Low Power SoCs: An Application Oriented Approach

EDA Consortium Executive Reception
Anaheim Hilton Hotel
Pacific Ballroom,
4:30-7:30pm

Monday, June 9

204C Collocated 6th IEEE Symposium on Application Specific Processors - Rooms: 204C Meeting, 204B Lunch

206B Workshop Introduction to Chips and EDA for a Non-Technical Audience

212A Workshop Cross-Layer Power and Thermal Management - Rooms: 212A Meeting, 212B Lunch

205A Workshop Women in Design Automation: Networking, Negotiation, and Nonsense: Achieving Career Balance in an Unbalanced World - Rooms: 205A Meeting, 205B Lunch

208B Workshop 4th Integrated Design Systems Workshop: DAC 2008 - OpenAccess: A Platform for Continuous Evolution and Innovation - Rooms: 208B Meeting, 208A Lunch

303AB Workshop Diagnostic Services in Network-on-Chips (DSNOC) - Test, Debug, and On-line Monitoring - Rooms: 303AB Meeting, 303C Lunch

207D Workshop Beyond Syntax and Semantics: Industry Experiences with OVL/SVA/PSL

204A Collocated IEEE International Workshop on Hardware - Oriented Security and Trust (HOST-2008) - Rooms: 204A Meeting, 206A Lunch

DAC Pavilion Booth #364
- Gary Smith on EDA: Trends and What's Hot at DAC
- EDA Heritage Series: Maxwell's Legacy
- Student Design Contest Award Presentation
- Next Generation Data Centers: Environmentally Green, Financially Green
- Today's Consumers: High Schoolers Spec Your Next Product
- Will 22nm Be Our Catch-22?

210AB Tutorial 1 Bridging a Verification Gap: C++ to RTL for Practical Design

209AB Tutorial 2 Programming Massively Parallel Processors: The NVIDIA Experience

213D HOTs Elevating Confidence in Creation and Re-use of Design IP Through Mutation-based Analysis Technology

Ballroom ABC HOTs IP Validation for Macro and Embedded SoC

ACM Turing Award Winners

Tuesday, June 10

206AB Session 1 iDesign I: Flow Engineering for Physical Implementation: Theory and Practice (For Designers)

207ABC Session 2 **SPECIAL SESSION:** Enabling Concurrency in EDA

208AB Session 3 CAD for FPGA

209AB Session 4 Analog Performance Modeling and Synthesis

210AB Session 5 Novel Techniques in Embedded Processor Design

210CD Session 6 **PANEL:** Electronics and Politics: What the Industry Needs from the Incoming US Administration

Ballroom ABC — General Session and Keynote Address 8:30-10:15am
EDA for Digital, Programmable, Multi-Radios
Justin R. Rattner, Intel Senior Fellow, Vice President, Director, Corporate Technology Group and Chief Technology Officer, Intel Corp.

LUNCH

IEEE Council on EDA's Distinguished Speaker Lecture and Reception
12:00-2:00pm
Room 303AB

Session 7 **SPECIAL SESSION:** Student Design Contest (For Designers)

Session 8A **PANEL:** Reinventing EDA with Manycore Processors

Session 8B **PANEL:** Multi-core SoC Design is the Challenge! What is the Solution?

Session 9 Formal Verification Technology

Session 10 Layout Techniques for Modern Chip Designs

Session 11 Application Mapping and Power Efficiency

Session 12 Variation-aware Design

BREAK

Session 13 iDesign II: SystemVerilog Implicit Port Enhancements... and Translation of an Existing VMM-based... (For Designers)

Session 14 Multi-core Simulation, Mixed-signal Power Optimization and Nanodevices

Session 15 Experiences and Advances in Formal and Dynamic Verification

Session 16 Emerging Nano/Biotechnologies

Session 17 Cache Optimization and Embedded Systems Modeling

Session 18 **PANEL:** ESL Hand-off: Fact or EDA Fiction? (For Designers)

DAC Pavilion Booth #364
- A Conversation with the 2008 Marie R. Pistilli Women in EDA Award Winner
- EDA: A View From Sand Hill Road
- Multi-processor SoCs: The Next Generation
- IP Selection: The Good, The Bad, and The Ugly
- EDA Globalization: Third World or New World?
- Quality Versus Time to Market: The Unmentionable Tradeoff
- SOI: Essential Technology or Dead End?

212A Workshop Effective Technical Writing

213D HOTs Advanced Methodologies in Validating and Integrating High-speed Serial Interconnects in the Ultra Deep Sub-micron CMOS Era (For Designers)

207D Management Day

SIGDA Ph.D. Forum and Member Meeting
6:00 - 7:30pm
Room: 204 Foyer

Wednesday, June 11

206AB Session 19 Analytical Modeling and Simulation of Complex Processing Systems

207ABC Session 20 **SPECIAL SESSION:** Wild and Crazy Ideas

208AB Session 21 **PANEL:** Next Generation Wireless - Multimedia Devices - Who is Up for the Challenge? (For Designers)

209AB Session 22 Diagnosis and Debug

210AB Session 23 Architectural and Precision Optimization in High-level Synthesis

210CD Session 24 Extraction, Interconnect and Timing

LUNCH

Ballroom ABC — Keynote Address 11:15am - 12:15pm
Challenges on Design Complexities for Advanced Wireless Silicon Systems
Sanjay K. Jha, Chief Operating Officer, Qualcomm and President, Qualcomm CDMA Technologies

Session 25 Architectures for On-chip Communication

Session 26 **SPECIAL SESSION:** CMOS Gate Modeling for Timing, Noise, and Power: Rapidly Changing Paradigm

Session 27 Advanced Wireless Design (For Designers)

Session 28 Manufacturing Aware Design and Design Aware Manufacturing

Session 29 Advances in Sequential Optimization

Session 30 **PANEL:** Verifying Really Complex Systems: On Earth and Beyond

BREAK

Session 31 Beyond the Die - Packaging and Die Stacking

Session 32 **SPECIAL SESSION:** ESL Methodologies for Platform-based Synthesis (For Designers)

Session 33 **SPECIAL SESSION:** Wireless: Business Meets Technology (For Designers)

Session 34 Leakage Analysis and Optimization

Session 35 Design Methods for On-chip Communication

Session 36 **PANEL:** Keeping Hot Chips Cool: Are IC Thermal Problems Hot Air? (For Designers)

DAC Pavilion Booth #364
- Hogan's Heroes - Behavioral Synthesis: Is That Light at the End of the Tunnel an Oncoming Train?
- Advanced Low Power Techniques: Is Your Design Method Too Powerful?
- DFM Design Rules: Worth The Effort?
- Designing the New-generation Wireless Platform: Lessons from iPhone and Android
- What's Holding Back Analog Design Automation?

213D HOTs Integration, Test, Repair and Debug of Embedded Memory IP in an SoC

HOTs What, Why and How: Using a Chip Prediction System to Find the Best IP Solution for Your Next Chip

45th DAC Party
7:30 - 10:00pm
Anaheim Marriott

Thursday, June 12

206AB Session 37 New Advances in Logic Synthesis

207ABC Session 38 **SPECIAL SESSION:** 3-D Semiconductor Integration and Packaging

208AB Session 39 Statistical Timing Analysis

209AB Session 40 Performance Driven Layout Optimization

210AB Session 41 Power and Thermal Considerations in Single- and Multi-core Systems

210CD Session 42 Multi-core Design Tools and Architectures

LUNCH

BallroomABC — DAC Best Paper Presentation and Keynote Address 12:45 - 1:45pm
Idea to Implementation: A Different Perspective on System Design
Jack Little, President and Co-Founder, The Mathworks, Inc.

Session 43 Reconfigurable Architecture Optimizations

Session 44 **SPECIAL SESSION:** Dude or Dud? Experiences from the Trenches (For Designers)

Session 45 Random Topics in Testing

Session 46 Securing and Debugging Embedded Systems

Session 47 Topics in Power and Thermal Management

Session 48 **PANEL:** DFM in Practice: Hit or Hype (For Designers)

BREAK

Session 49 Physical Effects of Variability

Session 50 Soft Error in Scaled CMOS Design

Session 51 Advances in Verification of Abstract (pre RTL) Models

Session 52 Design Space Exploration

Session 53 Noise Reliability Enhancement

Session 54 **PANEL:** Custom is from Mars and Synthesis from Venus (For Designers)

212A Collocated NANOARCH'08: 4th IEEE/ACM International Symposium on Nanoscale Architectures - Rooms: 212A Meeting, 212B Lunch

DAC Pavilion Booth #364
- 45nm: Collaborate, Aggregate, Differentiate
- Your Functional Verification Roadmap: OVM, VMM or Roll Your Own?

213D HOTs Hardened DDR PHY Integration

303A Workshop Maximizing Efficiency in the Development Cycle

Friday, June 13

208AB Tutorial 3 Robust Analog Mixed-signal Design

210AB Tutorial 4 DFM Revisited: A Comprehensive Analysis of Variability at All Levels of Abstraction

209AB Tutorial 5 Low Power Techniques for SoC Design

210CD Tutorial 6 System-level Design for Embedded Systems

212A Collocated NANOARCH'08: 4th IEEE/ACM International Symposium on Nanoscale Architectures - Rooms: 212A Meeting, 212B Lunch

Topic Area Legend:

Synthesis and FPGA | Business | Interconnect and Reliability | Analog/Mixed-signal/RF and Simulation | Verfication and Test | Physical Design | New and Emerging Technologies | DFM and the Manufacturing Interface | Wireless | Strictly Design | System-level and Embedded | Low Power Design

Management Day –Tuesday, June 10

10:30am-6:00pm

The Management Day is designed to provide managers with timely information to help them make decisions where business and technology intersect. The day is comprised of three sessions featuring presentations by managers representing key independent device manufacturers (IDMs) and major fabless companies.

Consumer application chips are the technology drivers today. They require different types of optimizations and thus the adoption of emerging solutions to meet such requirements. Optimizing for high volume production, low power, and shrinking sizes necessitates adequate trade-off analysis and technical/business decision-making by management. Also, moving to new semiconductor technology nodes, such as 45nm and 65nm, can significantly affect the choices of suppliers.

The Management Day sessions will discuss these changing needs and demonstrate corresponding management decision criteria to make the right choices from a pool of alternate options for flows, methodologies and suppliers. The leading managers of today's most complex nanometer chips will present these emerging solutions and their economic impact. This year's Management Day will provide a unique opportunity for managers to gain insights from their peers in the industry.

Wireless Theme at DAC

Wireless applications can be found in every aspect of our lives. The wireless communications industry is diverse and ranges from systems like cellular phones to personal wireless internet like WiFi, to shorter range devices like low-power Bluetooth devices.

DAC explores wireless design and its impact on design automation from both a business and a technical perspective. While wireless communications systems represented more than 67% of the total communications systems market in 2007, cellular technology was more than 40% of that wireless market and remains the single dominant element to drive design automation technology.

Wireless semiconductor systems design requires design success on numerous fronts. This makes DAC the ideal place for the industry to explore design automation advances to solve wireless design challenges. DAC covers the pressing deep submicron, complex SoC design, verification, low-power and hardware/software design challenges that must be resolved to support continued productivity of wireless design teams.

DAC Workshops

DAC has an exciting lineup of workshops and collocated events... nearly four times as many as in previous years. This year's schedule includes:

Sunday, June 8

8:30am-5:15pm	High-level Synthesis: Back to the Future
9:00am-6:00pm	5th International UML for SoC Design Workshop - UML in Application
9:00am-4:30pm	Biochips to Interface and Monitor Human Biological Functions
9:00am-5:15pm	System and SoC Debug Workshop
2:00-5:00pm	Design and Verification of Low Power SoCs: An Application Oriented Approach
4:00-7:00pm	Low Power Coalition Workshop - Advances in Low Power Design for Circuits and Systems

Monday, June 9

8:30am-5:30pm	Cross-layer Power and Thermal Management
9:00am-5:00pm	Diagnostic Services in Network-on-Chips (DSNOC)
10:00am-12:00pm	Introduction to Chips and EDA for a Non-technical Audience
9:00am-1:45pm	Workshop for Women in Design Automation (WWINDA): Networking, Negotiation, and Nonsense: Achieving Career Balance in an Unbalanced World
12:00-4:00pm	4th Integrated Design Systems Workshop: DAC 2008 OpenAccess: A Platform for Continuous Evolution and Innovation
1:00-5:15pm	Beyond Syntax and Semantics: Industry Experiences with OVL/SVA/PSL

Tuesday, June 10

10:00am-12:00pm	Effective Technical Writing
iDesign Track	Tuesday Keynote, Sessions 1, 7 and 13

Thursday, June 12

2:00-4:00pm	Maximizing Efficiency in the Development Cycle

Adjunct Event

Global Semiconductor Test Consortium Conference (GSC)
June 4-6, 2008: Hilton Hotel, San Diego
http://www.semitest.org/events/gscwebpage/

Collocated Events

MEMOCODE 2008
8:00am-5:00pm, June 5-7, 2008: Anaheim Convention Center

GSRC
June 8, 2008: Anaheim Hilton
http://www.gigascale.org/

6th IEEE Symposium on Application Specific Processors
8:30am-6:30pm , June 8-9, 2008: Anaheim Convention Center

IEEE International Workshop on Hardware-oriented Security and Trust (HOST-2008)
8:30am-5:30pm , June 9, 2008: Anaheim Convention Center

NANOARCH '08 : 4th IEEE/ACM International Symposium on Nanoscale Architectures
9:00am-5:00pm, June 12-13, 2008: Anaheim Convention Center

Exhibition

Visit the DAC exhibition to learn in-depth information on new products and services from 250 vendors offering products for all phases of the electronic design process including EDA tools, IP cores, embedded system and system-level tools, as well as design-for-manufacturing, silicon vendors and design services companies.

The DAC show floor features its unique exhibit booth and private suite combination, which gives you the freedom to deeply explore the products on the show floor and find the right solution for your design flow. Find out how you can improve performance and shorten the time-to-market on your next design.

Check out these features of the DAC exhibition:

NEW Best of DAC contest! Look for kiosks on the floor and vote for your favorite vendors! When you cast your ballot you will be entered to win a Nintendo Wii!

NEW Exhibitor Forum – DAC's newest feature for exhibit floor education. Attendees are invited to the Exhibitor Forum in Booth 2849 to hear a series of technical presentations from exhibitors on focused topics. Compare how exhibitors are solving your tough design issues with their latest tools and methodologies.

DAC Pavilion – The popular DAC Pavilion is back in Booth 364 with 20 presentations this year on business and technical issues.

New FREE Exhibits-only Pass. DAC is offering a new registration option to attendees. Register for the Exhibits-only pass by May 19 and receive entrance to all days of the exhibition, three keynotes, DAC Pavilion sessions and the new Exhibitor Forum at no charge. Don't hesitate, after May 19 the cost is $65 – still a terrific value!

Exhibition Hours

Monday-Wednesday, June 9-11	9:00am-6:00pm
Thursday, June 12	9:00am-1:00pm

EXHIBITING COMPANIES

Accelicon Technologies, Inc.
* ACCIT - New Systems Research
ACE Associated Compiler Experts bv
Agilent Technologies
Aldec, Inc.
Altos Design Automation
Analog Bits Inc.
Analog Rails
Anchor Semiconductor, Inc.
Ansoft Corp.
Apache Design Solutions, Inc.
Applied Simulation Technology
Artwork Conversion Software, Inc.
Atoptech
Atrenta Inc.
Attachmate
austriamicrosystems USA, Inc.
AutoESL Design Technologies Inc.
Averant, Inc.
Avery Design Systems, Inc.
Axiom Design Automation
Azuro, Inc.
Beach Solutions Ltd.
Berkeley Design Automation, Inc.
Blaze DFM, Inc.
Blue Pearl Software
Bluespec, Inc.
Breker Verification Systems
Calypto Design Systems
Carbon Design Systems, Inc.
CAST, Inc.
CebaTech, Inc.
Certess Inc.
ChipEstimate.com
ChipVision Design Systems Inc.
Cranova, Inc.
ClioSoft, Inc.
CLK Design Automation, Inc.
CMP
CoFluent Design
* Common Platform
Concept Engineering GmbH
Coupling Wave Solutions
CoWare, Inc.
CriticalBlue
* Cyclos Semiconductor, Inc.
DAC Pavilion
DAFCA, Inc.
Dassault Systemes ENOVIA Corp.
Dataram
DATE'09
Denali Software, Inc.
Design and Reuse
Dini Group (The)
Dolphin Integration
* Dorado Design Automation, Inc.
Doulos
* DTC, National Tsing Hua University
Duolog Technologies Ltd.
Dynalith Systems Co., Ltd.
EDXACT
Elsevier
EMA Design Automation, Inc.
Entasys Design, Inc.
Envision Technology
Europractice
EVE
Exhibitor Forum
Extreme DA
Fenix Design Automation
FishTail Design Automation
Forte Design Systems
FTL Systems, Inc.
* GATeIC
* Gauda
Genesys Testware, Inc.
GiDEL
Gradient Design Automation
Handshake Solutions
Helic S.A.
Hewlett-Packard Co.
Hummingbird - An Open Text Connectivity Solutions Group
IBM Corp.
IC Manage, Inc.
IEEE Media
IHS
Imperas, Inc.
Incentia Design Systems, Inc.
Infinicale
Innovative Silicon Inc.
Intel Corp.
InternetCAD.com, Inc./Timberwolf Systems
Interra Systems, Inc.
Jasper Design Automation, Inc.
Javelin Design Automation, Inc.
JEDA Technologies
* Jspeed Design Automation, Inc.
KETI / IP SoC Support Center
Kilopass Technology, Inc.
Laflin Instigate
Legend Design Technology, Inc.
Library Technologies, Inc.
Liga Systems, Inc.
LogicVision, Inc.
Lorentz Solution
Lynguent, Inc.
Magillem Design Services
Magma Design Automation, Inc.
MathWorks, Inc. (The)
Mentor Graphics Corp.
Micro Magic, Inc.
Micrologic Design Automation
Mixel, Inc.
MOSIS Service (The)
MunEDA GmbH
MyCAD, Inc.
Nangate
Nannor Technologies, Inc.
Nascentric, Inc.
National Instruments Corp.
NEC Informatec Systems, Ltd.
Novas Software, Inc.
Novelics
Nusym Technology, Inc.
OCP International Partnership
OEA International, Inc.
OneSpin Solutions GmbH
Open iT, Inc.
OptEM Engineering Inc.
Paradigm Works, Inc.
Pextra
Physware, Inc.
Platform Computing
* Polar Instruments Inc.
* POLYTEDA Software Corp.
Prentice Hall Professional / Pearson Education, Inc.
ProDesign Electronic Corp.
Prolific, Inc.
Pyxis Technology, Inc.
QThink
Real Intent, Inc.
Reed Business Information
Runtime Design Automation
Sagantec
Samsung
Samtec, Inc.
Samoff Europe
* Satin IP Technologies
Semifore, Inc.
Sequence Design, Inc.
Shearwater Group, Inc.
SIGDA/DAC University Booth
Sigrity, Inc.
Silicon Canvas Inc.
Silicon Design Solutions
Silicon Frontline Technology
Silicon Image
Silicon Integration Initiative - Si2, Inc.
Silicon Navigator
Simucad Design Automation Inc.
* Snowbush Microelectronics
SoftJin Technologies Pvt. Ltd.
Solido Design Automation Inc.
* Sonnet Software, Inc.
* Spatial
Springer
StarNet Communications
Sun Microsystems
Swati Design
* Synapse Design Automation
SynCira
Synfora, Inc.
Synopsys, Inc.
Synplicity, Inc.
SynTest Technologies, Inc.
Takumi Technology Corp.
Tanner EDA
Target Compiler Technologies
TechForce, Inc.
Teklatech
* Tela Innovations
Tensilica, Inc.
Time To Market Inc.
TOOL Corp.
True Circuits, Inc.
TSMC
TSSI - Test Systems Strategies, Inc.
Tuscany Design Automation, Inc.
UMC
Uniquify
VeriEZ Solutions, Inc.
Verific Design Automation
Veritools, Inc.
ViASIC Inc.
Virage Logic Corp.
* WinterLogic Inc.
Xoomsys
XYALIS
Z Circuit Automation, Inc.
Zeland Software, Inc..

(as of March 26, 2008)
* - indicates first time exhibitor

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