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Registration Hours

Sunday, June 3, 2007..... 8:30am – 6:00pm
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Co-Located Conferences

- **MSE 2007 - June 2-4, San Diego, CA**
- **Design Automation Summer School - June 2-3**
  San Diego Convention Center, Rm: 24AB - 8:00am – 6:00pm

Tutorial Registration

Friday, June 8, 2007..... 7:00am – 6:00pm
Tutorial registration is located on the second level outside meeting room 6.

DACnet - 2007

DACnet stations are located in Lobby E and in the Sails Pavilion located on the second level.

On-Site Information Desk

The Information Desk is located in Lobby C. Questions? Call 619-525-6239.

Book Signing

Thursday, June 7, 2007, 12:00pm – 12:30pm in Foyer Ballroom 20. Meet the leading authors of the hottest EDA books, get their thoughts on the topics, and have them sign your book.

The 44th Design Automation Conference Week in Review

Sunday, June 3	Monday, June 4	Tuesday, June 5	Wednesday, June 6	Thursday, June 7	Friday, June 8
• 4 Workshops	• FREE Monday Exhibits • Full-Day Tutorials • Hands-on Tutorials • Workshops • Keynote Address • Happy Hour on the Exhibit Floor • Pavilion Panels	• General Session • Keynote Address • Technical Sessions • Management Seminar • Hands-on Tutorial • Exhibits • Productivity Impact Luncheon • Pavilion Panels	• Technical Sessions • Hands-on Tutorials • Automotive Theme Sessions • Exhibits • DAC Party • Pavilion Panels	• Technical Sessions • Best Paper Awards • Keynote Address • Hands-on Tutorial • Exhibits • Pavilion Panels	• 5 Full-Day Tutorials

San Diego Welcome

44th Design Automation Conference

It is my pleasure to welcome the 44th Design Automation Conference (DAC) to beautiful San Diego. As the premier international event for Electronic Design Automation (EDA), San Diego is delighted to serve as your host to a conference with more than 10,000 attendees, 50 technical sessions and 250 exhibitors. Its 40-year commitment to advancing technologies to enable electronics products of all kinds is impressive, as is the community of developers, designers, researchers, managers and engineers it serves from leading electronics companies and noted universities.

While in San Diego, please take the time to enjoy Seaport Village, SeaWorld, our world-class zoo, beaches, museums, historical sites and wonderful restaurants. Thank you for choosing San Diego, America's finest city, as host for the 44th Design Automation Conference. San Diego welcomes all DAC attendees and its sponsors.

Sincerely,

Jerry Sanders
Mayor

Stay Connected at DAC

Wireless Internet

DAC is offering complimentary wireless internet throughout the San Deigo Convention Center. Look for SSID: DAC2007. Sponsored by Apache Design Solutions, EE Times and DAC.

Mobile Devices

DAC has a special web site built for viewing from handheld mobile devices. From your Windows Mobile or Blackberry device log in to www.dac.com and you will automatically be redirected to the mobile site. Presentation schedules, the exhibitor listing and other useful information are available and optimized for viewing on small screens.

Daily Updates on DAC.com

Check the DAC web site daily for a complete listing of each day's schedule, latest exhibitor announcements and press coverage.

DACnet - 2007

DACnet internet stations are available in the lower-level Lobby E and in the upper-level Sails Pavilion of the San Diego Convention Center. Power for laptop plug-in is also available at both locations.

Food Courts

Two food courts are available on the exhibit floor. Each food court includes tables with power connections for laptop plug-in. Wireless internet access is also available for attendee use.

Technical Program Highlights

This year DAC is celebrating its 44th year with a technical program that includes over 260 papers, panels, tutorials, and keynote presentations covering a wide range of design issues. The technical sessions are divided into eleven tracks: Analog/Mixed-Signal/RF and Simulation, Automotive Electronics, Business, DFM and the Manufacturing Interface, Interconnect and Reliability, Low Power Design, New and Emerging Technologies, Physical Design, Synthesis and FPGA, System Level and Embedded Design, and Verification and Test.

In each of these areas the sessions will cover aspects of both design methodology and design tools. The themed sessions for the 44th DAC focus on automotive electronics. The theme is woven into the Monday keynote address, Wednesday technical sessions, panels, and pavilion panels.

Management Seminar - details on pgs. 8 & 9

The Management Seminar on Tuesday, June 5, is designed for middle and senior management who wish to consider innovation as a part of strategic planning. The Seminar includes topics on Innovative Fundamentals, Innovation in the Semiconductor and Electronic Design Automation Markets, and Investing for Innovation.

Automotive Theme - details on pg. 6

The technical theme for this year's DAC is automotive electronics. An all-day track on Wednesday includes a special session, invited talks, a panel, four pavilion panels, and regular papers. Modern automobiles have an incredible array of electronic systems: engine management, satellite navigation, adaptive cruise control and many more. The increasing trend in automotive electronics shows few signs of abating. It has been estimated that electronics will account for as much as 40% of a car's bill-of-materials by the end of this decade. The modern car can now truly be described as a "networked computing platform," and the theme will highlight this issue in the context of electronic design automation.

Hands-on Tutorials - details on pgs. 55 - 57

The six Hands-on Tutorials are three-hour tutorials presented by exhibitors to demonstrate their solutions to issues in DFM.

Tutorials - details on pgs. 44 - 47

Monday, June 4 • 9:00am – 5:00pm

1) Anatomy of Variability and Making of "Variation Tolerance" Vaccine in Nanometer Technologies
2) System Design for Multimedia Applications - Challenges, Design Methods and Recent Developments

Friday, June 8 • 9:00am – 5:00pm

3) Formal Assertion Based Verification in an Industrial Setting
4) Design and Analysis of High-Performance Package and Die Power Delivery Networks
5) Soft Errors: Technology Trends, System Effects and Design Techniques
6) How Design Meets Yield in the Fab
7) Circuit and CAD Techniques for Low Power Design

Monday Keynote Monday, June 4 • 2:00pm – 3:00pm

Lawrence D. Burns - ***Vice President of Research & Development and Strategic Planning, General Motors Corp.***

Tuesday Keynote Tuesday, June 5 • 8:30am – 10:15am

Oh-Hyun Kwon - ***President, System LSI Division, Samsung Semiconductor Business***

Thursday Keynote Thursday, June 7 • 12:30pm – 1:45pm

Jan M. Rabaey - ***Donald O. Pederson Distinguished Professor, Director Gigascale Systems Research Center (GSRC), Scientific Co-director BWRC, University of California, Berkeley***

Automotive Theme

There has been an explosion of electronic content in automobiles recently. For 2007, the automotive semiconductor market is expected to be $19 billion (Gartner/Dataquest) and by 2010 it is expected that 40% of the bill of materials in cars will be for electronics. The Automotive theme addresses how design tools and methodologies will be used to support the tremendous design requirements for automotive electronics and what role EDA will play.

Attendees will have a chance to "look under the hood" of two cars that represent the future of automotive electronics: the GM Sequel Hydrogen car and the Wrightspeed X1 prototype electric car with a few lucky attendees getting a chance to test drive the Sequel Hydrogen car.

Technical presentations from experts representing leading electronics and automotive suppliers include a Keynote address by Larry Burns, Vice President of Research & Development and Strategic Planning for General Motors. Other technical presentations include sessions on Automotive Electronics as a major product differentiator, the network protocols for distributed architectures, safety issues including robust design, and the validating and testing of automotive software. Additional sessions address the use of virtual platforms to reduce MCU count, embedded systems design as a competitive advantage, and how the changing requirements of the automotive market will affect the R&D agendas of semiconductor and EDA companies.

- **Monday, June 4, 2:00pm • Keynote Address**
  Designing a New Automotive DNA
- **Wednesday, June 6, 8:30am • Session 16**
  Distributed Computing: Automotive Network Design and Analysis
- **Wednesday, June 6, 9:30am • Pavilion Panel**
  The Urban Challenge: Paving the way for Driverless Automobiles
- **Wednesday, June 6, 10:30am • Session 21**
  INVITED SESSION: Silicon, Safety and Self-Driving Cars
- **Wednesday, June 6, 11:00am • Pavilion Panel**
  Improving Automotive Competitiveness: New Methods and Tools For Embedded Design
- **Wednesday, June 6, 1:00pm • Pavilion Panel**
  Electronics: The Key to Disruption of Automobile Powertrain Technology
- **Wednesday, June 6, 2:00pm • Session 26**
  PANEL: Electronics: The New Differential in the Automotive Industry
- **Wednesday, June 6, 3:15pm • Pavilion Panel**
  On a Crash Course: Validation and Testing of Automotive Software
- **Wednesday, June 6, 4:30pm • Pavilion Panel**
  The One Ton Mobile Platform: Where is it Taking Us?
- **Wednesday, June 6, 4:30pm • Session 31**
  SPECIAL SESSION: Virtual Automotive Platforms

Exhibit Highlights

Exhibit Floor

Monday – Wednesday, June 4-6, 9:00am – 6:00pm

Thursday, June 7, 9:00am – 1:00pm

The 44th DAC Exhibition is located in Halls B through G of the San Diego Convention Center.

The DAC Exhibit floor is bursting with over 240 vendors offering products for all phases of the electronic design process including EDA tools, IP cores, embedded system and system-level tools, as well as silicon vendors, and design-for-manufacturing companies. The DAC show floor features its unique exhibit booth and private suite combination, which gives you the freedom to deeply explore the products on the show floor and find a solution that is right for your design. Visit the DAC exhibition and find out how you can improve performance and shorten the time-to-market on your next product.

Children under the age of 14 will NOT be allowed in the exhibit hall.

Exhibit-Only Registration

- Free Monday Exhibits-Only Passes - Attend the exhibition free of charge Monday, June 4.
- $65 Exhibit-Only registration will allow you to attend exhibits Monday through Thursday.

DAC Pavilion

DAC has an exciting line-up of panels and presentations in the DAC Pavilion, booth 6360 on the exhibit floor. The DAC Pavilion sessions are open to all exhibit floor attendees at no charge and feature 18 provocative technical, business and strategy discussions. See pages 19-22 for details.

New Exhibitors at DAC

DAC has always been the best place to see the industry's newest companies, and this year is no exception. With over 35 new exhibitors, DAC is the place to be to find out what the hot startups are up to. Among the companies participating in DAC for the first time are:

Analog Rails
Arasan Chip Systems
Atoptech
Attachmate
AutoESL Design Technologies Inc.
Breker Verification Systems
CAD Science, Inc.
CLK Design Automation, Inc.
eMemory Technology Inc.
Envision Technology
Evolvable Systems Research Institute, Inc
FSA
GateRocket, Inc.
Heller Ehrman
InsideChips.com
Interoperable PCell Libraries
Lightspeed Logic
Magillem Design Services
MataiTech LLC
Micrologic Design Automation
Mimosys AG
Mirabilis Design Inc.
Mixel, Inc.
Nanovata Design Automation
Novelics
Nusym Technology, Inc.
Plurality Ltd.
Quik-Pak
Samtec, Inc.
Silicon Frontline Technology
Swati Design Automation, Inc.
Teklatech
TSSI - Test Systems Strategies, Inc.
Unified Power Format

Management Seminar

Tuesday, June 5, 2007 **10:30am – 6:45pm | Room: 6A**

Innovation or Extinction - The Choice Is Yours!

Innovation is critical for the long term success of any industry. The electronics, semiconductor and the electronic design automation industry have pursued such a strategy successfully for several decades. This was made possible by technological advances in processing, innovative design flows and methodologies, and continued improvement in design tools. However, limitations in manufacturing, increasing design complexity and design costs have started to decelerate the possible gains obtained along these directions. In the recent past, growth in these industries has slowed and it is perceived by many that these industries need to do more to capture growth. In addition, the twin forces of globalization and technology have led to changes that impact business dramatically. Globalization has enabled vast and eager talent pools to participate in business at low cost. Technology has lowered the barriers to market entry and leveled the playing field in many situations. In the current scenario, innovation is not only key but perhaps the only method to differentiate your business from that of your competitors.

This seminar is designed for middle and senior management who wish to consider innovation as a part of strategic planning. The seminar is structured in three parts.

Registration for this event includes: entrance to the Keynotes, entrance to the Exhibition, a copy of "*Dealing with Darwin*" coffee breaks and the Productivity Impact Luncheon (produced by EDA Consortium and FSA, with contributions from EE Times).

1) Innovation Fundamentals

The audience is provided an introduction to the factors that affect the choice of innovation strategies such as category maturity cycles and business architectures. The speaker will describe various innovation strategies depending on the life cycle of a product and the market in which the company operates. We will also cover challenges in managing innovation.

Speaker: **Geoffrey Moore** - *TCG Advisors, San Mateo, CA*

Dr. Geoffrey Moore is a best-selling author and a managing partner at TCG Advisors. His recent book "*Dealing with Darwin*" has demystified the process of innovation and made innovation a key part of the corporate lexicon. Recognized for his expertise in market development and business and investment strategies, he serves as an advisor to many companies, drawing upon best practices derived from his extensive work with technology startups. Dr. Moore's other books, "*Crossing the Chasm*," "*Inside the Tornado*," "*The Gorilla Game*," and "*Living on the Fault Line*," are best sellers and required reading at leading business schools. Highly regarded as a dynamic public speaker, Dr. Moore is also a founder of The Chasm Group and a venture partner at Mohr Davidow Ventures. Prior to founding The Chasm Group in 1992, he was a principal and partner at Regis McKenna, Inc., a leading high tech marketing strategy and communications company, and for the decade prior, a sales and marketing executive in the software industry. He holds a bachelor's degree in literature from Stanford University and a doctorate in literature from the University of Washington.

Management Seminar

Tuesday, June 5, 2007 **10:30am – 6:45pm | Room: 6A**

Innovation or Extinction - The Choice Is Yours!

2) Innovation in the Semiconductor and Electronic Design Automation Markets

In this section, we will provide the audience with an evolution of innovation in these industries. We will then look at challenges facing the industry today and possible approaches for businesses to innovate given the background provided by Dr. Moore.

Speaker: **Raul Camposano** - *Xoomsys, Inc., Cupertino, CA*

Dr. Raul Camposano served as the chief technical officer, senior vice president and general manager of the Silicon Engineering Group at Synopsys until 2006. He held multiple positions at Synopsys, among them, general manager of the Design Tools business. Prior to joining Synopsys in 1994, Dr. Camposano was director for the German National Research Center for Computer Science, Professor of Computer Science at the University of Paderborn, and a research staff member at the IBM T.J. Watson Research Center. Dr. Camposano has authored/co-authored more than seventy technical papers and three books on EDA and is a fellow of the IEEE. He holds a B.S.E.E. and an M.S. from the University of Chile and a Ph.D. in computer science from the University of Karlsruhe.

3) Investing for Innovation

How does an investor look to fund companies that deal with innovations? How does one measure return on innovation? Are there any preferences for innovation types when investing? The speaker will also provide examples of investments that succeeded/failed and why.

Speaker: **Jim Smith** - *Mohr Davidow Ventures, Menlo Park, CA*

Dr. Jim Smith is a general partner at Mohr Davidow Ventures (MDV). He focuses on software and systems and semiconductor investments and is active in extending MDV's relationships with leading universities and research centers. Prior to MDV, he spent six years developing computing architectures and integrated circuits for high-performance multimedia systems at Silicon Graphics, Inc., including the multi-billion dollar revenue O2 and Octane workstation lines. He also spent three years as a researcher in the Computer Systems Laboratory at Stanford University. Dr. Smith has authored and refereed numerous papers on computing systems and circuit design. He received a doctorate in electrical engineering and a master's degree in industrial management from Stanford University, where he also earned a bachelor's degree in computer systems engineering and a master's degree in electrical engineering.

Monday Keynote

2:00pm - 3:00pm | Room: Ballroom 20ABC

Designing a New Automotive DNA

Lawrence D. Burns, *Vice President of Research & Development and Strategic Planning, General Motors Corp.*

The automotive industry stands on the threshold of a new opportunity - an opportunity that stems from the reinvention of the automobile using a new DNA that exchanges the internal combustion engine, petroleum, and mechanical linkages for fuel cells and batteries, hydrogen and electricity, and electronic systems and controls.

Electrically driven vehicles and the introduction of advanced electronics and connected vehicle technologies will revolutionize how our vehicles operate, how we interact with them, and how they communicate with each other and the outside world. These new technologies will also, importantly, dramatically change how automobiles are designed and built.

In this talk, Dr. Burns will highlight why the new automotive DNA will be paradigm shifting for the industry and address the design challenges and opportunities presented by the requirement for new electrical and electronics-based architectures, systems, and software for our vehicles.

Larry Burns is Vice President of General Motors Research & Development and Strategic Planning. In this post, he oversees GM's advanced technology, innovation programs, and corporate strategy. He is a member of GM's Automotive Strategy Board and Automotive Product Board.

In addition to driving innovation into today's vehicles, Burns is championing GM's "reinvention" of the automobile around advanced propulsion, electronics, telematics, and materials technologies. The goal is to realize sustainable mobility with vehicles that are aspirational and affordable.

Burns began his career in 1969 as a member of the Research & Development staff, where his research focused on transportation, logistics, and production systems. He subsequently held executive positions in several GM divisions in the areas of product program management, quality, production control, industrial engineering, and product and business planning. In May 1998, he was named a vice president of General Motors, with responsibility for R&D and Planning.

Burns holds a Ph.D. in civil engineering from the University of California at Berkeley. He also has a master's degree in engineering/public policy from the University of Michigan and a bachelor's degree in mechanical engineering from General Motors Institute (now Kettering University).

Burns is a member of the USCAR Operating Council and the FreedomCAR Partnership Executive Steering Committee. He serves on the University of Michigan's Automotive Research Center board and recently completed a six-year term on its College of Engineering National Advisory Council. In addition, he is a member of the Advisory Council for the University of California Berkeley's Institute of Transportation Studies and a member of the Board of Trustees of the Midwest Research Institute. Burns also sits on the board of the University of Michigan Center for Hearing Disorders and is a member of the National Advisory Group for the National Technical Institute for the Deaf at Rochester Institute of Technology.

In 2000, Burns received Kettering University's Engineering Alumni Achievement Award for his contributions to the engineering profession. In 2002, the Deafness Research Foundation recognized him with its National Campaign for Hearing Health Leadership Award. In 2005, he was a member of a General Motors team awarded the Franz Edelman Award from the Institute for Operations Research and the Management Sciences. Burns is also the recipient of the 2005 Alumni Merit Award from the University of Michigan Industrial and Operations Engineering Department. He recently completed a two-year term as National Honorary Chairman for the MATHCOUNTS Foundation.

8:30am - 10:15am | Room: Ballroom 20ABC

Tuesday Keynote

Perspective of the Future Semiconductor Industry: Challenges and Solutions

Oh-Hyun Kwon, *President, System LSI Division, Samsung Semiconductor Business*

The semiconductor industry currently faces serious challenges and changes on both the business and technology fronts. The business environment is becoming more difficult. The huge investment required for new fabrication facilities is forcing many IDMs (Integrated Device Manufacturers) to change their business model to either fablite or fabless. The significant costs to develop the next generation process technologies are necessitating joint development between various companies. Furthermore, due to severe competition in the mobile and digital consumer markets, low chip prices and short time-to-market are both essential for survival. To satisfy these market requirements, heavy R&D expenses and resources are needed. However, its return on investment is becoming marginal and even uncertain. To overcome this difficult situation, the industry is experiencing consolidation of once proudly independent companies. On the technical side, controlling chip yield, power consumption and design complexity have become extremely difficult in the nano-technology era.

This talk will present a perspective on how the semiconductor industry must respond to these challenges by developing new markets, new products, and new technologies. The solutions will come from (i) collaborations with key customers for new markets and products, as well as, with key partners for new technologies, and (ii) technology breakthroughs with innovative ideas, such as 3-D package, fusion technologies (OneDRAM™, OneNAND™), variation-tolerant designs, and low leakage devices. These approaches can lead to lower chip costs and relieve physical uncertainty problems.

Dr. Oh-Hyun Kwon was appointed as President of the System LSI Division at Samsung Electronics in 2004.

Dr. Kwon led the team that developed the industry's first 64M DRAM in 1992. He was also in charge of various memory technology development such as DRAM, SRAM, and flash memory until 1996. Since 1997, he has worked at the System LSI Division of Samsung Electronics for both product and business development.

Dr. Kwon has a Ph.D. in Electrical Engineering from Stanford University. He received his MS in EE from Korea Advanced Institute of Science and Technology and a BS in EE from Seoul National University.

Thursday Keynote

12:30pm - 1:45pm | Room: Ballroom 20ABC

Design without Borders - A Tribute to the Legacy of A. Richard Newton

Jan M. Rabaey, *Donald O. Pederson Distinguished Professor*
Director Gigascale Systems Research Center (GSRC)
Scientific Co-director BWRC University of California, Berkeley

Electrical engineers have learned how to build amazingly complex systems by assembling transistors, wires, and passive components into intricate networks. While solidly founded in semiconductor physics, pure engineering has made possible the design of multi-billion transistor chips in a repetitive, reliable and cost-effective way. A comprehensive "design methodology" was developed based on modularization, hierarchy and abstraction.

Today this story is repeating itself. Physicists, chemists and biologists are exploring entirely different components such as molecules, atoms, and enzymes. Systems built from those will most probably impact our lives and society in a profound way. Outcomes will influence the ways we build mechanical structures, do computing, make drugs, generate energy and take care of our environment.

Yet, while the basic components are dramatically different from our silicon devices, the basic strategy for building very complex systems from them remains unchanged. The art of design, as was developed in the silicon era, is just as applicable to these nano- or bio-constructions. Design methodology is a legacy that will live long after Moore's law has come to a halt. To quote Richard, "The Future is BDA (Bio Design Automation)".

Dr. Rabaey received the EE and Ph.D. degrees in applied sciences from the Katholieke Universiteit Leuven, Belgium. From 1983 until 1985, he was connected to the University of California, Berkeley as a Visiting Research Engineer. From 1985 until 1987, he was a research manager at IMEC, Belgium, and in 1987, he joined the faculty of the Electrical Engineering and Computer Science department of the University of California, Berkeley, where he now holds the Donald O. Pederson Distinguished Professorship. He was the associate chair of the EECS Dept. at Berkeley from 1999 until 2002, and is currently the Scientific co-director of the Berkeley Wireless Research Center (BWRC), as well as the Director of the GigaScale Systems Research Center (GSRC). Prof. Rabaey serves on the advisory board of a range of companies and research institutes in the areas of design automation, semiconductor intellectual property and wireless systems. He is an IEEE Fellow. Prof. Rabaey's main interests are in the exploring of limits in low-power design, and the conception and implementation of future-generation wireless systems.

Topics and Related Sessions

Of special interest to designers – Sessions: 1, 2, 3, 6, 7, 11, 12, 16, 20, 21, 22, 25, 26, 28, 31, 32, 35, 39, 41, 42, 44, 53

Session Tracks:

Analog/Mixed-Signal/RF and Simulation – Sessions: 9, 24, 50

Automotive Theme – Sessions: 16, 21, 31

Business – Sessions: 2 / Management Seminar

DFM and the Manufacturing Interface – Sessions: 7, 14, 22, 29, 45 / Tutorials 1 & 6 / All Hands-On-Tutorials

Interconnect and Reliability – Sessions: 1, 4, 10, 20, 32 / Tutorials 4 & 5

Low Power Design – Sessions: 6, 12, 39, 47 / Tutorial 7

New and Emerging Technologies – Sessions: 15, 17, 36, 51

Physical Design – Sessions: 19, 27, 34

Synthesis and FPGA – Sessions: 18, 23, 43, 46, 49, 52

System Level and Embedded – Sessions: 3, 8, 13, 25, 28, 35, 37, 40, 42, 44, 53 / Tutorial 2

Verification and Test – Sessions: 5, 11, 30, 33, 38, 41, 48 / Tutorial 3

Sunday, June 3, 2007

EDA Consortium Executive Reception
at the San Diego Marriott Hotel and Marina/ Marina Ballroom
5:00pm - 7:00pm

Rm: 6C	Rm: 6D	Rm: 6E	Rm: 6F
4th UML for SoC Design Workshop 9:00am - 5:30pm	**Low Power Coalition Workshop - Standards for Low Power Design Intent** 12:30pm - 3:30pm	**Design and Verification of Low Power ICs** 4:00pm - 7:00pm	**Hardware Dependent Software (HdS)** 1:00pm - 7:30pm

Monday, June 4, 2007

Free Monday - 9:00am – 6:00pm - Visit the exhibition for free

	Rm: 6C	Rm: 6D	Rm: 11A	Rm: 6A			DAC Pavilion
9:00	**Tutorial 1** Anatomy of Variability and Making of "Variation Tolerance" Vaccine in Nanometer Technologies	**Tutorial 2** System Design for Multimedia Applications - Challenges, Design Methods and Recent Developments	**Hands-on-Tutorial** Standard Cell Library and Hard IP Design *Blaze DFM, Inc.* *Ponte Solutions, Inc.* *Sagantec*	3rd Integrated Design Systems Workshop: Models for Design and Manufacturing - How Modeling Challenges are Touching Every Aspect of IC Design 12:00pm - 5:00pm	Workshop for Women in Design Automation: *Managing Your Career* 9:00am – 1:45pm • Room 8	Introduction to Chips and EDA for a Non-Technical Audience 10:00am – 12:00pm • Room 9	**Booth #6360**
10:00							Gary Smith on EDA: Trends & What's Hot at DAC? **9:30am – 10:30am**
12:00	**Lunch** (Rm: 1AB)	**Lunch** (Rm: 1AB)					EDA Exit Strategies: What's Next **10:45am – 11:45pm**
2:00	Organizers: **Ruchir Puri** **Samuel Naffziger** Speakers: **Hisashige Ando** **Tanay Karnik** **Lawrence T. Pileggi** **Mike Clinton** **Richard Klein**	Organizer: **Radu Marculescu** Speakers: **Mihaela van der Schaar** **Radu Marculescu** **Remus Albu**	**Hands-on-Tutorial** Design for Manufacturing Variability with Confidence *ClearShape Technologies, Inc.* *Cadence Design Systems, Inc.* *Texas Instruments Inc., UMC*		**Monday Keynote Speaker** ***Designing a New Automotive DNA*** **Lawrence D. Burns** - *Vice President of Research & Development and Strategic Planning, General Motors Corp.* 2:00pm – 3:00pm • Ballroom 20ABC		Student Design Contest Award Presentations **12:00pm – 1:00pm**
5:00							Hogan's Heroes: What We Hear and See in Optimized Timing and Power in 2007 **2:00pm – 3:00pm**
							Just Who is Providing the IP? **3:15pm – 4:00pm**
							Anticipating the Next Killer App: Is There an iPhone in Your Future? **4:15pm – 5:00pm**

IEEE Council on EDA's Distinguished Speaker Lecture and Reception in the Sails Pavilion from 6:00pm – 8:00pm

Tuesday, June 5, 2007

Exhibit Hours - 9:00am – 6:00pm

General Session and Keynote Speaker — Ballroom 20ABC

Perspective of the Future Semiconductor Industry: Challenges and Solutions
Oh-Hyun Kwon - President, System LSI Division, Samsung Semiconductor Business

8:30 to 10:15

BREAK 10:15am - 10:30am • Management Seminar - Innovation or Extinction - The Choice Is Yours! - 10:30 AM - 6:45 PM | Room: 6A

HOTs Rm: 11A

Deploying Statistical Timing – from Characterization to Analysis and Optimization
Altos Design Automation/Cadence Design Systems, Inc.

DAC Pavilion
Booth #6360

- Career Advancement for Technologists: An Interview with the Marie R. Pistilli Woman in EDA Award Winner **10:15am - 11:00am**
- Managing Mixed-Signal Designs: What's Working? What's Missing? **11:15am - 12:00pm**
- Deploying Formal: When and Where? **2:00pm - 3:00pm**
- ESL for Wireless **3:15pm - 4:15pm**
- To Be or Not To Be Compliant: That is the Question **4:30pm - 5:30pm**

Rm: 6B	Rm: 6C	Rm: 6D	Rm: 6E	Rm: 6F	
Session 1	**Session 2**	**Session 3**	**Session 4**	**Session 5**	10:30 to 12:00
SPECIAL SESSION: Trusted Hardware	**PANEL SESSION:** Mega Trends and EDA 2017	Industrial Application of System Level Methods	Novel Techniques for Interconnect	Formal & Semi-Formal Verification Techniques	

LUNCH 12:00pm - 2:00pm

Session 6	Session 7	Session 8	Session 9	Session 10	2:00 to 4:00
Leakage Power Analysis & Optimization	**PANEL SESSION:** Making Manufacturing Work for You	Energy & Performance Issues in On-Chip Communication Networks	Circuit Simulation	Signal & Power Delivery Integrity	

BREAK 4:00pm - 4:30pm

Session 11	Session 12	Session 13	Session 14	Session 15	4:30 to 6:30
SPECIAL SESSION: Functional Verification of ESL Models	**PANEL SESSION:** Early Power-Aware Design and Validation: Myth or Reality	Memories in Embedded Systems	Statistical Techniques for Timing Analysis and Design	**SPECIAL SESSION:** Wild And Crazy Ideas	

SIGDA Ph.D. Forum and Member Meeting in the Sails Pavilion from 6:30pm - 8:00pm

Presenters will be available in Room 1AB for additional 20-minute question-and-answer periods after each session. ☐ **Of special interest to designers**

Session Tracks: Analog/Mixed-Signal/RF and Simulation | Business | DFM and the Manufacturing Interface | Interconnect and Reliability | Low Power Design | Automotive Theme | New and Emerging Technologies | Physical Design | Synthesis and FPGA | System Level and Embedded | Verification and Test

Wednesday, June 6, 2007

Exhibit Hours - 9:00am – 6:00pm

	Rm: 6B	Rm: 6C	Rm: 6E	Rm: 6F	Rm: 6A
	Session 16	**Session 17**	**Session 18**	**Session 19**	**Session 20**
8:30 to 10:00	Distributed Computing: Automotive Network Design & Analysis	Emerging Nanoscale Hybrid Circuits & Architectures	Physical Implementation of FPGAs	Process Aware Physical Design	Reliable Design & CAD Solutions for Circuit Aging
	BREAK 10:00am - 10:30am				
	Session 21	**Session 22**	**Session 23**	**Session 24**	**Session 25**
10:30 to 12:00	**INVITED SESSION:** Silicon, Safety and Self-Driving Cars	**SPECIAL SESSION:** Silicon Measurement Correlation to Reliability	Optimizing Arithmetic & Communication	Analog & RF Simulation	**PANEL SESSION:** TLM: Crossing Over from Buzz to Adoption
	LUNCH 12:00pm - 2:00pm				
	Session 26	**Session 27**	**Session 28**	**Session 29**	**Session 30**
2:00 to 4:00	**PANEL SESSION:** Electronics: The New Differential in the Automotive Industry	Modern Placement Techniques	Advances in Embedded Hardware Design	Bridging the Gap with Silicon	Practical Solutions for Power-Aware Testing
	BREAK 4:00pm - 4:30pm				
	Session 31	**Session 32**	**Session 33**	**Session 34**	**Session 35**
4:30 to 6:30	**SPECIAL SESSION:** Virtual Automotive Platforms	**SPECIAL SESSION:** The Future of Interconnects	Advances in Decision Procedures	3D IC & Package Design Issues	**PANEL SESSION:** Corezilla: Build and Tame the Multicore Beast

HOTs

Rm: 11A

Approaching Yield in the Nanometer Age: *Mentor Graphics Corp./ Chartered Semiconductor Manufacturing/ Sierra Design Automation, Inc./ARM Ltd.*

Rm: 11A

Manufacturing Aware Optimization *Blaze DFM, Inc./Taiwan Semiconductor Manufacturing Company, Ltd.*

DAC Pavilion

Booth #6360

The Urban Challenge: Paving the Way for Driverless Automobiles
9:30am - 10:15am

Improving Automotive Competitiveness: New Methods and Tools For Embedded Design
11:00am - 12:00pm

Electronics: The Key to Disruption of Automobile Powertrain Technology
1:00pm - 1:45pm

DFM: Prevention or Cure
2:00pm - 3:00pm

On a Crash Course: Validation and Testing of Automotive Software
3:15pm - 4:15pm

The One Ton Mobile Platform: Where is it Taking Us?
4:30pm - 5:30pm

Wednesday Night Party • 7:00pm - 10:00pm • Sails Terrace, San Diego Convention Center

Presenters will be available in Room 1AB for additional 20-minute question-and-answer periods after each session. ☐ **Of special interest to designers**

Session Tracks: **Analog/Mixed-Signal/RF and Simulation** **Business** **DFM and the Manufacturing Interface** **Interconnect and Reliability** **Low Power Design** **Automotive Theme** **New and Emerging Technologies** **Physical Design** **Synthesis and FPGA** **System Level and Embedded** **Verification and Test**

Thursday, June 7, 2007

Exhibit Hours - 9:00am – 1:00pm

Hands On Tutorial	Rm: 6B	Rm: 6C	Rm: 6D	Rm: 6E	Rm: 6F	Rm: 6A	
Timing Closure: Requirements for Variation Aware Design *Extreme DA Corp./ Texas Instruments Inc./ PDF Solutions/UMC* **9:00am - 12:00pm** **Rm: 11A**	**Session 36**	**Session 37**	**Session 38**	**Session 39**	**Session 40**	**Session 41**	
	SPECIAL SESSION: Synthetic Biology	Programming & Scheduling Embedded Systems	Emerging Test Solutions	Circuit Level Power Analysis & Low Power Design	Parameter Tuning in System Architecture Exploration	**PANEL SESSION:** Verification Coverage: When is Enough Enough?	9:00 to 11:00
DAC Pavilion	**LUNCH 11:00am - 12:30pm**						
Booth #6360	**Best Paper Award Presentations and Keynote Speaker** — Ballroom 20ABC						12:30 to 1:45
P-cells or Free Cells **10:15am - 11:15am**	**Design without Borders – A Tribute to the Legacy of A. Richard Newton** *Jan M. Rabaey* - Donald O. Pederson Distinguished Professor, University of California, Berkeley						
	Session 42	**Session 43**	**Session 44**	**Session 45**	**Session 46**	**Session 47**	
Foyer Ballroom 20	**SPECIAL SESSION:** Thousand-Core Chips	Communication-Based Resource Allocation	Embedded Processor & MPSoC Design	Modeling Technology Impact	Technology Mapping & Physical Synthesis	System-Level Power Management & Analysis	2:00 to 4:00
Book Signing Session **12:00pm - 12:30pm**	**BREAK 4:00pm - 4:30pm**						
	Session 48	**Session 49**	**Session 50**	**Session 51**	**Session 52**	**Session 53**	
	Dynamic Verification of Processors & Processor-Based Designs	FPGA Tools & Methodologies	Mixed-Signal Modeling, Methodology & Synthesis	Design Methods & Manufacturability Solutions for Emerging Technologies	High-Performance Synchronization Techniques	**PANEL SESSION:** IP Exchange	4:30 to 6:00

Presenters will be available in Room 1AB for additional 20-minute question-and-answer periods after each session. ☐ **Of special interest to designers**

Session Tracks: **Analog/Mixed-Signal/RF and Simulation** **Business** **DFM and the Manufacturing Interface** **Interconnect and Reliability** **Low Power Design** **Automotive Theme** **New and Emerging Technologies** **Physical Design** **Synthesis and FPGA** **System Level and Embedded** **Verification and Test**

Friday, June 8, 2007

Tutorial Schedule

Breakfast - 8:00am - 9:00am in Rm: 1AB
Tutorial - 9:00am - 12:00pm

Lunch - 12:00pm - 1:00pm in Rm: 1AB
Tutorial - 1:00pm - 5:00pm

	Rm: 6F	Rm: 6A	Rm: 6C	Rm: 6D	Rm: 6E
9:00 to 5:00	**TUTORIAL 3** Formal Assertion Based Verification in an Industrial Setting Organizer: **Raj S. Mitra** Speakers: **Alok Jain** **Raj S. Mitra** **Jason Baumgartner** **Pallab Dasgupta**	**TUTORIAL 4** Design and Analysis of High-Performance Package and Die Power Delivery Networks Organizer: **Eli Chiprout** Speakers: **Byron Krauter** **Farid N. Najm** **Rajendran Panda** **Eli Chiprout**	**TUTORIAL 5** Soft Errors: Technology Trends, System Effects and Design Techniques Organizer: **Subhasish Mitra** Speakers: **Subhasish Mitra** **Pia N. Sanda** **Austin Lesea**	**TUTORIAL 6** How Design Meets Yield in the Fab Organizers: **Patrick Groeneveld** **Andrew B. Kahng** Speakers: **Ankush Oberai** **Pallab Chatterjee** **Ban Wong** **Robert Madge** **Christopher Progler** **Brady Benware**	**TUTORIAL 7** Circuit and CAD Techniques for Low Power Design Organizers: **David Blaauw** **Anantha Chandrakasan** Speakers: **Krisztian Flautner** **Alice Wang** **Nam Sung Kim** **David Blaauw**

☐ **Of special interest to designers**

Session Tracks: **Analog/Mixed-Signal/RF and Simulation** **Business** **DFM and the Manufacturing Interface** **Interconnect and Reliability** **Low Power Design** **Automotive Theme** **New and Emerging Technologies** **Physical Design** **Synthesis and FPGA** **System Level and Embedded** **Verification and Test**

DAC Pavilion Panels - Booth #6360

Monday, June 4, 9:30am – 10:30am

Gary Smith on EDA: Trends & What's Hot at DAC?

Moderator: **Robert Gardner** - *EDA Consortium, San Jose, CA*
Speaker: **Gary Smith** - *Gary Smith EDA, Santa Clara, CA*

An annual review of the technology trends in electronic design. What are the trends shaping design in the next 5 years? Will DFM and ESL be the hot topics again? What about multi-core design? Will SW engineers ever pay top dollar for EDA tools? What acquisitions were critical in 2006 and what are the ones to watch in 2007? What are the hot products that are 'must sees'? Do you have a question that needs an independent analysis? Q&A will follow.

Monday, June 4, 10:45am – 11:45am

EDA Exit Strategies: What's Next?

Moderator: **Kathryn Kranen** - *Jasper Design Automation, Inc.; Vice Chair, EDA Consortium, Mountain View, CA*
Speakers: **Rajeev Madhavan** - *Magma Design Automation, Inc., Santa Clara, CA*
Andrew Yang - *Apache Design Solutions, Inc., Mountain View, CA*
Jay Vleeschhouwer - *Merrill Lynch & Co., Inc., New York, NY*

The environment today is dominated by a drought in IPO's. At the large companies M&A activity has slowed. Leveraged buyouts are the chosen path in the semi industry, and the Sarbanes-Oxley Act is making being a public company an undesirable place to be. How does all this impact EDA startups today? Should startups stay private and grow organically? What are the other choices for exit strategies?

Monday, June 4, 12:00pm – 1:00pm

Student Design Contest Award Presentations

Moderator: **Alan Mantooth** - *Univ. of Arkansas, Fayetteville, AR*

Presentation of the nine student design award winners, spanning conceptual and two operational categories of the Student Design Contest, organized by the Design Automation Conference and the International Solid-State Circuits Conference (ISSCC). Award Contributors: ACM/SIGDA, Cadence Design Systems, Inc., IEEE Council on EDA, Intel Corp., Mentor Graphics Corp., Semiconductor Research Corp., Synopsys, Inc. and Tanner EDA.

Monday, June 4, 2:00pm – 3:00pm

Hogan's Heroes: What We Hear and See in Optimized Timing and Power in 2007

Moderator: **James Hogan** - *Board Director/Investor, San Jose, CA*
Speakers: **Paul Cunningham** - *Azuro, Inc., San Jose, CA*
Shishpal S. Rawat - *Intel Corp., Folsom, CA*
Sudhakar Sabada - *LSI Logic, Inc., Milpitas, CA*

Come listen to Jim Hogan grill key EDA technologists about your critical SoC design challenges. This year we will expand the focus to examine simultaneous optimization of timing and power across the entire design flow. Is the power problem solved and is timing now the real issue? How do you get the design engineer the information he needs early enough to plan for power and timing prior to implementation? No one will leave the panel saying they know nothing.

Monday, June 4, 3:15pm – 4:00pm

Just Who is Providing the IP?

Moderator: **Peggy Aycinena** - *EDA Confidential, San Mateo, CA*
Speakers: **Philippe Magarshack** - *STMicroelectronics, Crolles Cedex, France*
Mike Muller - *ARM Ltd, Cambridge, United Kingdom*

The market for IP has not grown to its full potential. The restraining factor is that the design community still develops its own solutions rather than reusing what is commercially available. This practice, rather than decreasing with the advent of high-quality, standards-based commercial IP, is on the rise. There are some exceptions, such as processors and memory models, but on the whole, semiconductor manufacturers continue to develop their own IP. When time to market is so important, why is this?

Monday, June 4, 4:15pm – 5:00pm

Anticipating the Next Killer App: Is There an iPhone in Your Future?

Moderator: **Ed Sperling** - *Electronic News , San Jose, CA*
Speakers: **Vojin Zivojnovic** - *ARM Ltd, Cambridge, United Kingdom*
Edward Valdez - *Parrot SA , Austin, TX*

How do consumer electronics companies develop the next disruptive device? Key technologists reveal their experiences regarding how the initial planning meetings ensue, the process behind creating a winning design team, and the decisions regarding when to bring in partners to begin the process of creating an ecosystem of support around the device.

DAC Pavilion Panels - Booth #6360

Tuesday, June 5, 10:15am – 11:00am

Career Advancement for Technologists: An Interview with the Marie R. Pistilli Woman in EDA Award Winner

Moderator: **William H. Joyner, Jr.** - *IBM Corp./SRC, Research Triangle Park, NC*
Speaker: **Marie R. Pistilli Award Winner:**
Jan Willis - *Cadence Design Systems, Inc., San Jose, CA*

You're a technologist. How should you optimize your career trajectory? That extra degree: should it be technical or business? Those extra courses: technology, management, or time management? Those opportunities for committee work, service and networking: do you pick the inter-company, intra-company, or industry committee? This award winner will offer her advice on what pays off and what doesn't - and the skills that mid-career technologists need to advance their careers. This year's Marie R. Pistilli Award Winner is Jan Willis, Senior Vice President, Industry Alliances, Cadence Design Systems, Inc., San Jose, California.

Tuesday, June 5, 11:15am – 12:00pm

Managing Mixed-Signal Designs: What's Working? What's Missing?

Moderator: **Gabe Moretti** - *Gabe On EDA, Venice, FL*
Speakers: **Warren P. Snapp** - *Boeing Phantom Works, Tacoma, WA*
Mohamed K. Mahmoud - *Texas Instruments Inc., Dallas, TX*

Moore's Law is great for digital design, but a challenge for analog/RF. Yet most of today's most interesting chips are mixed-signal designs integrating large amounts of computation with impressive analog function. How well are the tools keeping up with the huge challenges of these designs? What is – or is not – working?

Tuesday, June 5, 2:00pm – 3:00pm

Deploying Formal: When and Where?

Moderator: **Limor Fix** - *Intel Corp., Pittsburgh, PA*
Speakers: **Jon Michelson** - *Cisco Systems, Inc., San Jose, CA*
Lawrence Loh - *Jasper Design Automation, Inc., Mountain View, CA*
Prosenjit Chatterjee - *NVIDIA Corp., Santa Clara, CA*

Companies are embracing functional formal verification to ensure greater verification productivity, predictability and verification reuse. Advantages are gained by understanding the types of design best suited for formal verification, and where in the flow this technology should be applied. With an understanding of the characteristics of areas with high formal applicability, users can identify which blocks, portions or functionalities of the blocks will give the greatest return. Formal verification experts share their insights in deploying formal – when and where – for best results.

Tuesday, June 5, 3:15pm – 4:15pm

ESL for Wireless

Moderator: **John Blyler** - *ChipDesign Magazine, Portland, OR*
Speakers: **Vincent Perrier** - *CoFluent Design, Nantes Cedex, France*
James O. Bondi - *Texas Instruments Inc., Dallas, TX*

More and more, today's wireless designers are turning to ESL design tools to solve the growing performance and complexity issues. There's no doubt the design of wireless infrastructure systems is not getting any easier. Cellular systems are already packing voice, video and data services on the same link. Then add voice-over-IP (VoIP) and complexity rises. This panel will discuss and debate what ESL is doing today to aid wireless design, and what more is needed tomorrow.

DAC Pavilion Panels - Booth #6360

Tuesday, June 5, 4:30pm – 5:30pm

To Be or Not To Be Compliant: That is the Question

Moderator: **Sanjay Srivastava -** *Denali Software, Inc., Palo Alto, CA*
Speakers: **Rob Genco -** *Synopsys, Inc., Mountain View, CA*
Jeff Klaben - *Cadence Design Systems, Inc., San Jose, CA*
Lee Levenson - *Centralized Enterprise Licensing Users Group, Pasadena, CA*

With the continuing globalization of the enterprise company's design community, it is becoming increasingly difficult to verify, manage, and ensure compliance to contractual obligations set forth in the software publisher's license agreements. This panel will elicit and discuss the challenges facing both EDA and enterprise design companies to effectively verify and manage compliance of networked software, including such topics as linkage of complex software license agreement terms to actual usage, external vs. internal self-audit, and suitability of existing or other license management solutions to help address this growing issue.

Wednesday, June 6, 9:30am – 10:15am

The Urban Challenge: Paving the Way for Driverless Automobiles

Moderator: **Yatin Trivedi -** *Magma Design Automation, Inc., San Jose, CA*
Speaker: **Dave Ferguson -** *Intel Corp./Carnegie Mellon Univ., Pittsburgh, PA*

The Urban Challenge competition focuses on exploring fully-autonomous passenger vehicles that conduct navigation missions in urban environments. The goal of the Urban Challenge is to develop vehicles that can safely drive themselves in realistic urban settings. To succeed, the vehicles must obey traffic laws while safely merging into moving traffic, driving through traffic circles and busy intersections, and parking in parking lots. A multi-media presentation and demonstration of Carnegie Mellon University's entry into the Urban Challenge will provide an example of current results.

Wednesday, June 6, 11:00am – 12:00pm

Improving Automotive Competitiveness: New Methods and Tools For Embedded Design

Moderator: **Marios Zenios -** *Alto Consulting, Minneapolis, MN*
Speakers: **George Saikalis -** *Hitachi America, Ltd., , Farmington Hills , MI*
Frank Winters - *Delphi Electronics and Safety, Kokomo, IN*
Jon Friedman - *The MathWorks, Inc., Natick, MA*

Electronic control unit embedded designs are growing at an exponential rate in the automotive industry. The software component of these designs is growing even faster. By 2015 there will be more then 100 million lines of code in a high-end car. Automobile manufactures will live and die based on the functionality, efficiency and quality of their embedded designs. This panel explores how automotive leaders and their suppliers are changing embedded design methods and tools to improve their competitiveness.

Wednesday, June 6, 1:00pm – 1:45pm

Electronics: The Key to Disruption of Automobile Powertrain Technology

Moderator: **Marvin E. Bush -** *Chief Business Operations, Wrightspeed, Inc.*
Presenter: **Ian Wright -** *Founder & CEO, Wrightspeed, Inc.*

Electronics is the key to an imminent disruption in automobile powertrain technology.

The core technology of auto manufacturers is the mechanical powertrain - piston engines and transmissions. Most of the energy in the fuel is wasted as heat. Electronics is relegated to control, monitoring, and entertainment functions.

That's about to change. The power will come directly from moving electrons, switched by IGBTs, waveshaped by DSPs. No clutches, no gearshifting, no pistons. No tradeoff between power and efficiency. 1,000 hp and 100mpg equivalent is possible in the same car.

DAC Pavilion Panels - Booth #6360

Wednesday, June 6, 2:00pm – 3:00pm

DFM: Prevention or Cure

Moderator: **Nagaraj NS** - *Texas Instruments Inc., Dallas, TX*
Speakers: **Rich Brashears** - *Cadence Design Systems, Inc., San Jose, CA*
Joe Sawicki - *Mentor Graphics Corp., Wilsonville, OR*
Wolfgang Fichtner - *Synopsys, Inc., Mountain View, CA*

EDA customers are faced with a bewildering array of new DFM/DFY technologies. Are manufacturing and yield challenges best solved by "holistic" approaches, implemented in the existing library creation and RTL-to-GDSII flows, and emphasizing preventions over cures? Or should today's challenges be solved by "point" technologies, particularly at the post-GDSII level, and involving sophisticated litho simulations and hotspot fixing? This Pavilion Panel will present a discussion among proponents of the various available approaches: "general contractor" (Cadence), "tradesman" (Mentor) - and "both" (Synopsys).

Wednesday, June 6, 3:15pm – 4:15pm

On a Crash Course: Validation and Testing of Automotive Software

Moderator: **David Smith** - *Synopsys, Inc., Hillsboro, OR*
Speakers: **Raj Rajkumar** - *Carnegie Mellon Univ., Pittsburgh, PA*
S. Ramesh - *General Motors Corp., Bangalore, India*
Bill Milam - *Ford Motor Co., Dearborn, MI*

There is a big gap between how part suppliers (hardware, software) to the automotive industry test their products vs. what a typical customer expects. Not only do the end products need to be validated, but so do the tool chains used to create the products. Left to the current state of the art, this is certainly going to be a limiter to the growth in the industry – witness the number of software-related recalls and repairs by major automotive manufacturers in recent years. The goal of this panel is to explore the special needs for correctness and reliability in automotive software, what the car makers are doing, what the research community is doing, and where the promising developments are.

Wednesday, June 6, 4:30pm – 5:30pm

The One Ton Mobile Platform: Where is it Taking Us?

Moderator: **Ken Karnofsky** - *The MathWorks, Inc., Natick , MA*
Speakers: **Bill Milam** - *Ford Motor Co., Dearborn, MI*
Ivo Bolsens - *Xilinx, Inc., San Jose, CA*
Ingolf Krueger - *Univ. of California, La Jolla, CA*

The automotive industry accounts for increasing share of the semiconductor products, and a modest but growing proportion of EDA tools. How is this shaping the design methods, products and even R&D agenda in semiconductors and EDA? What are the specific chip and embedded software needs that must be served for success in this marketplace? What are the EDA tool needs, and the industry dynamics shaping this growth? At the end of the day, what is the value-add provided by EDA to automotive? Can and should big-three EDA be selling directly to big-three automotive – and if so, how?

Thursday, June 7, 10:15am – 11:15am

P-cells or Free Cells

Moderator: **Mike Santarini** - *EDN Magazine, San Mateo, CA*
Speakers: **Walter Ng** - *Chartered Semiconductor Manufacturing, Milpitas, CA*
James Roberts - *QUALCOMM Inc., Cary, NC*
Ed Petrus - *CiraNova, Santa Clara, CA*

P-cells (parameterized IC layout cells) written in open standard languages promise fundamental changes for analog and custom designers in the way they create and use custom layout. Can p-cells really be free of proprietary languages and databases? A panel of industry experts will debate the promise and the reality of the new approach, allowing you to decide if the technology can deliver the promise. Can p-cells really be free of proprietary languages and databases? What are the benefits of the new approach?

General Session/Keynote Address

Tuesday, June 5, 8:30am – 10:15am **Ballroom 20ABC**

Opening Remarks - **Steven P. Levitan -** *44th DAC General Chair*

A Tribute to A. Richard Newton *by* **Alberto Sangiovanni-Vincentelli** & **Petra Michel**

Awards presented by: **Diana Marculescu,** *ACM/SIGDA Representitive* & **Alan Mantooth,** *IEEE/CASS/CANDE/CEDA Representitive*

Awards/Scholarships

- A. Richard Newton Graduate Scholarships
- Marie R. Pistilli Women in EDA Achievement Award
- P.O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering
- 2006 Phil Kaufman Award for Distinguished Contributions to EDA sponsored by the EDA Consortium
- IEEE Emanuel R. Piore Award
- IEEE Circuits and Systems Society 2007 Industrial Pioneer Award
- IEEE Circuits and Systems Society 2007 Outstanding Young Author Award
- IEEE Transactions on Computer-Aided Design 2007 Donald O. Pederson Best Paper Award
- IEEE Transactions on Circuits and Systems 2007 Guillemin-Cauer Best Paper Award
- 2007 IEEE Fellows
- ACM Paris Kanellakis Theory and Practice Award
- ACM Transactions on Design Automation of Electronic Systems (TODAES) 2007 Best Paper Award
- ACM/SIGDA Distinguished Service Awards
- ACM Outstanding Dissertation in Electronic Design Automation Award
- SIGDA Outstanding New Faculty Award

Keynote Address

Perspective of the Future Semiconductor Industry: Challenges and Solutions

Oh-Hyun Kwon - *President, System LSI Division, Samsung Semiconductor Business*

SESSION 1

RM: 6B

SPECIAL SESSION: TRUSTED HARDWARE

Chair: Patrick Schaumont - *Virginia Polytechnic Inst., Blacksburg, VA*

The trustworthiness of the computing device has become an important consideration during hardware design and fabrication. For instance, devices are increasingly asked to store confidential information. This includes data like cryptographic keys, personal information, and the intellectual property (IP) in the device's design. Furthermore, computing systems in critical applications must work as specified. Therefore it is important that we design and fabricate trusted hardware. There are many potential attacks that can be used to exploit a computing device. Physical attacks, which monitor power, timing, electromagnetic radiation, etc. are known to exist, and can be used to steal confidential information from the system. A "malicious" foundry can perform a number of devious activities including stealing the mask, reverse engineering IP, subverting the hardware through back doors and time bombs, and overproducing counterfeit chips. Design tools can be subverted to insert malicious circuitry, and chip packagers can modify selected devices with their own that provide similar functionality, in addition to underhanded behavior, e.g. stealing information or malfunctioning at critical junctures.

This special session looks at the issues and provides some initial solutions for designing trusted hardware. The session is organized into four talks. The first talk will discuss potential attacks at the various stages of the hardware lifecycle. The next three speakers will present solutions to these attacks for different classes of hardware including microprocessors, FPGAs and ASICs.

1.1s Challenges for Trusted Hardware
Karl Levitt - *National Science Foundation, Arlington, VA*
Cynthia E. Irvine - *Naval Post Graduate School, Montery, CA*

1.2s Trusted Design in FPGAs
Steve Trimberger - *Xilinx Research Labs, San Jose, CA*

1.3 Physical Unclonable Functions for Device Authentification and Secret Key Generation
G. Edward Suh - *Cornell Univ., Ithaca, NY*
Blaise Gassend, Dwaine Clarke, Martin van Dijk, Jae W. Lee, Daihyun Lim, Srinivas Devadas - *Massachusetts Institute of Tech., Cambridge, MA*

1.4 Side-Channel Attack Pitfalls
Kris Tiri - *Intel Corp., Hillsboro, OR*

SESSION 2

RM: 6C

PANEL: MEGATRENDS AND EDA 2017

Chair: Greg Spirakis - *Retired Intel Corp., Currently Board Member at ArchPro, Saratoga, CA*
Organizer: Francine Bacchini

Today's megatrends: consumer cycles at 6-12 months (and getting faster), process technology accelerating through 45nm (but with higher risks and lower yields), fewer platform SOCs (each requiring more specialized hardware and software design tools), the search for 3-4 more "waves" for the semiconductor industry to ride to $1T by the end of the CMOS roadmap, design as a key enabler of Moore's Law and "more than Moore" value. What do these megatrends imply for the future of EDA?

Panelists:
Juan Antonio Carballo - *Argon Capital , Redwood City, CA*
Aart de Geus - *Synopsys, Inc. , Mountain View, CA*
Fu-Chieh Hsu - *Taiwan Semiconductor Manufacturing Co. , Hsinchu, Taiwan*
Kurt Keutzer - *Univ. of California , Berkeley, CA*
Kazu Yamada - *NEC Electronics America, Inc. , Santa Clara, CA*

SESSION 3

RM: 6D

INDUSTRIAL APPLICATION OF SYSTEM LEVEL METHODS

Chair: Grant Martin - *Tensilica Inc., Santa Clara, CA*

Industry is always looking to bridge the hardware-software divide by bringing together practical design methods and technologies that academia has formalized and stabilized. The papers in this session describe attempts to bring such methods into practice. Subjects include efficient hardware-software co-design using task-transaction level abstractions, formalizing the validation of complex system models, extensions to SystemC for process control and software modeling and a multimedia case study of MPSoC design with Simulink.

3.1 System-Level Design Flow Based on a Functional Reference for HW and SW
Walter Tibboel, Victor Reyes, Martin Klompstra, Dennis Alders - *NXP Semiconductors, Eindhoven, Netherlands*

3.2 Model-Driven Validation of SystemC Designs
Hiren D. Patel, Sandeep K. Shukla - *Virginia Polytechnic Inst., Blacksburg, VA*

3.3s Language Extensions to SystemC: Process Control Constructs
Bishnupriya Bhattacharya- *Cadence Design Systems, Inc., San Jose, CA*
John L. Rose - *Cadence Design Systems, Inc., Longmont, CO*
Stuart Swan - *Cadence Design Systems, Inc., San Jose, CA*

3.4s Simulink-Based MPSoC Design Flow: Case Study of Motion-JPEG and H.264
Kai Huang - *Zhejiang Univ., Hangzhou, China*
Sangil Han - *Seoul National Univ., Seoul, South Korea*
Katalin Popovici - *TIMA Labs., Grenoble, France*
Lisane Brisolara - *Univ. Rio Grande do Sul, Porto Alegre, Brazil*
Xavier Guerin - *TIMA Labs., Grenoble, France*
Lei Li, Xiaolang Yan - *Zhejiang Univ., Hangzhou, China*
Soo-Ik Chae - *TIMA Labs., Grenoble, France*
Luigi Carro - *Univ. Rio Grande do Sul, Porto Alegre, Brazil*
Ahmed A. Jerraya - *CEA-LETI MINATEC, Grenoble, France*

SESSION 4

RM: 6E

NOVEL TECHNIQUES FOR INTERCONNECT

Chair: Jiang Hu - *Texas A&M Univ., College Station, TX*

This session presents solutions to various interconnect-related issues. The first paper illustrates how a novel clocking scheme can be applied to real-life chip design. The following paper addresses routability and runtime by pre-routing dense pins using a multi-commodity flow formulation. A yield-driven track routing methodology is presented in the third paper. The final paper presents an original approach to feeding back routing congestion into placement.

4.1 Design of Rotary Clock Based Circuits
Zhengtao Yu, **Xun Liu** - *North Carolina State Univ., Raleigh, NC*

4.2 Escape Routing For Dense Pin Clusters In Integrated Circuits
Mustafa Ozdal - *Intel Corp., Hillsboro, OR*

4.3s TROY: Track Router with Yield-driven Wire Planning
Minsik Cho - *Univ. of Texas, Austin, TX*
Hua Xiang, Ruchir Puri - *IBM Corp., Yorktown Heights, NY*
David Z. Pan - *Univ. of Texas, Austin, TX*

4.4s IPR: An Integrated Placement and Routing Algorithm
Min Pan - *Cadence Design Systems, Inc., San Jose, CA*
Chris Chong-Nuen Chu - *Iowa State Univ., Ames, IA*

SESSION 5

RM: 6F

FORMAL AND SEMI-FORMAL VERIFICATION TECHNIQUES

Chair: Magdy S. Abadir - *Freescale Semiconductor Inc., Austin, TX*

This session hosts papers presenting advances in blending formal, semi-formal, and dynamic techniques for validation. The first paper presents a strategy for using formal engines to guide simulation. The second paper bring formal and semi-formal techniques to performance, rather than functional, validation. The last paper highlights challenges in handling local variables efficiently in the SVA-to-formal path.

5.1 An Effective Guidance Strategy for Abstraction-Guided Simulation
Flavio M. De Paula, Alan J. Hu - *Univ. of British Columbia, Vancouver , BC, Canada*

5.2 Leveraging Semi Formal and Sequential Equivalence Techniques for Multimedia SoC Performance Validation
Lovleen Bhatia, Jayesh Gaur, Praveen Tiwari, Raj S. Mitra, Sunil H. Matange - *Texas Instruments Inc., Bangalore, India*

5.3 Synthesizing SVA Local Variables for Formal Verification
Jiang Long - *Mentor Graphics Corp., San Jose, CA*
Andrew Seawright - *Mentor Graphics Corp., Wilsonville, OR*

SESSION 6

RM: 6B

LEAKAGE POWER ANALYSIS AND OPTIMIZATION

Chair: Kanak Agarwal - *IBM Corp., Austin, TX*

This session includes several interesting papers covering topics related to leakage analysis and optimization. The first two papers look at the problem of sleep-transistor sizing for leakage minimization and effects of random dopant induced threshold voltage shift. The next two papers address the problem of full-chip leakage power analysis, while the last one looks at the problem of minimizing leakage in sequential circuits.

6.1 Fine-Grained Sleep Transistor Sizing Algorithm for Leakage Power Minimization
De-Shiuan Chiou, Da-Cheng Juan, Yu-Ting Chen, Shih-Chieh Chang - *National Tsing-Hua Univ., Hsinchu, Taiwan*

ß **6.2 Width-dependent Statistical Leakage Modeling for Random Dopant Induced Threshold Voltage Shift**
Jie Gu, Sachin S. Sapatnekar, **Chris Kim** - *Univ. of Minnesota, Minneapolis, MN*

6.3 Modeling and Estimation of Full-Chip Leakage Current Considering Within-Die Correlation
Khaled R. Heloue, Navid Azizi, Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*

6.4s Statistical Analysis of Full-Chip Leakage Power Considering Junction Tunneling Leakage
Tao Li - *Tsinghua Univ., Beijing, China*

6.5s Skewed Flip-Flop Transformation for Minimizing Leakage in Sequential Circuits
Jun Seomun, Jaehyun Kim, Youngsoo Shin - *KAIST, Daejeon, South Korea*

SESSION 7

RM: 6C

PANEL: MAKING MANUFACTURING WORK FOR YOU

Chair: Ruchir Puri - *IBM Corp., Yorktown Heights, NY*
Organizer: Srikanth Venkataraman

How can the semiconductor industry improve the communication between what is done up front in the design, and what is done downstream in the fab and during test? This panel will examine whether product test can provide the necessary "grand unification" to solve today's broken handoffs between DFM, test chips, and fab yield management systems. Questions addressed include: What does the "grand unification" look like? Who are the key stakeholders and their roles in this unification? What new value, benefit and ROI will stakeholders realize from their roles? What is the "gap" of technologies and data flows that need to be deployed to make this work? In what order and when will we see these appear? And what are the limiters to this vision?

Panelists:
Steve Griffith - *Syntricity, San Diego, CA*
Bob Madge - *LSI Logic Corp., Milpitas, CA*
Walter Ng - *Chartered Semiconductor Manufacturing , Milpitas, CA*
Ankush Oberai - *Magma Design Automation, Inc., San Jose, CA*
Greg Yeric - *Synopsys, Inc., Mountain View, CA*
Yervant Zorian - *Virage Logic Corp., Fremont, CA*

SESSION 8

RM: 6D

ENERGY AND PERFORMANCE ISSUES IN ON-CHIP COMMUNICATION NETWORKS

Chair: Robert Dick - *Nothwestern Univ., Evanston, IL*

NoCs are a hot topic these days. Indeed, enabling on-chip communication via a network approach is crucial for integrating hundreds or thousands of IP cores in future systems on chip. The papers in this session cover techniques which can support various communication scenarios. Two papers address the energy/performance tradeoff achievable with Voltage/Frequency Islands. Two other papers present routing techniques for improving on-chip throughput and supporting guaranteed QoS. The last paper investigates ways to achieve high bandwidth by considering photonic NoCs.

8.1 Voltage-Frequency Island Partitioning for GALS-based Networks-on-Chip
Umit Y. Ogras, Radu Marculescu, Puru Choudhary, Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

8.2 Introducing the SuperGT Network-on-Chip
Theodore Marescaux - *IMEC, Leuven, Belgium*
Henk Corporaal - *Eindhoven Univ. of Tech., Eindhoven, Netherlands*

8.3 Layered Switching for Networks on Chip
Zhonghai Lu, Ming Liu, Axel Jantsch - *Royal Institute of Tech., Stockholm, Sweden*

8.4s Energy-Aware Synthesis of Networks-on-Chip Implemented with Voltage Islands
Lap Fai Leung, **Chi Ying Tsui** - *Univ. of Hong Kong, Hong Kong*

8.5s The Case for Low-Power Photonic Networks on Chip
Assaf Shacham, Keren Bergman, Luca P. Carloni - *Columbia Univ., New York, NY*

SESSION 9

RM: 6E

CIRCUIT SIMULATION

Chair: L. Miguel Silveira - *INESC-ID, Lisboa, Portugal*

This session surveys numerous aspects of contemporary circuit simulation. Papers discuss characterization and analysis of latches, parameter variation in oscillators, a new waveform model for gate-level timing analysis, and progress in reduction of circuits formulated as second order systems.

9.1 Interdependent Latch Setup/Hold Time Characterization via Euler-Newton Curve Tracing on State-Transition Equations.
Shweta Srivastava, Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*

9.2 PV-PPV: Parameter Variability Aware, Automatically Extracted, Nonlinear Time-Shifted Oscillator Macromodels
Zhichun Wang, Xiaolue Lai, Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*

9.3 Accurate Waveform Modeling using Singular Value Decomposition with Applications to Timing Analysis
Anand Ramalingam, Ashish Kumar Singh - *Univ. of Texas, Austin, TX*
Sani R. Nassif - *IBM Corp., Austin, TX*
Michael Orshansky, David Z. Pan - *Univ. of Texas, Austin, TX*

9.4s Simulating Improbable Events
Suwen Yang, **Mark Greenstreet** - *Univ. of British Columbia, Vancouver, BC, Canada*

9.5s SBPOR: Second-Order Balanced Truncation for Passive Order Reduction of RLC Circuits
Boyuan Yan, Sheldon X.-D. Tan, PU Liu - *Univ. of California, Riverside, CA*
Bruce McGaughy - *Cadence Design Sytems, Inc., San Jose, CA*

SESSION 10

RM: 6F

SIGNAL AND POWER DELIVERY INTEGRITY

Chair: Eli Chiprout - *Intel Corp., Hilsboro, OR*

This session deals with noise and reliability issues in signal and power lines. The first paper presents a technique that simultaneously sizes power wires and adds decaps. The second paper presents a new hierarchical methodology for multi-level on-chip voltage conversion. The third paper deals with the effects of signal integrity on timing analysis. The fourth paper presents a more practical approach for twisted bundle interconnect. The last paper addresses the effects of inductive coupling on delay uncertainty and clock skew.

10.1 On-Chip Decoupling Capacitance and P/G Wire Co-optimization for Dynamic Noise
Min Zhao, Rajendran Panda, Ben Reschke, Yuhong Fu - *Freescale Semiconductor, Inc., Austin, TX*
Trudi Mewett - *Australia Semiconductor Technology Company, Adelaide, Australia*
Sri Chandraskearan, Savithri Sundareswaran, Shu Yan - *Freescale Semiconductor, Inc., Austin, TX*

10.2 Optimal Selection of Voltage Regulator Modules in a Power Delivery Network
Behnam Amelifard, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

10.3 Top-k Aggressors Sets in Delay Noise Analysis
Ravikishore Gandikota, Kaviraj Chopra, David Blaauw, Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*
Murat Becer - *CLK Design Automation Inc., Littleton, MA*

10.4s A New Twisted Differential Line Structure in Global Bus Design
Zhanyuan Jiang, Shiyan Hu, Weiping Shi - *Texas A&M Univ., College Station, TX*

10.5s Effects of Coupling Capacitance and Inductance on Delay Uncertainty and Clock Skew
Abinash Roy, Noha Mahmoud, Masud Chowdhury - *Univ. of Illinois, Chicago, IL*

SESSION 11

RM: 6B

SPECIAL SESSION: FUNCTIONAL VERIFICATION OF ESL MODELS

Chair: Robert B. Jones - *Intel Corp., Hillsboro, OR*

In this session, featuring renowned verification experts from EDA industry and from academia, we will hear about research directions and emerging technologies/methodologies for ESL validation. Papers will cover simulation based verification, directions on how this can be strengthened using formal methods, and formal verification (also addressing correlation to RT-level models).

One of the promises of the emerging ESL paradigm is that it may help to address the constantly-increasing challenge of RTL functional verification. This is because ESL models can be much more abstract and thus simpler to analyze than the corresponding RT level implementation. A validated ESL model can potentially improve and accelerate RTL verification in several ways: it can be used as a "golden" specification for RTL verification, to formally verify ESL -> RTL refinement, or to synthesize correct-by-construction RTL. However, in order to fulfill this promise, the ESL model itself needs to be validated and correlated to the RTL modes.

Significant momentum is building around ESL (Electronic System Level) design. ESL models are usually implemented in extensions to C/C++; the de-facto standard is SystemC. These models have already been applied in several design activities, including early system analysis, SW/HW partitioning, and high-speed system simulation. Yet, the promise of ESL design shift for addressing the RTL verification gap is under-served. It is important to recognize this critical aspect now and encourage EDA and academic work in these directions, as it can take time until research/technology/tools are in place.

ESL based design methodologies affect many aspects of traditional design. Functional verification of ESL models is a pre-requisite for using them in improving RTL verification (which is currently one of the biggest, increasing challenges in logic design). This special session will attract EDA and academic attention to this under-served, yet critically important, aspect of the emerging ESL paradigm.

11.1 Formal Techniques for SystemC Verification
Moshe Y. Vardi - *Rice Univ., Houston, TX*

11.2 Design for Verification at System-Level and RTL
Anmol Mathur, Venkatram Krishnaswamy - *Calypto Design Systems, Inc., Santa Clara, CA*

11.3 ESL Model Validation Support in SystemC
Atsushi Kasuya, Tesh Tesfaye - *JEDA Technologies, Inc., Mountain View, CA*

11.4 Memory Modeling in ESL-RTL Equivalence Checking
Alfred Koelbl, Jerry Burch, Carl Pixley - *Synopsys, Inc., Hillsboro, OR*

SESSION 12

RM: 6C

PANEL: EARLY POWER-AWARE DESIGN AND VALIDATION: MYTH OR REALITY?

Chair: Stephen Bailey - *Mentor Graphics Corp., Longmont, CO*
Organizer: Gila Kamhi, Sarah Miller

Design for low power is crucial for developing and optimizing complex SoCs. Typically, power issues are tackled at the gate-level and backend stages, disconnected from microarchitectural power features or RTL. Industry leaders will debate whether early power-aware design and validation is viable, and which stage of the design process is best for dealing with power issues: gate level and below, or system level.

Panelists:
Steve Curtis - *Intel Corp., Austin, TX*
Juergen Karmann - *Infineon Technologies AG, Munich, Germany*
Stephen Kosonocky - *IBM Corp., Yorktown Heights, NY*
Enrico Macii - *Politecnico di Torino, Torino, Italy*
Wolfgang H. Nebel - *OFFIS Research Institute, Oldenburg, Germany*
YC Wong - *Broadcom, San Diego, CA*

SESSION 13

RM: 6D

MEMORIES IN EMBEDDED SYSTEMS

Chair: Nigel Topham - *Univ. of Edinburgh, Edinburgh, United Kingdom*

Unlike general purpose systems, those that are embedded have particularly stringent memory constraints. Advancements in efficient use of flash memories and memory protection mechanisms, as well as array access parallelization, data organization and on-line cache architecture tuning, will be presented in this exciting session.

ß **13.1 Endurance Enhancement of Flash-Memory Storage Systems: An Efficient Static Wear Leveling Design**
Yuan-Hao Chang - *National Taiwan Univ., Taipei, Taiwan*
Jen-Wei Hsieh - *National Chiayi Univ., Chiayi, Taiwan*
Tei-Wei Kuo - *National Taiwan Univ., Taipei, Taiwan*

13.2 System for Coarse Grained Memory Protection In Tiny Embedded Processors
Ram Kumar Rengaswamy, **Akhilesh Singhania**, Andrew Castner, Eddie Kohler, Mani Srivastava - *Univ. of California, Los Angeles, CA*

13.3 Reducing Off-Chip Memory Access Costs Using Data Recomputation in Embedded Chip Multi-processors
Hakduran Koc - *Syracuse Univ., Syracuse, NY*
Mahmut T. Kandemir - *Pennsylvania State Univ., University Park, PA*
Ehat Ercanli - *Syracuse Univ., Syracuse, NY*
Ozcan Ozturk - *Pennsylvania State Univ., University Park, PA*

13.4s A Memory-Conscious Code Parallelization Scheme
Liping Xue - *Univ. of Delaware, Newark, DE*
Ozcan Ozturk, **Mahmut T. Kandemir** - *Pennsylvania State Univ., University Park, PA*

13.5s A Self-Tuning Configurable Cache
Ann Gordon-Ross, Frank Vahid - *Univ. of California, Riverside, CA*

SESSION 14

RM: 6E

STATISTICAL TECHNIQUES FOR TIMING ANALYSIS AND DESIGN

Chair: Michael Orshansky - *Univ. of Texas, Austin, TX*

Managing variability in design continues to be a big challenge. Statistical techniques are applicable to understand the impact of variability, and enable variability-aware design. This session presents four papers dealing with statistical issues in design. The first paper gives an investigation of the impact of variability-aware optimization and evaluates the importance of using full-fledged statistical techniques for optimization. The next two papers provide improvements on core techniques for statistical timing analysis, including techiques for managing the explosion in the number of variables and methods for speeding up the max operation. The final paper provides a generic technique for constructing highly non-linear response surface models using neural networks.

ß **14.1 Comparative Analysis of Conventional and Statistical Design Techniques**
Steven M. Burns, Mahesh C. Ketkar, Noel Menezes, Keith A. Bowman, James W. Tschanz, Vivek De - *Intel Corp., Hillsboro, OR*

14.2 Fast Second-Order Statistical Static Timing Analysis Using Parameter Dimension Reduction
Zhuo Feng, Peng Li - *Texas A&M Univ., College Station, TX*
Yaping Zhan - *Advanced Micro Devices, Inc., Austin, TX*

14.3 NonLinear Statistical Static Timing Analysis for NonGaussian Variation Sources
Lerong Cheng - *Univ. of California, Los Angeles, CA*
Jinjun Xiong - *IBM Corp., Yorktown Heights, NY*
Lei He - *Univ. of California, Los Angeles, CA*

14.4 Beyond Low-Order Statistical Response Surfaces: Latent Variable Regression for Efficient, Highly Nonlinear Fitting
Amith Singhee, Rob A. Rutenbar - *Carnegie Mellon Univ., Pittsburgh, PA*

SESSION 15

RM: 6F

SPECIAL SESSION: WILD AND CRAZY IDEAS (WACI)

Chair: Lou Scheffer - *Cadence Design Systems, Inc., San Jose, CA*

15.1s Chip Multi-Processor Generator
Alex Solomatnikov, Amin Firoozshahian, Wajahat Qadeer, Ofer Shacham, Zain Asgar, Kyle Kelley, Megan Wachs, Rehan Hameed, Mark Horowitz - *Stanford Univ., Stanford, CA*

15.2s The Case for the Precision Timed (PRET) Machine
Stephen A. Edwards - *Columbia Univ., New York, NY*
Edward A. Lee - *Univ. of California, Berkeley, CA*

15.3s Quantum-Like Effects in Network-on-Chip Buffers Behavior
Paul Bogdan, Radu Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

15.4s CAD-based Security, Cryptography, and Digital Rights Management
Farinaz Koushanfar - *Rice Univ., Houston, TX*
Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

15.5s Line End Shortening is not Always a Failure
Puneet Gupta - *Blaze DFM, Inc., Sunnyvale, CA*
Andrew B. Kahng - *Univ. of California, San Diego, CA*
Youngmin Kim, Saumil Shah, Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*

15.6s You Can Get There From Here: Connectivity of Random Graphs on Grids
Steven P. Levitan - *Univ. of Pittsburgh, Pittsburgh, PA*

15.7s High Performance and Low Power Electronics on Flexible Substrate
Jing Li, Kunhyuk Kang, Aditya Bansal, Kausik Roy - Purdue Univ., West Lafayette, IN

15.8s Novel CNTFET-based Reconfigurable Logic Gate Design
Frédéric Gaffiot - *Ecole Centrale de Lyon, Lyon, France*

All speakers are denoted in bold
S - denotes short paper
ß - denotes best paper candidate

SESSION 16

RM: 6B

DISTRIBUTED COMPUTING: AUTOMOTIVE NETWORK DESIGN AND ANALYSIS

Chair: Antal Rajnak - *Mentor Graphics Corp., Vienna, Austria*

As signal count has risen to implement new automotive electronic functions, so it has become essential to distribute the signals via network buses. Network protocols such as CAN and FlexRay are becoming established. But much remains to be done to model safe yet efficient distributed architectures. The first three papers in this session present new work on period synthesis, timing analysis and jitter relevant to drive-by-wire applications. The fourth paper presents a model-checking approach to schedule optimization.

ß **16.1 Period Optimization for Hard Real-time Distributed Automotive Systems**
Abhijit Davare, Qi Zhu - *Univ. of California, Berkeley, CA*
Marco Di Natale - *General Motors Corp., Warren , MI*
Claudio Pinello - *Cadence Design Systems, Inc., Berkeley, CA*
Sri Kanajan - *General Motors Corp., Warren, MI*
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

16.2s Performance Analysis of FlexRay-based ECU Networks
Andrei Hagiescu, **Unmesh D. Bordoloi**, Samarjit Chakraborty - *National Univ. of Singapore, Singapore*
Prahladavaradan Sampath, P. Vignesh, V. Ganesan, S. Ramesh - *General Motors R&D - ISL, Bangalore, India*

16.3s Experimental Jitter Analysis in a FlexCAN Based Drive-by-Wire Automotive Application
Juan R. Pimentel - *Kettering Univ., Flint, MI*
Jason W. Paskvan - *Mentor Graphics Corp., Farmington Hills, MI*

16.4 Optimization of Static Task and Bus Access Schedules for Time-Triggered Distributed Embedded Systems with Model-Checking
Zonghua Gu, **Xiuqiang He**, Mingxuan Yuan - *Hong Kong Univ. of Science & Tech., Kowloon, Hong Kong*

SESSION 17

RM: 6C

EMERGING NANOSCALE HYBRID CIRCUITS AND ARCHITECTURES

Chair: Mohammad Tehranpoor - *Univ. of Connecticut, Storrs, CT*

This session presents circuit design methodologies and architectures that exploit the synergistic impact of CMOS coupled with other emerging nanotechnologies such as nanotubes, NEMS, and single electron transistors. The first paper describes how an order of magnitude improvement in logic density can be brought about in FPGAs by using distributed embedded nanotube based non-volatile RAMs. The second paper explores the design of ultra low-power circuits using a combination of CMOS and NEMS. The third paper presents a comprehensive SET/CMOS based ultra low-power architecture.

17.1 NanoMap: An Integrated Design Optimization Flow for a Hybrid Nanotube/CMOS Dynamically Reconfigurable Architecture
Wei Zhang - *Princeton Univ., Princeton, NJ*
Li Shang - *Queen's Univ., Kingston, ON, Canada*
Niraj K. Jha - *Princeton Univ., Princeton, NJ*

17.2 Design and Analysis of Hybrid NEMS-CMOS Circuits for Ultra Low-Power Applications
Hamed F. Dadgour, Kaustav Banerjee - *Univ. of California, Santa Barbara, CA*

ß **17.3 Towards An Ultra-Low-Power Architecture Using Single-Electron Tunneling Transistors**
Changyun Zhu - *Queen's Univ., Kingston, ON, Canada*
Zhenyu Gu - *Northwestern Univ., Evanston, IL*
Li Shang - *Queen's Univ., Kingston, ON, Canada*
Robert P. Dick - *Northwestern Univ., Evanston, IL*
Robert Knobel - *Queen's Univ., Kingston, ON, Canada*

SESSION 18

RM: 6E

PHYSICAL IMPLEMENTATION OF FPGAS

Chair: Tim Tuan - *Xilinx, Inc., San Jose, CA*

Physical effects plague modern and future FPGA architectures. Glitches and soft errors are commonplace and will become more so in the future. The first three papers provide techniques to mitigate glitches and soft errors. The final paper describes a novel architecture feature to enhance arithmetic operations.

18.1 GlitchMap: An FPGA Technology Mapper for Low Power Considering Glitches
Lei Cheng, Deming Chen, Martin DF Wong - *Univ. of Illinois, Urbana, IL*

18.2 Using Negative Edge Triggered FFs to Reduce Glitching Power in FPGA Circuits
Tomasz S. Czajkowski, Stephen D. Brown - *Univ. of Toronto, Toronto, ON, Canada*

18.3s Single-Event-Upset (SEU) Awareness in FPGA Routing
Shahin Golshan, Elaheh Bozorgzadeh - *Univ. of California, Irvine, CA*

18.4s Enhancing FPGA Performance for Arithmetic Circuits
Philip Brisk, Ajay K. Verma, Hadi Parandeh-Afshar, Paolo Ienne - *EPFL, Lausanne, Switzerland*

SESSION 19

RM: 6F

PROCESS AWARE PHYSICAL DESIGN

Chair: Jason Hibbeler - *IBM Corp., Fishkill, NY*

Modern physical design must be aware of the nanometer technology effects such as lithography, variability and random defect yield. Two papers optimized cells and wiring for lithography constraints, one adjusts the wiring to maximize defect limited yield, and the remaining paper addresses buffer insertion considering process variation.

19.1 Fast Min-Cost Buffer Insertion under Process Variations
Ruiming Chen, Hai Zhou - *Northwestern Univ., Evanston, IL*

19.2 Exact Combinatorial Optimization Methods for Physical Design of Regular Logic Bricks
Brian L. Taylor, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

19.3s Concurrent Wire Spreading, Widening and Filling
Olivier Rizzo - *Infineon Technologies AG, Sophia-Antipolis, France*
Hanno Melzner - *Infineon Technologies AG, Munich, Germany*

19.4s Modeling Litho-Constrained Design Layout
Min-Chun Tsai, Daniel Zhang, Zongwu Tang - *Synopsys, Inc., Mountain View, CA*

SESSION 20

RM: 6A

RELIABLE DESIGN AND CAD SOLUTIONS FOR CIRCUIT AGING

Chair: Marek Patyra - *Intel Corp., Hillsboro, OR*

Negative-Bias-Temperature-Instability emerges as the prominent factor for circuit performance degradation. This session consists of three papers to address the design for circuit reliability. The first paper presents the application of IDDQ measurement to diagnose the reliability under NBTI. A comprehensive understanding of NBTI is provided in the second paper, for both combinational and sequential circuits. The third paper incorporates NBTI models into the synthesis of digit circuits. These approaches will ensure the lifetime of circuit operation under increasingly severe NBTI.

20.1 Characterization and Estimation of Circuit Reliability Degradation under NBTI using On-Line IDDQ Measurement
Kunhyuk Kang, Keejong Kim, Ahmad Ehteshamul Islam, Muhammad Ashraful Alam, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

20.2 The Impact of NBTI on the Performance of Combinational and Sequential Circuits
Wenping Wang - *Arizona State Univ., Tempe, AZ*
Shengqi Yang - *Peking Univ., Beijing, China*
Sarvesh Bhardwaj, Rakesh Vattikonda, Sarma Vrudhula - *Arizona State Univ., Tempe, AZ*
Frank Liu - *IBM Corp., Austin, TX*
Yu Cao - *Arizona State Univ., Tempe, AZ*

20.3 NBTI-Aware Synthesis of Digital Circuits
Sanjay V. Kumar, Chris H. Kim, Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

SESSION 21

RM: 6B

INVITED SESSION: SILICON, SAFETY AND SELF-DRIVING CARS

Chair: David W. Smith - *Synopsys, Inc., Hillsboro, OR*

This session spans the subject of automotive electronics from silicon design to the most advanced end-use applications, with a particular emphasis on safety. The first presentation is delivered by one of the world's leading automotive device suppliers. It highlights the differences in automotive silicon design practices versus other application segments, including commentary on the consequent EDA requirements. The second item is a technical paper that focuses on creating robust designs by modeling safe operating areas in two hardware description languages. The third presentation describes leading-edge research into autonomous vehicles: cars that can safely drive themselves in realistic urban environments.

21.1 There Is More Than Moore In Automotive ....
Hartmut Hiller - *Infineon Technologies AG , Munich, Germany*

21.2 Modeling Safe Operating Area in Hardware Description Languages
Leonid B. Goldgeisser, Ernst Christen, Zhichao Deng - *Synopsys, Inc., Hillsboro, OR*

21.3 Autonomous Automobiles: Developing Cars That Drive Themselves
Dave Ferguson - *Intel Corp./Carnegie Mellon Univ., Pittsburgh, PA*

SESSION 22

RM: 6C

SPECIAL SESSION: SILICON MEASUREMENT CORRELATION TO RELIABILITY, NOISE AND TIMING EFFECTS

Chair: Yu Cao - *Arizona State Univ., Tempe, AZ*

Industrial and academic speakers on the advanced line of EDA research will focus on a newly highlighted area of silicon sampling approaches as well as CAD algorithms and methodologies required to feed silicon measurements back into EDA tools and flows and to correlate the data to the underlying models and algorithms in order to reduce design pessimism by improving silicon prediction. The EDA community has historically created diverse models and algorithms for effects in timing, signal integrity, and reliability. Each of these models typically considers one or two effects which are solved in isolation. However, in silicon, the "real deal" happens where the impact of voltage droop, cross-coupling noise, MIS, degradation and other timing , noise and reliability effects occur at the same time and are highly correlated. The actual silicon effects need to be understood and correlated to the developing models and algorithms.

22.1 Design-Silicon Timing Correlation - A Data Mining Perspective
Li-C Wang, Pouria Bastani - *Univ. of California, Santa Barbara, CA*
Magdy S. Abadir - *Freescale Semiconductor, Inc., Austin, TX*

22.2 Silicon Speedpath Measurement and Feedback into EDA Flows
Kip Killpack, Chandramouli Kashyap, Eli Chiprout - *Intel Corp., Hillsboro, OR*

22.3s Characterizing Process Variation in Nanometer CMOS
Kanak Agarwal, Sani Nassif - *IBM Corp., Austin, TX*

22.4s On-Chip Measurements Complementary to Design Flows for Integrity in SoCs
Makoto Nagata - *Kobe Univ., Kobe, Japan*

SESSION 23

RM: 6E

OPTIMIZING ARITHMETIC AND COMMUNICATION

Chair: Ken Stevens - *Univ. of Utah, Salt Lake City, UT*

Papers in this session address two perennial problems in circuit synthesis: how to build fast arithemtic, and how to communicate quickly. The first paper presents a very nice way to optimize arithmetic-like gate-level circuits, a traditional failing of logic synthesis. The second addresses improving communication in a latency-insensitive communication setting. The third considers adding speculation to synchronous pipelines, and the fourth looks at optimizing FIR filter circuits.

ß 23.1 Progressive Decomposition: A Heuristic to Structure Arithmetic Circuits

Ajay K. Verma, **Philip Brisk**, Paolo Ienne - *EPFL, Lausanne, Switzerland*

23.2 Topology-Based Optimization of Maximal Sustainable Throughput in a Latency-Insensitive System

Rebecca Collins, Luca Carloni - *Columbia Univ., New York, NY*

23.3s Synchronous Elastic Circuits with Early Evaluation and Token Counterflow

Jordi Cortadella - *Universitat Politecnica Catalunya, Barcelona, Spain*
Michael Kishinevsky - *Intel Corp., Hillsboro, OR*

23.4s Optimization of Area in Digital FIR Filters using Gate-Level Metrics

Levent Aksoy - *Istanbul Technical Univ., Istanbul, Turkey*
Eduardo Costa - *Universidade Catolica de Pelotas, Pelotas-RS, Brazil*
Paulo Flores, Jose Monteiro - *INESC-ID/IST, Lisbon, Portugal*

SESSION 24

RM: 6F

ANALOG AND RF SIMULATION

Chair: Anirudh Devgan - *Magma Design Automation, Inc., Austin, TX*

This session contains four papers that present novel algorithms for analog/mixed-signal and RF circuits. The first paper presents an algorithm for designing oscillators to conform to a specified oscillation frequency. The second paper presents an approach to calculating the cyclostationary effects of simultaneous switching noise (SSN) on PLLs. The third paper presents advances in efficient disstortion and intermodulation analysis of large circuits via hierarchical and parallelizable preconditioning techniques. The fourth paper presents a method for adapting time-varying noise analysis for computing parameter variability effects in mixed-signal circuits.

ß 24.1 Parameter Finding Methods for Oscillators with a Specified Oscillation Frequency

Igor Vytyaz - *Oregon State Univ., Corvallis, OR*
David C. Lee, Suihua Lu, Amit Mehrotra - *Berkeley Design Automation, Inc., Santa Clara, CA*
Un-Ku Moon, Kartikeya Mayaram - *Oregon State Univ., Corvallis, OR*

24.2 Modeling Simultaneous Switching Noise-Induced Jitter for System-on-Chip Phase-Locked Loops

Henry H. Chan, Zeljko Zilic - *McGill Univ., Montreal, QC*

24.3s Accelerating Harmonic Balance Simulation Using Efficient Parallelizable Hierarchical Preconditioning

Wei Dong, Peng Li - *Texas A&M Univ., College Station, TX*

24.4s Fast, Non-Monte-Carlo Estimation of Transient Performance Variation Due to Device Mismatch

Jaeha Kim, Kevin D. Jones - *Rambus Inc., Los Altos, CA*
Mark A. Horowitz - *Stanford Univ., Stanford, CA*

SESSION 25

RM: 6A

PANEL: TLM: CROSSING OVER FROM BUZZ TO ADOPTION

Chair: Daniel D. Gajski - *Univ. of California, Irvine, CA*
Organizer: Francine Bacchini

Transaction level modeling (TLM) has been used in both system and SoC design for some years, and TLM standards activity is driving increased usage. Some believe TLM is the next level of design and verification abstraction in EDA, but large gaps in standardization and tool support pose a challenge. Panelists will share their adoption experiences, discuss where and how TLM is being applied, debate what is needed for successful TLM use today and beyond.

Panelists:
Laurent Maillet-Contoz - *STMicroelectronics, Crolles, France*
Jack Dovovan - *ESLX Inc., Austin, TX*
Jack Greenbaum - *Green Hills Software, Inc., Santa Barbara, CA*
Haruhisa Kashiwagi - *STARC, Yokohama, Japan*
Tommi Makelainen - *Nokia, Tampere, Finland*
Rishiyur S. Nikhil - *Bluespec, Inc., Waltham, MA*

SESSION 26

RM: 6B

PANEL: ELECTRONICS: THE NEW DIFFERENTIAL IN THE AUTOMOTIVE INDUSTRY

Chair: Walden C. Rhines - *Mentor Graphics Corp., Wilsonville, OR*
Organizer: Nick Smith

Modern electronics is delivering huge improvements in automobile safety, efficiency and driver experience. So is the ability to conceive, design and implement electronic systems now the key competitive differentiator within the automotive industry, rather than traditional factors such as styling or manufacturing excellence? The Panel, which is designed to appeal to experts and non-experts alike, dissects this issue and discusses the dramatic impact of future automotive electronic technologies. The resultant challenges and opportunities presented within EDA are also highlighted.

Panelists:
Andrew Chien - *Ricardo Strategic Consulting , Detroit, MI*
Alberto Sangiovanni-Vincentelli - *Univ. of California , Berkeley, CA*
Christopher Hegarty - *Infineon Technologies AG, Munich , Germany*
Frank Winters - *Delphi Electronics and Safety, Kokomo, IN*

SESSION 27

RM: 6C

MODERN PLACEMENT TECHNIQUES

Chair: Hai Zhou - *Northwestern Univ., Evanston, IL*

Modern placement must handle various emerging challenges, such as mixed-size designs, density considerations, multi-supply voltages, and symmetry constraints. This session presents a set of new techniques for solving these issues. The first paper addresses the macro placement for mixed-size designs. The second paper proposes a novel idea for quadratic global placement. An incremental placement approach for multi-supply voltage design is presented in the third paper. The last paper introduces a tree-based formulation for handling symmetry constraints in analog placement.

27.1 MP-trees: A Packing-Based Macro Placement Algorithm for Mixed-Size Designs
Tung-Chieh Chen, Ping-Hung Yuh, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
Fwu-Juh Huang, Denny Liu - *MediaTek Inc., Hsin-Chu, Taiwan*

ß **27.2 RQL: Global Placement via Relaxed Quadratic Spreading and Linearization**
Natarajan Viswanathan - *Iowa State Univ., Ames, IA*
Gi-Joon Nam, Charles Alpert, Paul Villarrubia, Haoxing Ren - *IBM Corp., Austin, TX*
Chris Chu - *Iowa State Univ., Ames, IA*

27.3 Improving Voltage Assignment by Outlier Detection and Incremental Placement
Huaizhi Wu - *Atoptech, Inc., Santa Clara, CA*
Martin D. F. Wong - *Univ. of Illinois, Urbana, IL*

27.4 Analog Placement Based on Novel Symmetry-Island Formulation
Po-Hung Lin - *National Taiwan Univ., Taipei, Taiwan*
Shyh-Chang Lin - *Springsoft, Inc., Hsinchu, Taiwan*

SESSION 28

RM: 6E

ADVANCES IN EMBEDDED HARDWARE DESIGN

Chair: Tony Givargis - *Univ. of California, Irvine, CA*

This session presents various topics in the area of embedded hardware design. The first paper describes a WCET cache analysis approach. Next a novel multi-resolution bus tracer is described, followed by two papers dealing with security extensions to embedded processors. Finally an efficient pattern matching approach in hardware is presented.

28.1 Modeling the Function Cache for Worst-Case Execution Time Analysis
Raimund Kirner, Martin Schoeberl - *Vienna Univ. of Tech., Vienna, Austria*

28.2 An Embedded Multi-resolution AMBA Trace Analyzer for Microprocessor-based SoC Integration
Chung-Fu Kao, Ing-Jer Huang, Chi-Hung Lin - *National Sun Yat-Sen Univ., Kaohsiung, Taiwan*

28.3 Hardware Support for Secure Processing in Embedded Systems
Shufu Mao, Tilman Wolf - *Univ. of Massachusetts, Amherst, MA*

28.4s RIJID: Random Code Injection to Mask Power Analysis Based Side Channel Attacks
Jude A. Ambrose, Roshan G. Ragel, Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*

28.5s Compact State Machines for High Performance Pattern Matching
Piti Piyachon, Yan Luo - *Univ. of Massachusetts, Lowell, MA*

SESSION 29

RM: 6F

BRIDGING THE GAP WITH SILICON

Chair: Masanori Hashimoto - *Osaka Univ., Suita, Japan*

Modeling and simulation tools in DFM and timing analysis have evolved considerably over the last several years, but relatively little has been done in closing the loop with actual Si measurements. This session aims to show how post-Si and environmental information can be leveraged to increase our pre-Si prediction accuracy and fine tune the design.

29.1 Confidence Scalable Post-Silicon Statistical Delay Prediction under Process Variations
Qunzeng Liu, Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

29.2 Statistical Framework for Technology-Model-Product Co-Design and Convergence
Choongyeun Cho, Daeik Kim, Jonghae Kim - *IBM Corp., Hopewell Junction, NY*
Jean-Olivier Plouchart, Robert Trzcinski - *IBM Corp., Yorktown Heights, NY*

29.3 Extraction of Statistical Timing Profiles Using Test Data
Ying-Yen Chen, Jing-Jia Liou - *National Tsing-Hua Univ., Hsin-Chu, Taiwan*

29.4 An Analysis of Timing Violations Due to Spatially Distributed Thermal Effects in Global Wires
Krishnan Sundaresan - *Sun Microsystems, Inc., Sunnyvale, CA*
Nihar R. Mahapatra - *Michigan State Univ., East Lansing, MI*

SESSION 30

RM: 6A

PRACTICAL SOLUTIONS FOR POWER-AWARE TESTING

Chair: Sandip Kundu - *Univ. of Massachusetts, Amherst, MA*

This session proposes various complementary solutions for addressing the problem of excessive power consumption during test. The first paper presents an automated solution for the generation of power-aware scan test planning. The next two papers address the problem of power-constrained test pattern generation for at-speed testing. The last one presents a low-power test data compression scheme.

30.1 Scan Test Planning for Power Reduction
Michael E. Imhof, Christian G. Zoellin, Hans-Joachim Wunderlich - *Universitaet Stuttgart, Stuttgart, Germany*
Nicolas Maeding, Jens Leenstra - *IBM Corp., Boeblingen, Germany*

30.2 Critical-Path-Aware X-Filling for Effective IR-Drop Reduction in At-Speed Scan Testing
Xiaoqing Wen - *Kyushu Institute of Tech., Iizuka, Japan*
Kohei Miyase, Tatsuya Suzuki, Seiji Kajihara - *Kyushu Institute of Tech., Iizuka, Japan*
Yuji Ohsumi - *Dai Nippon Printing, Co., Ltd., Tokyo, Japan*
Kewal K. Saluja - *Univ. of Wisconsin, Madison, WI*

30.3 Transition Delay Fault Test Pattern Generation Considering Supply Voltage Noise in a SOC Design
Nisar Ahmed, **Mohammad Tehranipoor** - *Univ. of Connecticut, Storrs, CT*
Vinay Jayaram - *Texas Instruments, Inc., Dallas, TX*

30.4 New Test Data Decompressor for Low Power Applications
Dariusz Czysz - *Poznan Univ. of Technology, Poznan, Poland*
Grzegorz Mrugalski, **Janusz Rajski** - *Mentor Graphics Corp., Wilsonville, OR*
Jerzy Tyszer - *Poznan Univ. of Technology, Poznan, Poland*

SESSION 31

RM: 6B

SPECIAL SESSION: VIRTUAL AUTOMOTIVE PLATFORMS

Chair: Luciano Lavagno - *Politecnico Di Torino, Torino, Italy*

This session will feature both experts in the domain of virtualization mechanisms used to reduce the number of hardware processors in automotive electronics and potential users of the technology. Traditionally, adding new information processing functionality in cars required the addition of new computing hardware, leading to unacceptable growth in the number of microcontrollers. Virtualization of resources will be used to implement different applications on shared physical hardware. Applications will run on virtual platforms, being appropriately shielded from other applications through adequate protection mechanisms. Virtual platforms are a very hot topic in the automotive industry these days, as witnessed by the high activity around the AUTOSAR standardization effort. Designing for a virtual automotive platform involves the interplay of several factors and impacts all aspects of safety-critical distributed embedded system design including HW, SW, applications, Real-Time scheduling, and communication protocols.

31.1 Are Virtual Platforms Going to Rescue the Autonomous Driving Dream?
Massimo Osella - *General Motors Corp., Warren, MI*

31.2 Automotive Software Integration
Razvan Racu, Arne Hamann - *Tech. Univ. of Braunschweig, Braunschweig, Germany*
Kai Richter - *Symtavision GmbH, Braunschweig, Germany*
Rolf Ernst - *Tech. Univ. of Braunschweig, Braunschweig, Germany*

31.3 Virtual Platforms and Timing Analysis: Status, Challenges, and Future Directions
Marco Di Natale - *Scuola Superiore S. Anna, Pisa, Italy*

31.4 Computer-Aided Architecture Design and Optimized Implementation of Distributed Automotive EE Systems
Antal Rajnak, Ajay Kumar - *Mentor Graphics Corp., Wilsonville, OR*

SESSION 32

RM: 6C

SPECIAL SESSION: THE FUTURE OF INTERCONNECTS: HOW WILL BILLIONS OF TRANSISTORS COMMUNICATE IN THE NANOMETER ERA

Chair: Nagaraj NS - *Texas Instruments Inc., Dallas, TX*

In nanometer era, interconnects have become the primary limiter of performance, energy dissipation, and signal integrity in complex IC designs. In the next decade, CMOS technology will enable billions of transistors on a chip, which will impose unprecedented challenges on the interconnects in terms of bandwidth and power requirements. To address these challenges, a broad spectrum of novel solutions to the multifaceted interconnect problem must be explored. A failure to meet these challenges threatens to derail the progress of chip and system designs of the future. This special session will include presentations from world renowned experts in industry and academia to address these challenges by focusing on all three aspects of this crucial problem: technology; design; and CAD. Presentations will address issues ranging from: Interconnects in third dimensions - design and process challenges for 3D ICs; performance modeling and optimization challenges of carbon nanotube interconnects; characteristics, possibilities, and limitations of micro-photonic interconnects; and modeling simulation and CAD needs of future interconnects.

32.1 Interconnects in the 3rd Dimension: Design and Process Challenges for 3D ICs
Kerry Bernstein, Paul Andry, Jerome Cann, Phil Emma, David Greenberg, Wilfried Haeson, Michael Ignatowski, Steve Koester, John Macerlein, Ruchir Puri, Albert Young - *IBM Corp., Yorktown Heights, NY*

32.2 Performance Modeling and Optimization for Single- and Multi-Wall Carbon Nanotube Interconnects
Azad Naeemi, Reza Sarvari, James D. Meindl - *Georgia Institute of Tech., Atlanta, GA*

32.3 Micro-Photonic Interconnects: Characteristics, Possibilities and Limitations
Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*

32.4 CAD Implications of New Interconnect Technologies
Louis Scheffer - *Cadence Design Systems, Inc., San Jose, CA*

SESSION 33

RM: 6E

ADVANCES IN DECISION PROCEDURES

Chair: Alok Jain - *Cadence Design Systems, Inc., Noida, India*

This session focuses on advances in decision procedures. The first paper presents a technique to simplify the CNF to improve efficiency of SAT solvers. The second paper provides a decision procedure that efficiently takes into consideration formulae with a combination of Boolean and arithmetic terms. The final two papers describe techniques for efficiently generating resolution proofs from SAT solvers.

33.1 Alembic: An Efficient Algorithm for CNF Simplification
Hyojung Han, Fabio Somenzi - *Univ. of Colorado, Boulder, CO*

33.2 EHSAT: An Efficient RTL Satisfiability Solver Using an Extended DPLL Procedure
Shujun Deng, Jinian Bian, Weimin Wu, Xiaoqing Yang, Yanni Zhao - *Tsinghua Univ., Beijing, China*

ß **33.3 On-The-Fly Resolve Trace Minimization**
Ohad Shacham, Karen Yorav - *IBM Corp., Haifa, Israel*

33.4 On Resolution Proofs for Combinational Equivalence
Satrajit Chatterjee, Alan Mishchenko, Robert Brayton - *Univ. of California, Berkeley, CA*
Andreas Kuehlmann - *Cadence Design Systems, Inc., Berkeley, CA*

SESSION 34

RM: 6F

3D IC AND PACKAGE DESIGN ISSUES

Chair: John Berrie - *Zuken UK Ltd., Bristol, United Kingdom*

This session covers design beyond the boundaries of the chip die, including the hot topics of 3D IC design and system-in-package. Innovative approaches are presented in important areas where technology is developing rapidly.

ß **34.1 An Integer Linear Programming Based Routing Algorithm for Flip-Chip Design**
Jia-Wei Fang, Chin-Hsiung Hsu, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

34.2 Computationally Efficient Power Integrity Simulation for System-on-Package Applications
Krishna Bharath, Ege Engin, **Madhavan Swaminathan** - *Georgia Institute of Tech., Atlanta, GA*
Kazuhide Uriu, Toru Yamada - *Matsushita Electric Industrial Co., Ltd., Japan, Japan*

34.3s Off-chip Decoupling Capacitor Allocation for Chip Package Co-Design
Hao Yu - *Berkeley Design Automation, Santa Clara, CA*
Chunta Chu, Lei He - *Univ. of California, Los Angeles, CA*

34.4s Scalability of 3D-Integrated Arithmetic Units in High-Performance Microprocessors
Kiran Puttaswamy, Gabriel H. Loh - *Georgia Institute of Tech., Atlanta, GA*

34.5 Placement of 3D ICs with Thermal and Interlayer Via Considerations
Brent A. Goplen, Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

SESSION 35

RM: 6A

PANEL: COREZILLA: BUILD AND TAME THE MULTICORE BEAST

Chair: Markus Levy - *Multicore Association, El Dorado Hills, CA*

Organizer: Lauren Sarno

Multi-core SoCs are being built combining several microprocessors and/or DSPs on a chip, but are these SoCs being held back by the lack of adequate system-design and software development tools? Multi-core hardware design is leading the industry in supplying the advantages of flexible software-defined architectures, but support for systems optimization, integration and verification of multi-core systems is seriously lacking. This panel will discuss the roadmap for multi-core designs and the tools available to support them.

Panelists:
Gordon Cameron - *Mentor Graphics Corp., Newbury, United Kingdom*
Wen-mei W. Hwu - *Univ. of Illinois , Urbana, IL*
James R. Larus - *Microsoft Corp., Redmond, WA*
Christopher K. Lennard - *ARM Ltd , Cambridge, United Kingdom*
Craig Lund - *Mercury Computer Systems, Inc., Chelmsford, MA*
James Reinders - *Intel Corp., Hillsboro, OR*
Takashi Yoshimori - *Toshiba Corp., Kawasaki, Japan*

All speakers are denoted in bold
S - denotes short paper
ß - denotes best paper candidate

SESSION 36

RM: 6B

SPECIAL SESSION: SYNTHETIC BIOLOGY: AN EMERGING DISCIPLINE WITH NEW ENGINEERING RULES AND DESIGN TOOLS

Chair: Ion Mandoui - *Univ. of Connecticut, Storrs, CT*

With recent advances in our understanding of cellular processes and improvements in DNA synthesis methods, we can now regard cells as "programmable matter." Through genetic engineering, we are equipping cells with new sophisticated capabilities for gene regulation, information processing, and communication. These new capabilities serve as catalysts for Synthetic Biology, an emerging engineering discipline to program cell behaviors as easily as we program computers. Synthetic biology will improve our quantitative understanding of natural biological processes and will also have biotechnology applications in areas such as biosensing, synthesis of pharmaceutical products, molecular fabrication of biomaterials and nanostructures, and tissue engineering. In this session, we propose to discuss the current state-of-the-art in synthetic biology and address the challenges as we move forward towards foundational technology for highly complex systems and applications.

36.1 Synthetic Biology: From Bacteria to Stem Cells
Ron Weiss - *Princeton Univ., Princeton, NJ*

36.2 Engineering Synthetic Gene Circuits in Bacteria
Lingchong You - *Duke Univ., Durham, NC*

36.3 Programming Living Cells to Function as Massively Parallel Computers
Jeff Tabor - *Univ. of California, San Francisco, CA*

36.4 Synthesizing Stochasticity in Biochemical Systems
Brian Fett - *Univ. of Minnesota, Minneapolis, MN*
Jehoshua Bruck - *California Institute of Tech., Pasadena, CA*
Marc D. Riedel - *Univ. of Minnesota, Minneapolis, MN*

SESSION 37

RM: 6C

PROGRAMMING AND SCHEDULING EMBEDDED SYSTEMS

Chair: Paolo Ienne - *EFPL, Lausanne, Switzerland*

Programming models and code compression for embedded system have a significant impact on design. Even more, scheduling real-time applications impacts design in important ways. This session will explore new advances in programming, compression and scheduling for embedded systems.

37.1 Instruction Splitting for Efficient Code Compression
Talal Bonny, Joerg Henkel - *Univ. of Karlsruhe, Karlsruhe, Germany*

37.2 An Embedded Coherent-Multithreading Multimedia Processor and Its Programming Model
Jui-Chin Chu, Wei-Chun Ku, **Shu-Hsuan Chou**, Tien-Fu Chen, Jiun-In Guo - *National Chung Cheng Univ., Chia-Yi, Taiwan*

37.3 Efficient Computation of Buffer Capacities for Cyclo-Static Dataflow Graphs
Maarten H. Wiggers - *Univ. of Twente, Enschede, Netherlands*
Marco J.G. Bekooij - *NXP Semiconductors, Eindhoven, Netherlands*
Gerard J.M. Smit - *Univ. of Twente, Enschede, Netherlands*

37.4 Energy-Aware Scheduling for Real-Time Multiprocessor Systems with Uncertain Task Execution Time
Changjiu Xian, Yung-Hsiang Lu, Zhiyuan Li - *Purdue Univ., West Lafayette, IN*

SESSION 38

RM: 6D

EMERGING TEST SOLUTIONS

Chair: Alex Orailoglu - *Univ. of California, San Diego, CA*

This session provides wide aspects of test technologies for emerging test problems. The first two papers address SoC test problems, the third paper proposes a new RTL DFT methodology, and the fourth paper treats an at-speed overtesting problem.

38.1 A Robust Protocol for Concurrent On-Line Test (COLT) of NoC-based Systems-on-a-Chip
Praveen S. Bhojwani, Rabi N. Mahapatra - *Texas A&M Univ., College Station, TX*

38.2 SOC Test Architecture Optimization for Signal Integrity Faults on Core-External Interconnects
Qiang Xu, Yubin Zhang - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*
Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

38.3 A DFT Method for Time Expansion Model at Register Transfer Level
Hiroyuki Iwata, Tomokazu Yoneda, Hideo Fujiwara - *Nara Institute of Science & Tech., Nara, Japan*

38.4 Test Generation in the Presence of Timing Exceptions and Constraints
Dhiraj Goswami, **Kun-Han Tsai**, Mark Kassab, Janusz Rajski - *Mentor Graphics Corp., Wilsonville, OR*

SESSION 39

RM: 6E

CIRCUIT LEVEL POWER ANALYSIS AND LOW POWER DESIGN

Chair: Chris Kim - *Univ. of Minnesota, Minneapolis, MN*

This session covers various aspects related to circuit level power analysis and low power design. The first three papers address the problem of subthreshold design and analysis, as well as modeling techniques for dynamic voltage drop. The last two papers address the problem of leakage effect in sub-65nm circuits and energy aware data compression.

39.1 Analysis and Optimization of Sleep modes in Subthreshold Circuit Design

Mingoo Seok, Scott Hanson, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

39.2 Nanometer Device Scaling in Subthreshold Circuits

Scott Hanson, Mingoo Seok, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

39.3 Efficient Modeling Techniques for Dynamic Voltage Drop Analysis

Hedi Harizi - *Qimonda AG, Neubiberg, Germany*
Robert Haeussler - *Infineon Technologies AG, Neubiberg, Germany*
Markus Olbrich, Erich Barke - *Univ. of Hannover, Hannover, Germany*

39.4s On Estimating Impact of Loading Effect on Leakage Current in sub-65nm Scaled CMOS Circuits based on Newton-Raphson Method

Ashesh Rastogi, Wei Chen, **Sandip Kundu** - *Univ. of Massachusetts, Amherst, MA*

39.5s Energy-Aware Data Compression for Multi-Level Cell (MLC) Flash Memory

Yongsoo Joo, Youngjin Cho, Donghwa Shin, Naehyuck Chang - *Seoul National Univ., Seoul, South Korea*

SESSION 40

RM: 6F

PARAMETER TUNING IN SYSTEM ARCHITECTURE EXPLORATION

Chair: Erwin de Kock - *NXP Semiconductors, Eindhoven, Netherlands*

This session presents modeling techniques for estimation and optimization of system architecture. The first three papers employ statistical techniques for speeding up cycle simulation, estimating system performance, and tuning caches for low power. The fourth paper optimizes memory size for multi-media applications.

40.1 Shared Resource Access Attributes for High-Level Contention Models

Alex Bobrek - *Carnegie Mellon Univ., Pittsburgh, PA*
JoAnn M. Paul - *Virginia Tech., Arlington, VA*
Donald E. Thomas - *Carnegie Mellon Univ., Pittsburgh, PA*

40.2 A Probabilistic Approach to Model Resource Contention for Performance Estimation of Multi-featured Media Devices

Akash Kumar, Bart Mesman, Henk Corporaal, Bart Theelen - *Eindhoven Univ. of Tech., Eindhoven, Netherlands*
Yajun Ha - *National Univ. of Singapore, Singapore*

40.3 Automatic Cache Tuning for Energy-Efficiency using Local Regression Modeling

Peter Hallschmid, Resve Saleh - *Univ. of British Columbia, Vancouver, BC, Canada*

40.4 Reducing Data-Memory Footprint of Multimedia Applications by Delay Redistribution

Balaji Raman, Samarjit Chakraborty, Wei Tsang Ooi - *National Univ. of Singapore, Singapore*
Santanu Dutta - *NVIDIA Corp., Santa Clara, CA*

SESSION 41

RM: 6A

PANEL: VERIFICATION COVERAGE: WHEN IS ENOUGH ENOUGH?

Chair: Alan Hu - *Univ. of British Columbia, Vancouver, BC, Canada*

Organizer: Francine Bacchini

For EDA users, verification is a challenging and time-consuming process. Recent tools have driven powerful new methodologies, and have renewed debate on the issue of coverage interoperability among heterogeneous verification tools and their respective handling of coverage data. New methodologies hold promise for better decision-making, as does a baseline standard for coverage interoperability. Learn from industry-leading EDA users and vendors as they explore these emerging solutions to the ever-growing challenge of functional verification.

Panelists:

Tom Fitzpatrick - *Mentor Graphics Corp., San Jose, CA*
David J. Lacey - *Hewlett-Packard Co., Richardson, TX*
Andrew Piziali - *Consultant for Cadence Design Systems, Inc., Parker, TX*
Rajeev Ranjan - *Jasper Design Automation, Inc., Mountain View, CA*
Mercedes Tan - *Sun Microsystems, Inc., Sunnyvale, CA*
Avi Ziv - *IBM Corp., Haifa, Israel*

Thursday, June 7 • 2:00pm – 4:00pm

All speakers are denoted in bold
S - denotes short paper
ß - denotes best paper candidate

SESSION 42

RM: 6B

SPECIAL SESSION: THOUSAND-CORE CHIPS

Chair: David Yeh - *Texas Instruments Inc., Dallas, TX*

While there is wide consensus that future chips will be multi-core, will industry ever scale to thousand-core chips? This special session examines this important question from four perspectives: technology, architecture, programming, and design automation. There is no debate that we have sufficient raw transistors. But, what will the power characteristics be? How will the cores be interconnected on and off-chip? How do we size the core cache? How will we program such chips while dealing with legacy software? How can EDA mitigate design, testing and verification complexity?

42.1 Thousand-Core Chips - A Technology Perspective
Shekhar Y. Borkar - *Intel Corp., Hillsboro, OR*

42.2 The Kill Rule for Multicore
Anant Agarwal - *Massachusetts Institute of Tech., Cambridge, MA*

42.3 Sequential Programming Models for Programming Thousand-Core Systems
Wen-Mei Hwu, Shane Ryoo, Sain-Zee Ueng, John H. Kelm - *Univ. of Illinois, Urbana, IL*
Issac Gelado - *Universitat Politecnica de Catalunya, Barcelona, Spain*
Samuel S. Stone, Robert E. Kidd, Sara Sadeghi Baghsorkhi, Aqeel A. Mahesri, Stephanie Tsao - *Univ. of Illinois, Urbana, IL*
Nacho Navarro - *Universitat Politecnica de Catalunya, Barcelona, Spain*
Steve S. Lumetta, Matthew I. Frank, Sanjay J. Patel - *Univ. of Illinois, Urbana, IL*

42.4 Multi-Core Design Automation Challenges
John Darringer - *IBM Corp., Yorktown Heights, NY*

SESSION 43

RM: 6C

COMMUNICATION-BASED RESOURCE ALLOCATION

Chair: Luca Carloni - *Columbia Univ., New York, NY*

This session's papers consider communication issues to generate better designs. This principle is applied across a broad range of abstraction levels: microarchitectural, reconfigurable and multiprocessor – to produce improved results. The final two short papers describe novel tools that help guide designers towards better designs.

43.1 Interconnect and Communication Synthesis for Distributed Register-File Microarchitecture
Kyoung-Hwan Lim, YongHwan Kim, Taewhan Kim - *Seoul National Univ., Seoul, South Korea*

43.2 Selective Bandwidth and Resource Management in Scheduling for Dynamically Reconfigurable Architectures
Sudarshan Banerjee, Elaheh Bozorgzadeh - *Univ. of California, Irvine, CA*
Juanjo Noguera - *Technical Univ. of Catalonia, Barcelona, Spain*
Nikil Dutt - *Univ. of California, Irvine, CA*

43.3 Multiprocessor Resource Allocation for Throughput-Constrained Synchronous Dataflow Graphs
Sander Stuijk, Twan Basten, Marc Geilen, Henk Corporaal - *Eindhoven Univ. of Tech., Eindhoven, Netherlands*

43.4s Global Critical Path: A Tool for System-Level Timing Analysis
Girish Venkataramani - *Carnegie Mellon Univ., Pittsburgh, PA*
Mihai Budiu - *Microsoft Corp., Mountain View, CA*
Tiberiu Chelcea, Seth C. Goldstein - *Carnegie Mellon Univ., Pittsburgh, PA*

43.5s Designer-Controlled Generation of Parallel and Flexible Heterogeneous MPSoC Specification
Pramod Chandraiah, Rainer Doemer - *Univ. of California, Irvine, CA*

SESSION 44

RM: 6D

EMBEDDED PROCESSOR AND MPSoC DESIGN

Chair: Nikil Dutt - *Univ. of California, Irvine, CA*

The session presents exciting new system-level design challenges targeting diverse platforms ranging from low-end energy and area-constrained processors to very high-end performance-driven many-core network and multimedia processors. Papers address topics ranging from novel instruction encodings for extensible/configurable processors, application mapping approaches on state-of-the-art network processors, and architecture design of pipelined multimedia MPSoCs.

44.1 RISPP: Rotating Instruction Set Processing Platform
Lars Bauer, Muhammad Shafique, Simon Kramer, Joerg Henkel - *Univ. of Karlsruhe, Karlsruhe, Germany*

44.2s ASIP Instruction Encoding for Energy and Area Reduction
Paul Morgan, Richard Taylor - *CriticalBlue, Edinburgh, United Kingdom*

44.3s Approximation Algorithm for Data Mapping on Block Multi-threaded Network Processor Architectures
Chris Ostler, Karam S. Chatha - *Arizona State Univ., Tempe, AZ*

44.4 Program Mapping onto Network Processors by Recursive Bipartitioning and Refining
Jia Yu - *Univ. of Pittsburgh, Pittsburgh, PA*
Jingnan Yao, Laxmi Bhuyan - *Univ. of California, Riverside, CA*
Jun Yang - *Univ. of Pittsburgh, Pittsburgh, PA*

44.5 Design Methodology for Pipelined Heterogeneous Multiprocessor System
Seng Lin Shee, Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*

SESSION 45

RM: 6E

MODELING TECHNOLOGY IMPACT

Chair: Davide Pandini - *STMicroelectronics, Agrate Brianza, Italy*

With technology scaling, the interaction between design practice (circuit and layout) and performance and algorithms is becoming more complex. This session includes a number of papers that examine this interaction at the device, layout, and interconnect levels.

45.1 A General Framework for Spatial Correlation Modeling in VLSI Design

Frank Liu - *IBM Corp., Austin, TX*

45.2 Modeling and Analysis of Non-Rectangular Gate for Post-Lithography Circuit Simulation

Ritu Singhal, Asha Balijepalli, Anupama Subramaniam - *Arizona State Univ., Tempe, AZ*
Frank Liu, Sani Nassif - *IBM Corp., Austin, TX*
Yu Cao - *Arizona State Univ., Tempe, AZ*

45.3 A Framework for Accounting for Process Model Uncertainty in Statistical Static Timing Analysis

Guo Yu, **Wei Dong**, Zhuo Feng, Peng Li - *Texas A&M Univ., College Station, TX*

45.4 Fast Capacitance Extraction in Multilayer, Conformal and Embedded Dielectric using Hybrid Boundary Element Method

Ying Zhou - *Texas A&M Univ., College Station, TX*
Zhuo Li - *Pextra Corp., College Station, TX*
Weiping Shi - *Texas A&M Univ., College Station, TX*

SESSION 46

RM: 6F

TECHNOLOGY MAPPING AND PHYSICAL SYNTHESIS

Chair: Mahesh Iyer - *Synopsys, Inc., Mountain View, CA*

This section focuses on technology mapping and physical synthesis. The first three papers address various aspects of technology mapping and the last paper merges physical design and logic synthesis.

46.1 A Unified Approach to Canonical Form-based Boolean Matching

Giovanni Agosta, **Francesco Bruschi**, Gerardo Pelosi, Donatella Sciuto - *Politecnico di Milano, Milano, Italy*

46.2 Gate Sizing For Cell Library-Based Designs

Shiyan Hu - *Texas A&M Univ., College Station, TX*
Mahesh Ketkar - *Intel Corp., Oregon, OR*
Jiang Hu - *Texas A&M Univ., College Station, TX*

46.3 Statistical Leakage Power Minimization Using Fast Equi-Slack Shell Based Optimization

Xiaoji Ye - *Texas A&M Univ., College Station, TX*
Yaping Zhan - *Advanced Micro Devices, Inc., Austin, TX*
Peng Li - *Texas A&M Univ., College Station, TX*

46.4 Techniques for Effective Distributed Physical Synthesis

Wenting Hou - *Synopsys, Inc., Beijing, China*
Freddy Y.C. Mang - *Synopsys, Inc., Mississauga, ON, Canada*
Pei-Hsin Ho - *Synopsys, Inc., Portland, OR*

SESSION 47

RM: 6A

SYSTEM-LEVEL POWER MANAGEMENT AND ANALYSIS

Chair: Vivek Tiwari - *Intel Corp., Santa Clara, CA*

This session covers various aspects related to system-level power management including disk architectures, hybrid power sources, and the effects of leakage variability. The last two papers in the session address the issue of speeding up power analysis and optimizing power for multiple voltage systems.

47.1 SODA: Sensitivity Based Optimization of Disk Architecture

Yan Zhang, Sudhanva Gurumurthi, **Mircea R. Stan** - *Univ. of Virginia, Charlottesville, VA*

47.2 Dynamic Power Management with Hybrid Power Sources

Jianli Zhuo, Chaitali Chakrabarti - *Arizona State Univ., Tempe, AZ*
Kyungsoo Lee, Naehyuck Chang - *Seoul National Univ., Seoul, South Korea*

47.3 System-on-Chip Power Management Considering Leakage Power Variations

Saumya Chandra - *Univ. of California, San Diego, CA*
Kanishka Lahiri, Anand Raghunathan - *NEC Labs America, Princeton, NJ*
Sujit Dey - *Univ. of California, La Jolla, CA*

47.4s Accelerating System-on-Chip Power Analysis Using Hybrid Power Estimation

Mohammad A. Ghodrat - *Univ. of California, Irvine, CA*
Kanishka Lahiri, Anand Raghunathan - *NEC Labs America, Princeton, NJ*

47.5s A Provably Good Approximation Algorithm for Power Optimization Using Multiple Supply Voltages

Hung-Yi Liu, Wan-Ping Lee, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

Thursday, June 7 • 4:30pm – 6:00pm

All speakers are denoted in bold
S - denotes short paper
ß - denotes best paper candidate

SESSION 48

RM: 6B

DYNAMIC VERIFICATION OF PROCESSORS AND PROCESSOR-BASED DESIGNS

Chair: Grant Martin - *Tensilica Inc., Santa Clara, CA*

This sesssion presents various tools and methods for verifying complex processor and processor-based designs. These methods include intelligent generation of test-cases for system-level verification of parallel computer systems, verification of the external interrupt behaviors of microprocessors, and coverage model generation based on a formal model of potential specification misinterpretations. The session ends with a case study presenting a block and chip level verification methodology constructed from reusable elements.

48.1 Intelligent Interleaving of Scenarios: A Novel Approach to System Level Test Generation

Shady Copty, **Itai Jaeger**, Yoav Katz, Michael Vinov - *IBM Corp., Haifa, Israel*

48.2 Automatic Verification of External Interrupt Behaviors for Microprocessor Design

Fu-Ching Yang, Wen-Kai Huang, Ing-Jer Huang - *National Sun Yat-Sen Univ., kaohsiung, Taiwan*

48.3s A Framework for the Validation of Processor Architecture Compliance

Allon Adir, Sigal Asaf, Laurent Fournier, **Itai Jaeger**, Ofer Peled - *IBM Corp., Haifa, Israel*

48.4s Functional Verification of SiCortex Multiprocessor System-on-a-Chip

Oleg Petlin, **Wilson Snyder** - *SiCortex, Inc., Maynard, MA*

SESSION 49

RM: 6C

FPGA TOOLS AND METHODOLOGIES

Chair: Xiaojian Yang - *Synplicity, Inc., Sunnyvale, CA*

This session focuses on new improvements in FPGA synthesis at system and logic level. The first paper introduces a new BDD synthesis approach using linear BDD expansion considering delay as a parameter when searching for cuts. The second paper proposes a general tool flow targeting high throughput video processing applications. The third paper considers rewiring to reduce area and delay.

49.1 DDBDD: Delay-Driven BDD Synthesis for FPGAs

Lei Cheng, Deming Chen, Martin DF Wong - *Univ. of Illinois, Urbana, IL*

49.2 An High-End Realtime Stream Processing Library for FPGAs

Amilcar Lucas, Sven Heithecker, Rolf Ernst - *Technical Univ. of Braunschweig, Braunschweig, Germany*

49.3 How Much Can Logic Perturbation Help from Netlist to Final Routing for FPGAs

Catherine L. Zhou, Wai-Chung Tang, Wing-Hang Lo, Yu-Liang Wu - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

SESSION 50

RM: 6D

MIXED-SIGNAL MODELING, METHODOLOGY AND SYNTHESIS

Chair: Puneet Gupta - *Univ. of California, San Diego, CA*

Going to the system level while considering the impact of process technology is a key issue in today's mixed-signal design. This sessions presents new ideas to deal with this challenge. The first paper presents a new way to estimate yield, inspired by advances in statistical timing analysis. The second paper deals with built-in compensation of process variations. The third paper presents a new divide and conquer approach to response surface modeling for analog blocks. The fourth paper finally shows an integrated approach to structural and parametric analog synthesis.

50.1 Efficient Parametric Yield Extraction for Multiple Correlated Non-Normal Performance Distributions of Analog/RF Circuits

Xin Li, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

50.2 Variation Resilient Low-Power Circuit Design Methodology using On-Chip Phase Locked Loop

Kunhyuk Kang, Keejong Kim, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

50.3s Parameterized Macromodeling for Analog System-Level Design Exploration

Jian Wang, Xin Li, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

50.4s Simultaneous Multi-Topology Multi-Objective Circuit Sizing Across Thousands of Analog Circuit Topologies

Trent L. Mcconaghy, Pieter J. Palmers, Georges G. Gielen, Michiel Steyaert - *Katholieke Univ., Leuven, Belgium*

SESSION 51

RM: 6E

DESIGN METHODS AND MANUFACTURABILITY SOLUTIONS FOR EMERGING TECHNOLOGIES

Chair: Chris Dwyer - *Duke Univ., Durham, NC*

Advances in automated design methods and design-for-manufacturability techniques are needed to harness the potential offered by a wide variety of emerging technologies. This session presents solutions to challenges encountered for a mix of technologies ranging from microfluidics to carbon nanotubes, thin-film transistors, and quantum computing.

51.1 Integrated Droplet Routing in the Synthesis of Microfluidic Biochips

Tao Xu, Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

51.2s OPC-Free and Minimally Irregular IC Design Style

Wojciech Maly - *Carnegie Mellon Univ., Pittsburgh, PA*
Yi-Wei Lin, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

51.3s Automated Design of Misaligned-Carbon-Nanotube-Immune Circuits

Nishant P. Patil, Jie Deng, Philip Wong, Subhasish Mitra - *Stanford Univ., Stanford, CA*

51.4s Quantum Circuit Placement: Optimizing Qubit-to-qubit Interactions through Mapping Quantum Circuits into a Physical Experiment

Dmitri Maslov - *Univ. of Waterloo, Waterloo, ON, Canada*
Sean M. Falconer - *Univ. of Victoria, Victoria, BC, Canada*
Michele Mosca - *Univ. of Waterloo, Waterloo, ON, Canada*

51.5s Reliability Analysis for Flexible Electronics: Case Study of Integrated a-Si:H TFT Scan Driver

Tsung-Ching Huang - *Univ. of California, Santa Barbara, CA*
Huai-Yuan Tseng, Chen-Pang Kung - *FETD/EOL/ITRI, Hsinchu, Taiwan*
Kwang-Ting Cheng - *Univ. of California, Santa Barbara, CA*

SESSION 52

RM: 6F

HIGH-PERFORMANCE SYNCHRONIZATION TECHNIQUES

Chair: Jordi Cortadella - *Universitat Politecnica Catalunya, Barcelona, Spain*

The session presents four papers targetting timing optimization using different synchronization techniques. The first paper proposes an exact polynomial approach for clock period minimization combined with delay insertion. The second paper presents an advanced strategy to improve the performance of telescopic units. The third paper explores the applicability of desynchronization to tackle variability. The fourth paper presents a novel design for self-resetting latches to improve the performance and power consumption of asynchronous pipelines.

52.1 Clock Period Minimization with Minimum Delay Insertion

Shih-Hsu Huang, **Chun-Hua Cheng**, Chia-Ming Chang, Yow-Tyng Nieh - *Chung Yuan Christian Univ., Chung Li, Taiwan*

52.2 An Efficient Mechanism for Performance Optimization of Variable-Latency Designs

Yu-Shih Su, Da-Chung Wang, Shih-Chieh Chang - *National Tsing-Hua Univ., Hsinchu, Taiwan*
Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

52.3s A Fully-Automated Desynchronization Flow for Synchronous Circuits

Nikolaos Andrikos, Luciano Lavagno - *Politecnico di Torino, Torino, Italy*
Davide Pandini - *STMicroelectronics, Agrate Brianza, Italy*
Christos P. Sotiriou - *FORTH-ICS, Heraklion, Greece*

52.4s Self-Resetting Latches for Asynchronous Micro-Pipelines

Tiberiu Chelcea, Girish Venkataramani, Seth C. Goldstein - *Carnegie Mellon Univ., Pittsburgh, PA*

SESSION 53

RM: 6A

PANEL: IP EXCHANGE - I'LL SHOW YOU MINE IF YOU'LL SHOW ME YOURS

Chair: Ron Wilson - *EDN Magazine, San Mateo, CA*
Organizer: Lauren Sarno

Between concept and production, there are many points where hardware and software developers need to exchange requirements and intellectual property. What data models need to be provided in the future? How are we going to get there? Is the current data sufficient for users to integrate IP in their systems? Who should be defining the standards: IP models, EDA tools and/ or users? Are the current standards sufficient to build SoC and ensure users' success? Is an IP exchange function clearly needed? This panel of IP and EDA vendors and end users will debate these issues.

Panelists:

Soo-kwan Eo - *Samsung Electronics , Yongin-Si, South Korea*
John Goodenough - *ARM Ltd , Sunnyvale, CA*
Serge Leef - *Mentor Graphics Corp. , Wilsonville, OR*
Laurent Lestringand - *NXP Semiconductors , Sophia Antipolis, France*
Pierre Bricaud - *Synopsys, Inc. , Mountain View, CA*
David Witt - *Texas Instruments Inc. , Dallas, TX*

Monday Tutorials

Continental Breakfast	**8:00am – 9:00am**	**Rm: 1AB**	(Breakfast and lunch is included in the tutorial fee.)
Lunch	**12:00pm – 1:00pm**	**Rm: 1AB**	

Tutorial 1 - Anatomy of Variability and Making of "Variation Tolerance" Vaccine in Nanometer Technologies

Monday, June 4, 9:00am – 5:00pm **Rm: 6C**

Organizers: **Ruchir Puri** - *IBM Corp., Yorktown Heights, NY*
Samuel Naffziger - *Advanced Micro Devices, Inc., Austin, TX*
Presenters: **Hisashige Ando** - *Fujitsu Labs, Ltd., Kanagawa, Japan*
Tanay Karnik - *Intel Corp., Hillsboro, OR*
Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*
Mike Clinton - *Texas Instruments Inc., Dallas, TX*
Richard Klein - *Advanced Micro Devices, Inc., Austin, TX*

With variability looming large, microelectronics industry is now facing one of the most important and difficult challenges of nanometer scale integrated circuits. This tutorial will discuss variability in VLSI circuits taking a holistic approach in addressing various aspects: from the detailed nature of variability to how to build variation tolerant designs. This tutorial will take a comprehensive look at the anatomy of variability in 65nm technologies and below. We will present an overview of the state of the art in variation-tolerant designs both at architecture and circuits level, while highlighting important unsolved research problems for the future. We will also discuss techniques for dealing with systematic and random sources of variability with a focus on CAD, and the impact of regularity on design manufacturability. In addition, a comprehensive analysis of variability in SRAM designs will also be presented.

Tutorial 2 - System Design for Multimedia Applications - Challenges, Design Methods and Recent Developments

Monday, June 4, 9:00am – 5:00pm **Rm: 6D**

Organizer: **Radu Marculescu** - *Carnegie Mellon Univ., Pittsburgh, PA*
Presenters: **Mihaela van der Schaar** - *Univ. of California, Los Angeles, CA*
Radu Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*
Remus Albu - *Philips Research USA, Briarcliff Manor, NY*

Embedded multimedia devices ranging from entertainment centers and multi-modal navigation devices, to mobile phones and PDAs are now designed using generic platforms rather than starting from scratch. These platforms are based on heterogeneous multiprocessor architectures which are challenging to design, program, and implement. Consequently, significant research efforts have been recently directed towards (i) efficient and scalable design of real-time multimedia applications, (ii) platform analysis and optimization techniques for multimedia systems, and (iii) Systems-on-Chip (SoC) for multimedia implementations.

This tutorial addresses the challenges and design methods for next generation of multimedia algorithms that should be complexity scalable, as well as system designs that should be multimedia aware. By scope and contents, this tutorial lies at the intersection of multiprocessor SoC platforms and low power design, software development and CAD tools for multimedia system design. This is relevant to researchers, students, and industry practitioners working to improve multimedia performance over resource-constrained systems.

Friday Tutorials

Continental Breakfast	**8:00am – 9:00am**	**Rm:1AB**	(Breakfast and lunch is included in the tutorial fee.)
Lunch	**12:00pm – 1:00pm**	**Rm:1AB**	

Tutorial 3 - Formal Assertion Based Verification in an Industrial Setting

Friday, June 8, 9:00am – 5:00pm **Rm: 6F**

Organizer: **Raj S. Mitra** - *Texas Instruments Inc., Bangalore, India*
Presenters: **Alok Jain** - *Cadence Design Systems, Inc., Noida, India*
Raj S. Mitra - *Texas Instruments Inc., Bangalore, India*
Jason Baumgartner - *IBM Corp., Austin, TX*
Pallab Dasgupta - *Indian Institute of Tech., Kharagpur, India*

Increased complexities of hardware designs have made exhaustive simulation of designs near impossible - thereby creating a need for some complementary verification technique. Recent advances in formal verification techniques, with sophisticated heuristics, have made them usable on larger blocks of hardware, but it still takes considerable skill to use these techniques on real world industrial designs, and plan the formal verification approach to be integrated into the traditional verification flows.

This tutorial describes practical techniques (abstraction techniques, partitioning methodologies, best practices, planning strategies, and integration with simulations) to formally verify real industrial designs. These techniques have been practiced and made to yield results on several industrial designs, and some of these are taken up as case studies in the tutorial.

Design, Verification, and CAD engineers will benefit from this tutorial by becoming aware of the current state of formal verification techniques (automated and manual), and knowing how to effectively apply these techniques at various stages of the design process.

Tutorial 4 - Design and Analysis of High-Performance Package and Die Power Delivery Networks

Friday, June 8, 9:00am – 5:00pm **Rm: 6A**

Organizer: **Eli Chiprout** - *Intel Corp., Hillsboro, OR*
Presenters: **Byron Krauter** - *IBM Corp., Austin, TX*
Farid N. Najm - *Univ. of Toronto, Toronto, Canada*
Rajendran Panda - *Freescale Semiconductor, Inc., Austin, TX*
Eli Chiprout - *Intel Corp., Hillsboro, OR*

This tutorial will address multiple aspects of comprehending, analyzing and designing a high performance power delivery network from die to package. At the heart of any approach are the design requirements and constraints which will be outlined. Die and package electrical modeling, dynamic co-interaction and design optimization will be detailed. The effects of inductance, both at the package and die level will be discussed. The session will describe model reduction and simulation approaches and the problem of generating an excitation for the electrical model. Decoupling capacitance optimization will also be highlighted. An overview of the latest research and concepts in "vectorless" analysis methods will be given. The tutorial will give a comprehensive view of the design problem and outline what tradeoffs should be used for the design of robust power delivery networks.

Friday Tutorials

Continental Breakfast 8:00am – 9:00am **Rm: 1AB** (Breakfast and lunch is included in the tutorial fee.)
Lunch 12:00pm – 1:00pm **Rm: 1AB**

Tutorial 5 - Soft Errors: Technology Trends, System Effects and Design Techniques

Friday, June 8, 9:00am – 5:00pm **Rm: 6C**

Organizer: **Subhasish Mitra** - *Stanford Univ., Stanford, CA*
Presenters: **Subhasish Mitra** - *Stanford Univ., Stanford, CA*
Pia N. Sanda - *IBM Corp., White Plains, NY*
Austin Lesea - *Xilinx, Inc., San Jose, CA*

Radiation-induced soft errors are getting worse in digital systems manufactured in advanced technologies. Stringent data integrity and availability requirements of enterprise computing and networking applications demand special attention to soft errors in sequential elements and combinational logic. This tutorial will discuss the impact of technology scaling on soft error rates, circuit-level modeling of soft errors, architectural impact of soft errors, challenges associated with evaluation of run-time behaviors of systems in the presence of soft errors, actual data on system behaviors in the presence of soft errors, metrics for quantifying soft error vulnerabilities, design of architectures with Built-in-Soft-Error-Resilience techniques, and actual case studies for general designs and FPGA-based designs. Two of the presenters co-founded a new workshop on soft errors (SELSE 2005-2007). Lessons learnt from these workshops will also be included in the tutorial.

Tutorial 6 - How Design Meets Yield in the Fab

Friday, June 8, 9:00am – 5:00pm **Rm: 6D**

Organizers: **Patrick Groeneveld** - *Magma Design Automation, Inc., Santa Clara, CA*
Andrew B. Kahng - *Univ. of California, San Diego, CA*
Presenters: **Ankush Oberai** - *Magma Design Automation, Inc., San Jose, CA*
Pallab Chatterjee - *SiliconMap, LLC, Livermore, CA*
Ban Wong - *Chartered Semiconductor Manufacturing, Milpitas, CA*
Robert Madge - *LSI Logic Corp., Milpitas, CA*
Christopher Progler - *Photronics Inc., Allen, TX*
Brady Benware - *Mentor Graphics Corp., Wilsonville , OR*

This tutorial will present the state-of-the-art approaches to yield learning, yield diagnosis, and yield improvement techniques that perform optimization of the chip before it reaches the fab. These techniques are increasingly critical to reaching timely volume production of high-value IC products such as GPUs and baseband processors. The five presenters will address yield from different angles, providing a uniquely broad perspective. This makes the tutorial of interest to designers, EDA professionals, product managers and researchers who have interest in the concepts of yield, yield learning, and design optimization for yield. The first part of the tutorial lays down the ways that yield is actually treated inside the fab. This includes on-die yield measurement, diagnosis and how such volume statistical data is used to improve wafer production in 'cycles of process learning'. The second set of presenters specifically addresses ways of using this knowledge to improve the design flow upstream. This includes not only a mask perspective, but also higher-level layout- and circuit-design techniques that will result in a better yielding IC production.

Friday Tutorials

Continental Breakfast	**8:00am – 9:00am**	**Rm:1AB**	(Breakfast and lunch is included in the tutorial fee.)
Lunch	**12:00pm – 1:00pm**	**Rm:1AB**	

Tutorial 7 - Circuit and CAD Techniques for Low Power Design

Friday, June 8, 9:00am – 5:00pm **Rm: 6E**

Organizers: **David Blaauw -** *Univ. of Michigan, Ann Arbor, MI*
Anantha Chandrakasan - *Massachusetts Institute of Tech., Cambridge, MA*
Presenters: **Krisztian Flautner -** *ARM Ltd, Cambridge, United Kingdom*
Alice Wang - *Texas Instrument Inc., Dallas, TX*
Nam Sung Kim - *Intel Corp., Hillsboro, OR*
David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

Strict power consumption constraints and increasing process variations are placing conflicting demands on today's design engineers. The widening margins needed to ensure robust design in the face of process variations are worsening already stressed power consumption budgets. On the other hand, many power reduction methods, such as low voltage operation, adversely effect circuit robustness. These conflicting design objectives have created a particularly difficult optimization space for today's designers. This has become the motivating force behind a recent surge of adaptive methods where the circuit operation is dynamically adjusted to address runtime workload, environmental and process conditions. This tutorial, presents an in-depth survey of recently proposed adaptive methods for power reduction in the face of increased silicon uncertainty. In the first section, we examine the different source of power and energy consumption, high lighting the importance of subthreshold and gate oxide leakage currents. We then contrast the principles behind different dynamic and leakage reduction methods, such as dynamic voltage / frequency scaling, multithreshold CMOS, variable threshold CMOS and their broad set of variations. We survey the adaptive application of these methods to address workload and process variations, highlighting so-called "canary circuit" design, in-situ delay and process monitors, and dynamic error detection and correction methods. The second section of this tutorial is a survey of the application of adaptive power reduction methods in industry, with particular emphasis on practical design and integration issues, current trends and new research opportunities. The third section discusses adaptive methods for power reduction in SRAM design, highlighting the stress that increased process variations has placed on 6T cell design and proposed solutions. The final section of this tutorial is devoted to the hardware / software interface, discussing system level issues and operating system design for adaptive workload and power management as well as industrial experiences in adaptive embedded applications.

4th UML for SoC Design Workshop

Sunday, June 3, 9:00am – 5:30pm • Rm: 6C

Workshop Registration Required
$100 - ACM/IEEE Member
$150 - Non-Member

Organizers: **Yves Vanderperren** - *Katholieke Universiteit, Leuven, Belgium*
Bruce Powel Douglass - *Telelogic, Madison, WI*
John Wolfe - *Mentor Graphics Corp., Mobile, AL*

The 4th workshop on the Unified Modeling Language (UML) for System-on-a-Chip (SoC) design consists of reviewed and selected papers from designers and researchers around the globe. UML is attracting growing interest as a system level visual language to support the tasks of specifying, analyzing, designing, and verifying SoCs. The UML for SoC Design Workshop is meant to initiate discussions, exchange experience and present state-of-the-art contributions related to UML applied to SoC design and hardware aspects. Keynotes by Wolfgang Mueller, co-Editor of the 'UML for SoC' Springer book, and Jeremy Goulding, CEO of the UML tool vendor ArtisanSW, will open the morning and afternoon sessions. Other presentations will explore embedded system specification, design, modeling, synthesis, and design flows supported by UML. Several tools will be demonstrated during the afternoon coffee break. The workshop is open to anyone interested in learning more about UML for SoC Design.

9:00am - Welcome and Morning Keynote Address

9:00am **Welcome and Introduction by the Workshop Organizers**

9:15am **Application of Diagrams in Engineering - An UML Perspective**

Wolfgang Mueller - *co-Editor of the 'UML for SoC Design' Springer book, C-LAB, Paderborn, Germany*

9:45am - Session 1: UML and SoC Languages - 1

9:45am **Model-Driven SoC/SoPC Design via UML to Impulse C**

Yi Fan Wu, Yang Xu - *Beijing Institute of Control Engineering, Beijing, China*

10:15am **Using UML as a Front-End for an Efficient Simulink-Based Multithread Code Generation Targeting MPSoCs**

Lisane Brisolara, Marcio Oliveira, Francisco Nascimento, Luigi Carro, Flávio Wagner - *Federal Univ. of Rio Grande do Sul, Porto Alegre, Brazil*

10:45am - Coffee Break

11:00am - Session 2: UML Based Methodologies / Case Studies

11:00am **FPGA Design Based on UML/MDA Approach: Application to an RF Emitter Transceiver Development**

Ali Koudri, Denis Aulagnier, Joël Champeau - *Thales, Ensieta, Brest, France*

11:30am **UML-Based Specification Method of Hardware IPs for Efficient IP Reuse**

Yeonbok Lee, Yuji Ishikawa, Shota Watanabe, Kenshu Seto, Satoshi Komatsu, Masahiro Fujita - *Tokyo Univ., Tokyo, Japan*

Seongwoon Kang, Gilark Park, Hirofumi Hamamura - *Samsung, Seoul, South Korea*

12:00pm **Automated Specifications for Chip Design Using UML**

Rad Kadengal - *SwitchCore, Lund, Sweden*

12:30pm - Lunch

2:00pm - Afternoon Keynote Address

Any Color You Like, so Long as It's Black

Jeremy Goulding - *CEO of ArtisanSW, Cheltenham, United Kingdom*

2:30pm - Session 3: UML and SoC Languages - 2

2:30pm **UML and MDA for Transactional Level Modeling**

Sara Bocchio, Alberto Rosti - *STMicroelectronics, Milano, Italy*

Elvinia Riccobene, Patrizia Scandurra - *Univ. of Milano, Milano, Italy*

3:00pm **From UML to Structural Hardware Designs**

Robert Thomson, Vassilios Chouliaras, David Mulvaney - *Loughborough Univ., Loughborough, United Kingdom*

3:30pm - Coffee Break and Tool Demos

Demos from ArtisanSW, Curtin Univ. of Technology, Federal Univ. of Rio Grande do Sul, Loughborough Univ., Mentor Graphics, STMicroelectronics, Tokyo Univ./Samsung

4:00pm - Session 4: UML Based Partitioning

4:00pm **Hardware/Software Partitioning of UML Models**

Peter Green, Yandong Lu - *Univ. of Manchester (Manchester, United Kingdom)*

4:30pm **Using UML 2.0 for the Creation of a Concept-Based SoC Design**

Waseem Ahmed - *Curtin Univ. of Technology, Sarawak, Malaysia*

Doug Myers - *Curtin Univ. of Technology, Bentley, Australia*

5:00pm - Session 5: Survey Results and Workshop Discussion

5:00pm **"It's A Long Way To Tipperary, It's A Long Way To Go", Are We There?** Moderated by the Organizers

5:30pm - Workshop Wrap-up by the Organizers

Low Power Coalition Workshop - Standards for Low Power Design Intent

Sunday, June 3, 12:30pm – 3:30pm **Rm: 6D**

Organizers: **Bill Bayer** - *Si2, Austin, TX*
Sumit DasGupta - *Si2, Austin, TX*
Nick English - *Si2, Austin, TX*

Workshop Registration Required
$75 - ACM/IEEE Member
$100 - Non-Member

Low-power requirements are a primary concern for IC designs across all product categories. They affect all electronic systems, all of which are experiencing intense pressure to reduce power consumption.

For the IC design process, several advanced techniques have emerged to reduce power consumption in SoCs including the use of multiple power domains, multiple supply voltages, dynamic and adaptive voltage and frequency scaling, and task-dependent power shut-off. However, these new techniques impose new requirements on existing design libraries, tools and methodologies.

The Low Power Coalition is developing new approaches to help specify, manage and communicate power-related information and constraints consistently throughout the design flow. One of the first actions of the LPC was the issuance of the Common Power Format specification. CPF captures low power design intent so that it can be used to consistently communicate low power constraints throughout the IC design flow. This workshop will cover some of the recent activity and planned roadmap of the LPC.

12:30pm Introduction to the Low Power Coalition
Gil Watt - *Chairman of the LPC, AMD, Boston, MA*

12:40pm Overview of CPF
Qi Wang - *Cadence Design Systems, Inc., San Jose, CA*

1:00pm Convergence Activities with other Power-Aware Formats
Gary Delp - *LSI Logic Corp., Rochester, MN*

1:20pm Library Considerations for Low Power
Rob Aitken - *ARM Ltd, Sunnyvale, CA*

1:40pm End-user Experiences
Herve Menager - *NXP, San Jose, CA*

2:00pm EDA Tool Developers for Low Power
Tom Miller - *Sequence Design, Inc., Santa Clara, CA*
Devadas Varma - *Calypto Design Systems, Inc., Santa Clara, CA*
Anand K. Iyer - *ArchPro Design Automation, Inc., Milpitas, CA*
Dave Allen - *Atrenta Inc., San Jose, CA*

2:40pm Panel Discussion (all presenters)

Design & Verification of Low Power ICs

Sunday, June 3, 4:00pm – 7:00pm **Rm: 6E**

Organizers: **Karen Bartleson** - *Synopsys, Inc., Colorado Springs, CO*
Yatin Trivedi - *Magma Design Automation, Inc., San Jose, CA*

Workshop Registration Required
$75 - ACM/IEEE Member
$100 - Non-Member

Power management is critical in IC design, especially for mobile devices, battery-operated systems, and non-portable systems with power consumption constraints.

For an interoperable, multi-vendor tool flow for low-power design and verification, the IEEE is producing a standard based on the Unified Power Format (UPF) and other contributions.

UPF is language-independent and comprehensive, specifying power-aware requirements, design intent, implementation, verification and analysis. UPF became an Accellera standard in February 2007, and EDA vendors are actively developing tool support. The IEEE process began in February, using its entity-based model for market-relevant standards. In this workshop, experts will provide everything an engineer or tool developer needs to use UPF today (with an eye towards the IEEE standard) including its purpose, technical constructs and usage. Leading EDA suppliers will show interoperability in a multi-vendor flow. Attendees will be well-equipped to leverage UPF today -- and the future IEEE standard -- to meet their low-power IC challenges.

4:00pm **Introduction**

Yatin Trivedi - *Director, Industry Partnership Program, Magma Design Automation, Inc., San Jose, CA*

4:05pm **Customer Perspective**

David Peterman - *Manager, Wireless Terminals Business Unit EDA, Texas Instruments Inc., Dallas, TX*

4:15pm **Brief History of Low Power Standards**

Shrenik Mehta - *Accellera Chair; Senior Director, Frontend Technologies & OpenSPARC Program, Sun Microsystems, Inc., Sunnyvale, CA*

Edward Rashba - *Director, New Business Ventures, IEEE Standards Association, Piscataway, NJ*

4:30pm **Technical Content of Low Power Standard**

Stephen Bailey - *Product Marketing Manager, Verification, Mentor Graphics Corp., Wilsonville, OR*

Gary Delp - *Distinguished Engineer, LSI Logic Corp., Rochester, MN*

5:15pm **Low Power Solution Flow for Design and Verification**

Mike Keating - *Synopsys Fellow, Synopsys, Inc., Mountain View, CA*

Juergen Karmann - *Senior Staff Engineer Design Methodology, Automotive, Industrial & Multimarket, Infineon Technologies AG, Munich, Germany*

6:00pm **Interoperability in Action: A Multi-Vendor Collaborative Solution**

6:45pm **Roundtable and Wrap-up**

Hardware Dependent Software (HdS)

Sunday, June 3, 1:00pm – 7:30pm **Rm: 6F**

Organizers: **Wolfgang Ecker -** *Infineon Technologies AG, Munich, Germany*
Rainer Dömer - *Univ. of California, Irvine, CA*

Workshop Registration Required
$100 - ACM/IEEE Member
$150 - Non-Member

Modern SoCs contain several programmable cores such as processors, DSPs, or ASIPs. The need for higher hardware productivity, flexibility in communication standards, and a wide number of standards, that must be supported, increase the number of programmable devices further on. There is no surprise that hardware dependent software take more and more of the development effort of a modern SoC. This workshop brings together all stakeholders of HdS that report 20 minutes each on their topics: Industry, EDA and SW-IP Providers Research. A final panel discusses the challenges of HdS on EDA.

1:00pm Welcome and Introduction by the Workshop Organizers
Hardware Dependent Software: A Growing Challenge in SoC Design?

1:30pm Session 1: The driving Factor: Industries Needs

1:30pm **HdS from Semiconductor's Perspective**
Stefan Heinen - *Infineon Technologies AG*
2:00pm **HdS from System-House Perspective**
Tommi Makkelainen - *Nokia*
2:30pm **HdS from FPGA's Perspective**
Patrick Lysaght - *Xilinx, Inc.*

3:00pm Coffee Break

3:15pm Session 2: EDA's view on HdS

3:15pm **Tools and Models for HsD Design and Analyis**
Bart Vanthournout - *CoWare, Inc.*
3:45pm **HdS from an SW-IP Provider's Perspective**
Neil Henderson - *Mentor Graphics Corp.*
4.15pm **Use Case Analysis--from device driver to Application**
Rami Mukhtar - *VaST Systems Technology*

4:45pm Coffee Break

5:00pm Session 3: HdS in Research and Education

5:00pm **MPSoC Mapping Techniques**
Stylianos Mamagkakis - *IMEC*
5:30pm **OS Modeling**
Andreas Gerstlauer - *UCI with Co-Authors from UCI and Univ. of Paderborn*
6:00pm **HdS Modeling**
Frédéric Pétrot - *TIMA Labs*

6:30pm Session 4: PANEL - Challenges of HdS towards EDA

Moderator: **Adam Morawiec** - *ECSI*
Panelists: **Neil Henderson -** *Mentor Graphics Corp.*
Bart Vanthournout - *CoWare, Inc.*
Rami Mukhtar - *VaST Systems Technology*
Pierre Bricaud - *Synopsys, Inc.*
Grant Martin - *Tensilica Inc.*

7:30pm Workshop Wrap-up

Workshop for Women in Design Automation

Managing Your Career

Monday, June 4, 9:00am – 1:45pm **Rm: 8**

Organizer: **Peggy Aycinena** - *EDA Confidential Editor and EDA Weekly Contributing Editor*

Workshop Registration Required
$50 - ACM/IEEE Member
$75 - Non-Member

WWINDA 2007 will address **Managing Your Career** and include such topics as: **The First 5 Years** – building credibility and respect; **Transitions** – from individual contributor to manager, from engineer into sales or marketing, from academia to industry; **Networking** – maintaining an effective network of colleagues; **Politics** – navigating the political landscape in industry or academia; **Balance and Scaling** – how to effectively prioritize tasks and delegate work; **Mentoring** – finding and becoming a mentor; and **Leadership** – developing skills for heading up teams, projects, and organizations. The keynote speaker and panelists will discuss their own career trajectories and offer practical suggestions to workshop attendees for increased professional success.

WWINDA Chair: **Sabina Burns** - *Sr. Director, Corp. Marketing and Communications, Virage Logic Corp.*
WWINDA Vice-Chair: **Peggy Aycinena** - *Editor, EDA Confidential*

Steering Committee

Nanette Collins - *Publicity Chair, 44th DAC*
Marie R. Pistilli - *Co-Chair, Board of Directors, MP Associates, Inc.*
Daya Nadamuni - *Independent Analyst, WWINDA Past Chair*

WWINDA Mission Statement

To be a workshop of relevance to women in Electronic Design Automation, to provide a forum for the interchange of ideas for successful careers in the EDA profession, to address the particular needs of professional women, and to provide an opportunity for peer networking.

Keynote Address

Dr. Terri Fiez is an IEEE Fellow and Professor of Electrical Engineering at Oregon State University. A panel discussion will follow the keynote, and presentation of the annual Marie R. Pistilli Women in EDA Achievement Award for outstanding contributions towards the advancement of women in electronic design automation. The professional development workshop also includes a continental breakfast and lunch and an excellent opportunity to network with other design automation industry professionals.

Panel: Career Trajectories - The Voices of Experience

Moderator: **Peggy Aycinena** - *EDA Confidential Editor and EDA Weekly Contributing Editor*
Speakers: **Penny Herscher** - *President & CEO, firstRain*
Daphne Huckaby - *Design Management, QUALCOMM, Inc.*
Daya Nadamuni - *Chief Analyst, Gary Smith EDA*
Diana Feng Raggett - *President & CEO, Javelin Design Automation*

Introduction to Chips and EDA for a Non-Technical Audience

Monday, June 4, 10:00am – 12:00pm **Rm: 9**

Organizer: **Pamela McDaniel** - *Synopsys, Inc., Mountain View, CA*

Workshop Registration Required
$10 - Registration Fee

How can it be that cell phones continue to do more things while getting smaller every year? Are you amazed and curious about berries that are hand-held computers instead of something you put on your breakfast cereal? Do the technical people around you seem to know everything while you're secretly and hopelessly lost?

If you are a non-technical professional in the Electronic Design Automation (EDA) or chip industry and want to know more about how chips are designed and manufactured, this workshop is for you. Whether you're just starting out or you've been with an EDA or chip company for a while, this two-hour session will give you just what you need to gain a basic understanding of chips and EDA. It will help you feel more informed and comfortable in the fast-paced and amazing world of chips and EDA.

This workshop provides:

* A simplified explanation of how chips are designed and manufactured
* An understanding of how essential EDA is to chip design
* An opportunity to see and touch the parts that make up chips and electronic products
* A non-threatening, fun event with working knowledge to take away

This workshop is for:

* Non-engineering staff from technology companies
* Analysts and media people unfamiliar with EDA and semiconductor industries
* Educators and students who are curious about chip technology and design automation
* Friends and relatives of technical people

Workshop objectives:

* Provide a basic understanding of EDA and semiconductors to non-technical people
* Present information in simple, easy-to-understand terms
* Use hands-on parts (wafers, chips, masks …) for enhanced experience
* Encourage people to join and invest in the EDA industry
* Address ongoing requests to help non-technical people understand the EDA industry.

Speaker: **Karen Bartleson** - *Synopsys, Inc., Colorado Springs, CO*

3rd Integrated Design Systems Workshop

Models for Design and Manufacturing - How Modeling Challenges are Touching Every Aspect of IC Design

Monday, June 4, 12:00pm – 5:00pm **Rm: 6A**

Organizers: **Bill Bayer** - *Si2, Austin, TX*
Sumit DasGupta - *Si2, Austin, TX*
Nick English - *Si2, Austin, TX*

Workshop Registration Required
$50 - ACM/IEEE Member
$75 - Non-Member

Rules-based design methods are rapidly being replaced by the need for models representing everything in modern chip design flows -- from the system-level analysis through foundry process variation. This workshop will bring together experts in important modeling areas such as: delay calculation, statistical timing, low power, DFM, yield, IP blocks, pcells, etc.

Speakers will first examine the necessity for model based design and how it is impacting design tools and flows, convergence/divergence issues, business implications and anticipated interactions between foundries, fabless design and EDA. They will then discuss significant research, development and cooperation across the industry, and debate whether it is sufficient and timely enough to meet the needs of coming technology nodes and what impacts can be expected on IC business models. Lunch is provided.

1. Modeling for Power Minimization
Gary Delp - *LSI Logic Corp., Rochester, MN*
David Hathaway - *IBM Corp., Essex Junction, VT*

2. Modeling for Timing
Bob Kezer - *Intel Corp., Mont Vernon, VT*
Rob Aitken - *ARM Ltd, Sunnyvale, CA*

3. Modeling for Design Reuse
Chris Rowen - *Tensilica Inc., Santa Clara, CA*
James Spoto - *Independent Consultant, Irvine, CA*

4. Modeling for DFM/DFY
Walter Ng - *Chartered Semiconductor Manufacturing, Milpitas, CA*
Andrew B. Kahng - *Univ. of California, La Jolla, CA*

5. Panel Discussion: All speakers
Moderator: **Chandu Visweswariah** - *IBM Corp., Yorktown Heights, NY*

Hands-On-Tutorials

Monday, June 4, 9:00am – 12:00pm **Rm: 11A**

Standard Cell Library and Hard IP Design

Presented by Blaze DFM, Inc. / Ponte Solutions, Inc. / Sagantec

This Design for Manufacturing (DFM) hands-on tutorial addresses the topic of designing standard cells and other hard IP to minimize manufacturing issues.

Currently, most DFM issues are encountered at metal 2 and below, which means the primary impact is on IP blocks including standard cells, memories and hard IP. Finding and correcting DFM issues in these elements plays a major role in the effort to improve yield.

Tutorial participants will learn how critical area analysis (CAA) and lithography simulation are used in concert with layout optimization to identify and repair weak spots in the layout that can harm yield. Example cells will be examined by both Ponte's Yield Analyzer™ CAA tool and Blaze's Halo™ lithography simulator, which will identify issues for automatic correction by Sagantec's DFM-Fix™ layout optimizer.

Monday, June 4, 2:00pm – 5:00pm **Rm: 11A**

Design for Manufacturing Variability with Confidence

Presented by ClearShapeTechnologies, Inc. / Cadence Design Systems, Inc. / Texas Instruments Inc. / UMC

With the introduction of sub-90 nm technologies, systematic variations cause catastrophic and electrical failures. This means that silicon is different from what is modeled and designed based on ideal layout. The result is large margins applied at every stage of the design, long timing closure cycle time, long manufacturing turnaround times, catastrophic and parametric yield loss and major bottlenecks at the RET/OPC stage.

Despite the use of the resolution enhancement technologies during manufacturing, there is residual variability resulting from the printing of the structures. These systematic variations depend on the layout shapes and are deterministic and predictable when modeled correctly. These variations have a predictable impact on the critical dimension (CD) of a transistor gate, and the shape of an interconnect wire.

In this tutorial, technology leaders in chip design, semiconductor manufacturing, physical implementation and DFM analysis will discuss the intricacies and deliver a practical solution to the variability challenge.

Hands-On-Tutorials

Tuesday, June 5, 2:00pm – 5:00pm **Rm: 11A**

Deploying Statistical Timing -- from Characterization to Analysis and Optimization

Presented by Altos Design Automation / Cadence Design Systems, Inc.

Statistical static timing analysis (SSTA) offers a number of advantages over traditional corner based static timing analysis (STA), most notably it provides a more realistic estimation of timing relative to actual silicon performance. Armed with a better answer, designers can focus their optimization efforts on the paths that have the biggest impact on overall performance resulting in improved yield, reduced power (especially leakage) and shorter design cycles. In addition, STA may miss chip failures due to process variations that SSTA will be able to pin-point. This hands-on tutorial will show how to incorporate SSTA into your existing design methodology.

The tutorial will contrast the results of performing analysis and optimization using both STA and SSTA on a provided design. The attendees will also learn how to easily and efficiently characterize a statistical timing library that accounts for process variations.

The attendees will walk away with practical experience of the complete SSTA design methodology and a detailed understanding of its key advantages.

Wednesday, June 6, 9:00am – 12:00pm **Rm: 11A**

Approaching Yield in the Nanometer Age: The Framework for an Extensible DFM Methodology

Presented by Mentor Graphics Corp. / Chartered Semiconductor Manufacturing / Sierra Design Automation, Inc. / ARM Ltd

As we dive deeper into the nanometer space, we must rethink the way we design. Tools, techniques, and methods that once worked without fail cannot hold up at the 65 and 45 nm depths, making it more challenging than ever to achieve yield.

Not only are more DRC rules required, but the rules are becoming much more complex in light of more manufacturing issues. Yet advanced DRC is still not enough. We must redefine the sign-off process itself to include a spectrum of new methods that assess design quality. This means that the fabless model increases in importance where foundry information must flow freely so more of the responsibility for yield can fall on the shoulders of the designer.

Therefore, in the nanometer age, sign-off must include not only fundamental, rule-based physical verification and parasitic extraction but also a set of automated technologies that help improve yield by enhancing design itself.

DFM solutions must deliver these automated technologies to the designer in a practical and easy to use way. This includes new ways to visualize and prioritize the data produced by the analytical tools. It also requires that existing tools expand their architectures to provide yield characterization and enhancement capabilities. Finally, the most successful DFM methodologies in the nanometer age will apply these new capabilities throughout the design flow — not just at the point of sign-off.

This tutorial will go into detail on these technical challenges and solutions within both the business and historical context of the IC design and manufacturing process. It will show the importance of the fabless model as part of a more holistic DFM methodology and describe what the new tools should look like.

Hands-On-Tutorials

Wednesday, June 6, 2:00pm – 5:00pm **Rm: 11A**

Manufacturing Aware Optimization

Presented by Blaze DFM, Inc. / Taiwan Semiconductor Manufacturing Company, Ltd.

This hands-on tutorial addresses the topic of manufacturing variations and their impact on the design flow. It covers approaches for modeling and predicting manufacturing variations, and using the predicted manufacturing variation data to optimize designs using novel electrical DFM techniques.

The tutorial begins with an overview of issues addressed in the TSMC DFM Design Kit (DDK). This includes a description of DFM design issues and modules provided by TSMC to EDA vendors to bring awareness of DFM effects into the chip design flow.

Participants will run the Blaze™ IF fill synthesis tool from Blaze DFM, which uses a TSMC-provided density modeling engine to drive fill synthesis. Different fill synthesis considerations will be discussed, and the impact of fill on timing and timing variation will be shown.

A leakage power reduction methodology using the Blaze MO™ gate-length biasing will also be presented.

Thursday, June 7, 9:00am – 12:00pm **Rm: 11A**

Timing Closure: Requirements for Variation Aware Design

Presented by Extreme DA Corp. / Texas Instruments Inc./ PDF Solutions / UMC

Scaling of the designs leads to the emergence of new physical challenges that limit continuing improvement of circuit performance. Among them, statistical process and environmental variations have caused headache to designers. In previous silicon generations, conservative margins could be afforded to guard-band against these uncertainties. However at the technologies nodes of 65nm and below, more realistic analysis is needed to deliver silicon that meets yield and performance goals.

In this tutorial, the audience will be introduced to the components of a next generation timing analysis methodology. We show practical examples starting from front-end and back-end process characterization that captures variability statistics of systematic and random variations.

Experiences from Foundry, IDM, and EDA perspectives will be covered. The use of the extracted variability data in the library characterization, RC extraction, timing analysis and optimization flows will be demonstrated.

Sponsors

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ACM is an educational and scientific society uniting the world's computing educators, researchers and professionals to inspire dialogue, share resources and address the field's challenges. ACM strengthens the profession's collective voice through strong leadership, promotion of the highest standards, and recognition of technical excellence. ACM supports the professional growth of its members by providing opportunities for life-long learning, career development, and professional networking. For more information, please visit http://www.acm.org

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ACM/SIGDA

The Resource for EDA Professionals ACM/SIGDA (Special Interest Group on Design Automation) has a tradition of over forty years of supporting conferences and the EDA profession. In addition to sponsoring DAC, SIGDA sponsors ICCAD, DATE, and ASP-DAC, plus approximately 15 smaller symposia and workshops. SIGDA provides a broad array of additional resources to our members, to students and professors, and to the EDA profession in general. SIGDA organizes the University Booth and Ph.D. Forum at DAC and the CADathlon at ICCAD, and funds various scholarships and awards. SIGDA provides its members with full access to SIGDA-sponsored conference proceedings in the ACM Digital Library and the SIGDA E-Newsletter containing information on upcoming conferences and funding opportunities, emailed to SIGDA members twice each month. The SIGDA E-Newsletter also includes SIGDA News which highlights the most relevant events in the EDA and semiconductor industry, and the "What is...?" column that brings to the attention of EDA professionals the most recent topics of interest in design automation. SIGDA has recently initiated the creation of eight Technical Committees in various areas of EDA, ranging from Physical Design and Logic Synthesis, to System Level Design, Low Power Design, Reconfigurable Computing, Testing, Verification, and Emerging Technologies. Attend the 10th Ph.D. Forum/Member Meeting on Tuesday evening to find out how the Technical Committees provide a link between SIGDA activities and various technical areas in EDA. Finally, SIGDA provides strong support for the ACM journal TODAES (Transactions on Design Automation of Electronic Systems).

For further information on SIGDA's programs and resources, see http://www.sigda.org. In addition, SIGDA members may also want to consider joining our parent organization, ACM. ACM membership provides access to a variety of ACM products and resources, including discounts on conferences, subscriptions to ACM journals and magazines, and the ACM Digital Library, an invaluable IT resource. For further details, see ACM's home page at http://www.acm.org. As an EDA professional, isn't it time YOU joined SIGDA?

Sponsors

SIGDA/DAC University Booth

This year marks the 20th University Booth at the Design Automation Conference. The booth is an opportunity for university researchers to display their results and to interact with visitors from industry. Priority is given to presentations that complement the conference technical program. Demos that highlight benchmark results are also encouraged. The Design Contest winners, DAC speakers, and PhD Forum participants are invited to give demonstrations presenting their work at the University Booth. In honor of its 20th year, look for a completely redesigned booth, a special section on Microelectronic Systems Education, and a related call for papers from the ACM Transactions on Design Automation for Electronic Systems (TODAES). The schedule of presentations is published at the conference and will also be available on the SIGDA web site at http://www.sigda.org/programs/Ubooth/Ubooth2007/. The organizers thank the Design Automation Conference for its continued support of this project.

44th DAC Proceedings DVD

Additional copies of the 2007 DAC DVD may be ordered prepaid from:
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EDA Consortium

The EDA Consortium (EDAC) is the international industry association for the providers of tools and services that enable engineers to create the world's electronics products. Its mission is to promote the health of the EDA industry by addressing common industry needs and providing valued services.

By publishing the Market Statistics Service (MSS) EDAC enables worldwide tracking of revenue for CAE, IP, PCB, ESL and DFM. By co-sponsoring the prestigious annual Phil Kaufman Award, the EDA Consortium and the IEEE Council on EDA bring industry-wide recognition to distinguished contributions to EDA. As a co-sponsor of DAC and DATE, the EDA Consortium represents the interests of exhibiting companies.

EDAC members influence industry initiatives by participating on committees to address common needs as well as play a positive role in reducing costs for the industry and its customers. Examples of committee accomplishments include an EDA operating systems roadmap, anti-piracy education, licensing guidelines, and the reduction of governmental export controls.

EDAC offers international forums and symposiums which are well attended by industry CEOs, executives, press, and analysts. These events cover topics of interest to emerging and large EDA companies alike.

EDA Consortium members receive a 10% discount on DAC booth/suite space. For more information call 408-287-3322 or visit www.edac.org. EDAC is located in San Jose, CA, USA.

Sponsors

IEEE Circuits and Systems Society

The IEEE Circuits and Systems Society (CASS) is one of the largest societies within IEEE and in the world devoted to the analysis, design, and applications of circuits, networks, and systems. It offers its members an extensive program of publications, meetings and technical and educational activities, encouraging an active exchange of information and ideas. The Society's peer reviewed publication activities include: Trans. on CAD; Trans. on CAS-Part I: Regular Papers; Trans. on CAS-Part II: Express Briefs and Trans. on CAS for Video Technology. In addition, there are Trans. on VLSI; Trans. on Multimedia and Trans. on Mobile Computing which are co-sponsored with IEEE sister societies and its newest publication, Trans. on Biomedical Circuits and Systems also co-sponsored with an IEEE sister society. Also new this year is the CASS Electronic Newsletter. CASS also sponsors or co-sponsors a number of international conferences, which include the Design Automation Conference (DAC), the Int'l Conference on Computer-Aided Design (ICCAD) and the Int'l Symposium on Circuits and Systems (ISCAS). A worldwide comprehensive program of advanced workshops including a new series on "Emerging Technologies in Circuits and Systems," as well as our continuing education short courses, bring to our worldwide membership the latest developments in cutting-edge technologies of interest to industry and academia alike.

The IEEE/CASS has been serving its membership for over 50 years with such member benefits as:

- Discounts on all Society publications, conferences and workshops (including co-sponsored and sister society publications and conferences)
- The Society Magazine which includes articles on emerging technologies, society news and current events
- Opportunities to network with peers and experts within our 17 focused committee meetings, the local events of over 60 chapters and more than 20 annual conferences/workshops
- Opportunity to read and review papers, write articles and participate in the Society's government
- The CASS Electronic Newsletter
- And all the personal and professional benefits of IEEE/CASS/CANDE/CEDA membership

Computer Aided Network Design

Computer Aided Network Design (CANDE) is a joint technical committee of the IEEE Circuits and Systems Society and the Council on Electronic Design Automation. CANDE is dedicated to bringing design automation professionals together to further their education, to assist in building relationships, and to sponsor initiatives which grow the CAD/EDA industry. CANDE sponsors a workshop in the Fall to address emerging technologies and to provide an opportunity for the generation of new ideas. CANDE is the sponsoring technical committee from CASS for both DAC and ICCAD.

For more information, please contact:
IEEE/CASS/CANDE.
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Council on Electronic Design Automation

The Council on Electronic Design Automation (CEDA) is an IEEE Council formed in 2005 by the IEEE Technical Activities Board. CEDA aims to bring together the EDA-related activities that run through many of the IEEE's societies, conferences and workshops. CEDA's responsibilities include sponsorship of several conferences and publications, such as ICCAD, DAC, and the Transactions on CAD and the sponsorship of a Distinguished Speaker Series. Members of CEDA include the IEEE Antennas and Propagation, Computer, Circuits and Systems, Electron Devices, Microwave Theory and Techniques, and Solid State Circuits Societies. For more information on CEDA, go to www.ieee-ceda.org.

Awards

Marie R. Pistilli Women in EDA Achievement Award

Jan Willis - *Senior Vice President, Industry Alliances, Cadence Design Systems, Inc.*

For her significant contributions in helping women advance in the field of EDA technology.

P.O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering

The objective of the P.O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under-represented groups (women, African American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship and SIGDA continues to administer the program for DAC. DAC normally funds two or more $4000 scholarships, renewable up to five years, to graduating high school seniors.

The 2007 winners are:

Erin Powers - *attending Harvey Mudd College, Claremont, CA*

Sean Sanders - *attending Georgia Institute of Technology, Atlanta, GA*

For more information about the P.O. Pistilli scholarship, contact Dr. Cherrice Traver, ECE Dept., Union College, Schenectady, NY 12308. email: traverc@union.edu.

A. Richard Newton Graduate Scholarships

The DAC Executive Committee has chosen to name our existing DAC Graduate Scholarships after the late Professor A. Richard Newton. We feel that supporting young faculty and graduate research is an appropriate way to honor his vision and carry out some of his goals.

Each year the Design Automation Conference sponsors several $24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in "design and test automation of electronic and computer systems". Each scholarship is awarded directly to a university for the Faculty Investigator to expend in direct support of one or more DA graduate students. The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are: the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Advisor: Kartik Mohanram, *Department of Electrical and Computer Engineering, Rice Univ., Houston, TX*
Students: Quming Zhou, Mihir Choudhury
Design Optimization for the Robustness to Single-event Effects in sub-100nm Process Technologies

Advisor: Baris Taskin, *Department of Electrical and Computer Engineering, Drexel Univ., Philadelphia, PA*
Student: Vinayak Honkote
Routing for Resonant Clocking Technology in Multi-GHz Range

2006 Phil Kaufman Award For Distinguished contributions to EDA: Sponsored by the EDA Consortium

Dr. Robert Dutton, *Robert and Barbara Kleist Professor of Engineering at Stanford Univ. and Director of the Integrated Circuits Laboratory*

Robert Dutton is the recipient of the prestigious 2006 Phil Kaufman Award for his contributions as the "Father of TCAD (Technology Computer Aided Design)" which he pioneered and helped transition into successful industrial and commercial deployments.

Awards

IEEE Emanuel R. Piore Award

Randal E. Bryant - *Carnegie Mellon Univ., Pittsburgh, PA*

The IEEE Emanuel R. Piore Award was established by the IEEE Board of Directors in 1976 for outstanding contributions in the field of information processing in relation to computer science, deemed to have contributed significantly to the advancement of science and to the betterment of society. The Award is named in honor of Emanuel Piore, who was an enlightened American scientist who understood the value of basic scientific research, as well as that of applied research. The award is sponsored by the IEEE Emanuel R. Piore Award Fund.

IEEE Circuits and Systems Society 2007 Industrial Pioneer Award

Rob A. Rutenbar – *Carnegie Mellon Univ., Pittsburgh, PA*

For pioneering contributions to the development of EDA tools for synthesis of analog/mixed-signal integrated circuits and to their dissemination into widespread use in semiconductor industry by industrial cooperation and by starting up a CAD company.

IEEE Circuits and Systems Society 2007 Outstanding Young Author Award

Zhuo Li - *IBM Austin Research Laboratory, Austin, TX*

For the paper entitled, ***A Fast Algorithm for Optimal Buffer Insertion,*** IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 24, no. 6, pp. 879-891, June 2005 (paper co-authored with Weiping Shi)

IEEE Transactions on Computer-Aided Design 2007 Donald O. Pederson Best Paper Award

Guoyong Shi - *Shanghai Jiao Tong Univ., Shanghai, China*

Bo Hu - *Cadence Design Systems, Inc., San Jose, CA*

C.-J. Richard Shi - *Univ. of Washington, Seattle, WA*

For the paper entitled, ***On Symbolic Model Order Reduction***, IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 25, no. 7, pp. 1257-1272, July 2006

IEEE Transactions on Circuits and Systems 2007 Guillemin-Cauer Best Paper Award

Payam Heydari - *Univ. of California, Irvine, CA*

Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

For the paper entitled, ***Model-Order Reduction Using Variational Balanced Truncation with Spectral Shaping,*** IEEE Transactions on Circuits and Systems: Regular Papers, vol. 53, no. 4, pp. 879-891, April 2006

2007 IEEE Fellows

Ruchir Puri - *IBM Corp., Yorktown Heights, NY*
For contributions to automated logical and physical design of electronic circuits.

Anirudh Devgan - *Magma Design Automation, Inc., Austin, TX*
For contributions to electrical analysis, and simulation of integrated circuits.

ACM Paris Kanellakis Theory and Practice Award

Robert K. Brayton - *Univ. of California, Berkeley, CA*

For leading the development and practical realization of algorithms for logic synthesis and for electronic system simulation, thereby helping to create key enabling technologies for the Electronic Design Automation industry.

Awards

ACM Transactions on Design Automation of Electronic Systems (TODAES) 2007 Best Paper Award

Impact of intercluster communication mechanisms on ILP in clustered VLIW architectures • Volume 12, Issue 1, January 2007, Page 1
Anup Gangwar - *Freescale Semiconductor, Inc., India Pvt. Ltd., India*
M. Balakrishnan - *Indian Institute of Technology, Delhi, India*
Anshul Kumar - *Indian Institute of Technology, Delhi, India*

ACM/SIGDA Distinguished Service Awards

Daniel Gajski - *Univ. of California, Irvine, CA*
Mary Jane Irwin - *Pennsylvania State Univ., University Park, PA*
Donald E. Thomas - *Carnegie Mellon Univ., Pittsburgh, PA*
Chuck Shaw - *Cadence Design Systems, Inc., San Jose, CA*
For outstanding contributions to the creation of the SIGDA/DAC University Booth, on the occasion of its 20th edition.

Soha Hassoun - *Tufts Univ., Medford, MA*
Steve P. Levitan - *Univ. of Pittsburgh, Pittsburgh, PA*
For outstanding contributions to the creation of the SIGDA Ph.D. Forum at DAC on the occasion of its 10th edition.

Richard Auletta - *Cadence Design Systems, Inc., Louisville, CO*
For over a decade of service to SIGDA as University Booth Coordinator, Secretary/Treasurer, and Executive Committee Member-at-Large.

ACM Outstanding Dissertation in Electronic Design Automation Award

Haifeng Qian - *Univ. of Minnesota, Minneapolis, MN*
For the dissertation entitled ***Stochastic and Hybrid Linear Equation Solvers and their Applications in VLSI Design Automation***

SIGDA Outstanding New Faculty Award

Michael Orshansky - *Univ. of Texas, Austin, TX*
For a junior faculty member early in her or his academic career who demonstrates outstanding potential as an educator and/or researcher in the field of electronic design automation.

44th DAC Best Paper Candidates

Fifteen papers were nominated by the Technical Program Committee as a DAC Best Paper Candidate; six in front-end design and nine in back-end design. Final decisions will be made after the papers are presented at the conference. The awards for the best papers, one in front-end design and one in back-end design, will be presented at 12:30 on Thursday, June 7 in Ballroom 20ABC, just before the Keynote Address.

- ***3.4 Simulink-Based MPSoC Design Flow: Case Study of Motion-JPEG and H.264***
- ***6.2 Width-dependent Statistical Leakage Modeling for Random Dopant Induced Threshold Voltage Shift***
- ***8.1 Voltage-Frequency Island Partitioning for GALS-based Networks-on-Chip***
- ***9.1 Interdependent Latch Setup/Hold Time Characterization via Euler-Newton Curve Tracing on State-Transition Equations***
- ***13.1 Endurance Enhancement of Flash-Memory Storage Systems: An Efficient Static Wear Leveling Design***
- ***14.1 Comparative Analysis of Conventional and Statistical Design Techniques***
- ***16.1 Period Optimization for Hard Real-time Distributed Automotive Systems***
- ***17.3 Towards An Ultra-Low-Power Architecture Using Single-Electron Tunneling Transistors***
- ***20.1 Characterization and Estimation of Circuit Reliability Degradation under NBTI using On-Line IDDQ Measurement***
- ***23.1 Progressive Decomposition: A Heuristic to Structure Arithmetic Circuits***
- ***24.1 Parameter Finding Methods for Oscillators with a Specified Oscillation Frequency***
- ***27.2 RQL: Global Placement via Relaxed Quadratic Spreading and Linearization***
- ***30.4 New Test Data Decompressor for Low Power Applications***
- ***33.3 On-The-Fly Resolve Trace Minimization***
- ***34.1 An Integer Linear Programming Based Routing Algorithm for Flip-Chip Design***

Student Design Contest

The Student Design Contest promotes excellence in the design of electronic systems by providing a competition for graduate and undergraduate students at universities and colleges. It is co-organized by ISSCC and DAC. This year we received nearly 50 submissions in three categories:. operational systems, operational chips, and conceptual designs based on simulation. 9 award winners were selected.

The Student Design Contest is jointly sponsored by DAC, industry sponsors, and ISSCC.

Awards will be given at the DAC Pavilion on Monday, June 4 from 12:00pm - 1:00pm. The ceremony will include brief overview presentations from each winning project team.

Award Contributors:

Student Design Contest Co-Chairs

William J. Bowhill Intel Corp. Hudson, MA	Byunghoo Jung Purdue Univ. West Lafayette, IN	Alan Mantooth Univ. of Arkansas Fayetteville, AR

2007 Student Design Contest Winners

- ***A Wireless Implantable Microsystem for Continuous Blood Glucose Monitoring***
  Mohammad Mahdi Ahmadi, Graham A. Jullien - *Univ. Of Calgary*
- ***Design of an Ultra-Low Voltage UWB Baseband Processor***
  Vivienne Sze, Anantha P. Chandrakasan - *MIT*
- ***HBS: A Handheld Breast Cancer Detector Based on Frequency Domain Photon Migration***
  Keun Sik No, Qiang Xie, Pai H. Chou - *Univ. of California, Irvine*
  Richard Kwong, Albert Cerussi, Bruce J. Tromberg - *Beckman Laser Institute*
- ***An Energy-Efficient Reconfigurable Multiprocessor IC for DSP Applications***
  Guichang Zhong, Alan N. Willson, Jr. - *Univ. of California, Los Angeles*
- ***The Scale Vector-Thread Processor***
  Ronny Krashinsky, Christopher Batten, Krste Asanovic - *MIT*
- ***A 94dB SFDR 78dB DR 2.2MHz BW Multi-bit Delta-Sigma Modulator with Noise Shaping DAC***
  Jianzhong Chen, Yong Ping Xu - *National Univ. of Singapore*
- ***A 230mV-to-500mV 375KHz-to-16MHz 32b RISC Core in 0.18μm CMOS***
  Jian-Shiun Chen, Yi-Ming Wang, Yu-Juey Chang, Jinn-Shyan Wang, Tien-Fu Chen, Chingwei Yeh - *Natl. Chung Cheng Univ.*
- ***A 152mW/195mW Multimedia Processor with Fully Programmable 3D Graphics and MPEG/H.264/JPEG for Handheld Devices***
  Jeong-Ho Woo, Ju-Ho Sohn, Hyejung Kim, Hoi-Jun Yoo - *KAIST*
  Euljoo Jeong, Jongcheol Jeong, Suk Joong Lee - *Corelogic, Inc.*
- ***A 252Kgates/4.9Kbytes SRAM/71mW Multi-Standard Video Decoder for High Definition Video Applications***
  Chih-Da Chien, Yi-Hung Shih, Chien-Chang Lin, He-Chun Chen, Chih-Wei Wang, Cheng-Yen Yu, Jiun-In Guo - *Natl. Chung Cheng Univ.*
  Chih-Liang Chen, Ching-Hwa Cheng - *Feng-Chia Univ.*

Adjunct Meetings

EDA Consortium Executive Reception co-sponsored by EDN Magazine & TSMC

Sunday, June 3 **5:00pm – 7:00pm**

San Diego Marriott Hotel and Marina/Marina Ballroom

Join the leaders of the EDA industry for a lively evening of networking and a panel discussion by distinguished members of the technology community. This EDA Consortium event, co-sponsored by EDN Magazine, TSMC, and representatives of the TSMC design ecosystem, will be an industry-wide welcome to DAC and an opportunity to re-connect with a diverse group of colleagues. Kick off DAC with EDAC!

IEEE Council on EDA's Distinguished Speaker Lecture and Reception

Monday, June 4 **6:00pm – 8:00pm** **Rm: Sails Pavilion**

The IEEE Council on Electronic Design Automation (CEDA) is holding its second annual distinguished speaker lecture at DAC. The lecture will host the recipient of the 2007 IEEE Transactions on Computer-Aided Design Donald O. Pederson Best Paper Award. In addition to this lecture, EDA award recipients (e.g., IEEE Fellow, IEEE Technical Field Awards, etc.) will be recognized for their accomplishments at the accompanying reception.

Productivity Impact Luncheon

Produced by the EDA Consortium and FSA, with contributions from EE Times - Admission $60

Tuesday, June 5 **12:00pm – 1:30pm** **Rm: Ballroom 20D**

Themed "Changing the Dialogue between Engineers & Management," the luncheon will examine factors affecting engineering productivity while presenting dialogue vignettes, research and practical examples. Speakers include:

Kathryn Kranen - Jasper Design Automation, Mountain View, CA, EDA Consortium, Vice-Chairperson
Brian Fuller - EE Times, San Francisco, CA
Lisa Tafoya - FSA, Dallas, TX

10th Annual SIGDA Ph. D. Forum/Member Meeting

Tuesday, June 5 **6:30pm – 8:00pm** **Rm: Sails Pavilion**

SIGDA invites you to attend our 10th annual PhD Forum and Member Meeting in DAC 2007. SIGDA members are invited, as are all members of the EDA Community. We will begin with an overview of SIGDA programs including the newly created Technical Committees, followed by the presentation of this year's ACM Paris Kanellakis Practice and Theory Award, as well as ACM/SIGDA Distinguished Service and Technical Leadership Awards. However, the main focus of the meeting will be the Ph.D. Forum. Aimed at strengthening ties between academia and industry, students will present posters and discuss their Ph.D. dissertation research with interested attendees. The Ph.D. Forum gives students feedback on their research, and gives the EDA community a preview of work in process. Light refreshments will be served at 7:30 pm. For more information, see http://www.sigda.org/daforum.

Additional Meetings

Design Automation Summer School

Saturday, June 2 & Sunday, June 3 8:00am – 6:00pm Rm: 24AB

Graduate students and young professionals in design automation are invited to participate in the third Design Automation Summer School (DASS) held on June 2-3 at DAC this year. DASS offers attendees an opportunity to participate in a two-day intensive course on selected areas of research and development in design automation. Each topic of instruction in this course is covered by a distinguished speaker who defines the topic, describes recent accomplishments in considerable detail, and outlines upcoming challenges. Interactive discussions and follow-up activities among the participants round off an intensive, yet comprehensive activity geared towards graduate students and young professionals in design automation.

DASS is co-sponsored by the National Science Foundation, ACM SIGDA, and the DAC Professional Development Fund. The deadline for all applications is April 27, 2007. Full or partial scholarships are extended to a majority of the selected student applicants. Further details on the application process and the technical program for DASS 2007 are available at http://www.ece.rice.edu/~kmram/dass07.

ACM/SIGDA Symposia/Workshop Leaders Luncheon

Monday, June 4 12:00pm – 2:00pm Rm: 23AB

Organizers of symposia and workshops sponsored by ACM/SIGDA, as well as ACM/SIGDA volunteers and Technical Committee members are invited to a lunch get-together. ACM staff and SIGDA Board Members will be available for detailing and explaining the steps of starting or organizing an event. A brief overview of other new ACM/SIGDA activities will be presented followed by updates from SIGDA's newly established Technical Committees.

The IP-XACT Specification in Action: Open Public Meeting of The SPIRIT Consortium

Monday, June 4 5:00pm – 9:00pm Rm: 26AB

How can you approach integrating multi-vendor flows? Do your tool suppliers and IP providers support IP-XACT? What is the most recent progress in this IP meta-data standard? The open, general meeting of The SPIRIT Consortium will present the latest adoption stories, vendor demos, and technical updates on practical approaches to more integrated design flows. Beyond extending usage into the RTL and hardware implementation space, the upcoming releases of the specification will enable the ESL to RTL flow with consistent language-neutral architectural descriptions.

Si2 Members Meeting

Monday, June 4 6:00pm – 7:30pm
Rm: 27A

The Annual Si2 Members Meeting is open to both member and non-member companies who are interested in Si2 activities in such areas as OpenAccess, advanced library modeling systems, DFM and low-power. A Happy Hour will be held at the beginning and end of the meeting with refreshments and light hors d'oeuvres. To register for this event, leave a message at this link: http://www.si2.org/?page=455

Synopsys University Reception

Monday, June 4 6:30pm – 8:30pm
Rm: 23ABC

University professors and students are invited to join Synopsys and Sun Microsystems for an evening reception including drinks and hors d'oeuvres. Prize drawings will be held throughout the evening and the following keynote presentations will be featured.

Scaling the Power Wall

Dr. Jan M. Rabaey - *Donald O. Pederson Distinguished Professor, Director Gigascale Systems Research Center, Scientific Director Berkeley Wireless Research Center*

Power Reduction: Is it Time to Re-examine Asynchronous Design?

Dr. Robert Damiano - *Synopsys Fellow and Vice President, Advanced Technology Group*

Join us for a chance to win a Nintendo Wii!

Additional Meetings

Cadence-ARM Wireless Technical User Group Meeting

Tuesday, June 5 **7:30am – 9:00am** **Rm: 30CDE**

See real-world examples of successful ARM and Cadence technologies deployed for wireless applications.

Advances in Parallel Circuit Simulation: Analog Mixed-Signal Breakfast

Tuesday, June 5 **7:30am – 10:00am**

San Diego Marriott Hotel & Marina, Marina Salon D&E

Please join us for a breakfast panel event where Industry and academic experts will present their views on the future of parallel circuit simulation. Gain insight on how new hardware architectures, compilers, circuit simulation algorithms and device modeling will evolve to meet the challenges created by new process technologies, emerging markets and advanced integrated circuits. If you are involved in defining and driving your company's circuit simulation roadmap, you won't want to miss this special event.

Register Now! Please visit Synopsys Booth #5278 or Marriott Hotel, Marina Salon D&E. Walk-in registrations will be available, space permitting.

Brion Technologies Lithography and Design Forum

Tuesday, June 5 **11:30am – 2:00pm** **Rm: 23A**

Brion Technologies, an ASML company, invites you to attend a special luncheon event. During the meeting, you will learn how Brion's unique core competency in computational lithography is being used to change the way chips are designed. If you've ever worried about yield, performance or power, this event is a must-attend. We will have a special guest speaker to provide the user's view as well. Brion is unifying design and manufacturing in ways that were previously impossible. Join us for lunch and find out how.

Power Forward Initiative Lunch Panel

Tuesday, June 5 **11:30am – 1:00pm** **Rm: 30CDE**

Get an update on Power Forward Initiative progress since last year. Find out how CPF is already delivering advanced low-power design productivity.

VMM Methodology User Forum Luncheon

Tuesday, June 5 **11:30am – 2:00pm**

San Diego Marriott Hotel & Marina, Marina Salon F

Moderator: **Stuart Sutherland** • Sponsor: **Synopsys**

Who should attend: Engineers and managers looking to improve verification productivity with the VMM methodology for SystemVerilog. Transform your verification process with the VMM methodology! The VMM Methodology User Forum Luncheon features a panel of industry verification engineers and managers who will describe how the VMM methodology for SystemVerilog has transformed their verification processes for higher productivity, increased quality and more predictability. Following panelist presentations, the microphone will be opened for an audience-panel interactive discussion, moderated by an industry-recognized SystemVerilog expert. Register Now! At Synopsys Booth # 5278 or Marriott Hotel, Salon F. Walk-up registrations are welcome on a space-available basis.

IP Quality: How to Rate IP Using VSIA's QIP Metric Standard

Tuesday, June 5 **12:00pm – 1:30pm** **Rm: 32AB**

FREE lunch provided. Join VSIA for a Quality IP (QIP) Metric training session discussing the recently released QIP Metric version 3.0 that now includes vendor assessment, soft IP, hard IP and verification IP extensions. Mentor Graphics will provide an overview of the QIP Metric and Denali Software will provide a step-by-step walk through on how to complete the Metric for an IP core. The session will be wrapped up with a description from QIP Metric user LSI.

5th Annual ESL Symposium
The Missing Link: In Search of an ESL-to-RTL Design Flow

Tuesday, June 5 **12:00pm – 2:00pm** **Rm: 33ABC**

FREE lunch provided. ESL design enables more freedom for architectural exploration, early system design feedback, faster/more reliable system IP design and integration, early HW/SW development, increased productivity during hardware creation, and reduction in pre-silicon bugs. However, there is a gap between the ESL and RTL design flows that continues to cause problems for some designers. Industry experts will discuss what's needed to crease an ESL-to-RTL methodology, how the domains connect today and what's missing, how ESL design can leverage RTL tools and existing RTL IP, how an ESL-to-RTL flow would impact the IP industry, and share how they manage the domain gap and map technologies for crossing the ESL-to-RTL divide.

Additional Meetings

Accellera Breakfast and Panel Discussion

Wednesday, June 6 **7:30am – 9:30am** **Rm: 26AB**

Organizer: **Kevin Silver** - *Denali Software, Inc., Palo Alto, CA*

The lunch panel topic is: "IP, SystemVerilog's Final Frontier." The industry asked for SystemVerilog, and Accellera delivered. With support from leading EDA vendors, and the leadership of Accellera's member representatives in the design and verification community, SystemVerilog is now being successfully deployed across the industry. Early adopters are already reaping the rewards of using SystemVerilog for functional verification, but what about the application of SystemVerilog to design and integration of IP for SoC design? Panelists representing commercial IP providers, EDA vendors, and IP consumers will address real world benefits of SystemVerilog in the IP domain, and examine state-of-the art flows for IP design and integration, which is next frontier for SystemVerilog. This panel is sponsored by Denali Software, and is open to all DAC attendees.

Smooth Sailing or Rough Seas: Navigating the Power and OpenAccess Maelstrom - Synopsys Interoperability Breakfast

Wednesday, June 6 **7:30am – 9:30am**

San Diego Marriott Hotel & Marina, South Tower, 3rd Floor, Marina Ballroom D-E

Dr. Chi-Foon Chan, President and COO of Synopsys, invites you to explore the sometimes stormy world of interoperability. Don your foul weather gear, and hear the current conditions and latest forecasts for the important topics of low power and OpenAccess. The Tenzing Norgay Interoperability Achievement Award winner will be announced. Visit the open PCell showcase during breakfast to see the latest developments in custom analog IC design interoperability.

EDSFair Emerging Company Area - 44th DAC Breakfast Briefing

Wednesday, June 6 **7:30am – 10:30am** **Rm: 16B**

Don't miss your super express train to Japan market! Wanna start your business in Japan? The Emerging Company Area at Electronic Design and Solution (EDS) Fair 2007, a special section for emerging companies is offering low-cost and high-added-value opportunity to show your state-of-the-art technologies to SoC designers, managers and decision-makers from top electronics companies. For more information to find a trigger for your business promotion, please visit http://www.acteva.com/booking.cfm?bevaid=114221#bookingfor

Accellera Open Membership Meeting (Open to all DAC attendees)

Wednesday, June 6 **10:00am – 11:30am** **Rm: 27A**

Organizer: **Kevin Silver** - *Denali Software, Inc., Palo Alto, CA*

Accellera Technical Committees will provide standards' updates and honor the recipient of Accellera's Technical Excellence Award.

ACM TODAES Editorial Board

Wednesday, June 6 **11:00am – 2:00pm** **Rm: 25A**

SystemVerilog Design With Verification: Oil and Water Can Mix

Wednesday, June 6 **11:30am – 1:00pm** **Rm: 30CDE**

The traditional view is that logic designers design and verification engineers verify. However, the reality is that today's accelerated project schedules require bugs to be found as early as possible. Thus, certain aspects of verification are essential as part of the design process. This session describes Design with Verification, a Cadence environment in which logic designers can leverage formal analysis and more sophisticated testbenches at the block level, and how it links to full-chip verification. This session also discusses how SystemVerilog—as an integrated design and verification language that supports assertions, constraints, coverage, and more verifiable RTL—is enabling easy adoption of Design with Verification. Various experts in the field, as well as several designers dealing with these issues in real-world situations, will be featured in this exciting and interactive luncheon panel.

Additional Meetings

Interoperable PCell Library Lunch Workshop

Wednesday, June 6 12:00 pm – 1:30 pm Rm: 32AB

Complimentary Hot Buffet lunch (served 12:00-12:30pm)

Synopsys, Ciranova, AWR, Silicon Canvas, and Silicon Navigator have created an industry initiative to promote interoperable PCell libraries (IPLs) on OpenAccess, and released a proof-of-concept interoperable PCell library as open-source. This library has been verified to work in tools from all participants. For the first time in semiconductor industry history, an integrated circuit designer will be able to use the same PCell libraries in tools from all five vendors, plus with OpenAccess-based tools from other vendors or universities, or developed in-house.

At this workshop, you will learn how the library was created, explore how foundries and semiconductor vendors can develop their own IPLs, and learn the next steps for the IPL initiative. All interested companies and EDA vendors are invited to participate. Registration is free on a first-come, first-served basis at http://www.iplnow.com Seating may not be available at the door.

Solving the SoC Memory Puzzle

Wednesday, June 6 12:00 pm – 2:00 pm Rm: 29CD

FREE lunch provided

SoCs have evolved from simple computers-on-chips to complex heterogeneous multiprocessing systems and the demand for on-chip and external memory has skyrocketed. More local storage and on-chip shared memory, greater bandwidth to external memory, and special requirements like data security have all become problems. Silicon IP and EDA tools are now struggling to catch up with these design requirements. Join moderator Ron Wilson and an expert panel over lunch as they examine IP and tools for generating on-chip memory structures, IP for interfaces and controllers to external memory, and system-level tools for crafting memory system architectures.

Cadence-IBM Seminar: Optimizing the Path into ASIC for First-Time-Right Silicon

Thursday, June 7 7:30 am – 9:00 am Rm: 30CDE

Learn the benefits of developing 65nm designs with low-power techniques.

2007 EDA Marketing Forum (formerly Hacks & Flacks)

Thursday, June 7 8:00 am Rm: 9

Publications that the EDA community reads are undergoing radical changes. They have gone from "print only" to "print and Web" and now to many instances of "Web only." New Web vehicles and tools are creating different ways of pushing and pulling news content, and producing thinner print publications. Digital news is now portable via pagers, cellphones and PDAs. The role of the press release has changed with the use of SEO (search engine optimization), podcasting, and RSS (Really Simple Syndication). How are companies and editors impacted by these changes? Are editors no longer acting as the primary gatekeepers and disseminators of information or are they still powerful as opinion leaders and spokespeople? Have new technologies changed the way publications are directing editorial content and behavior?

Join us for BREAKFAST to take part in this lively discussion among editors, marketing and PR professionals, publishers, and advertising executives.

DAC Solutions Workshops

Thursday, June 7 11:30 am – 1:00 pm Rm: 27B

"Get to grips with the latest know-how on ESL and verification methodology at the DAC Solutions Workshops. Now in its 3rd series at DAC, these fast-paced 2 hour technical seminars have been put together by Doulos in co-operation with leading vendors especially for DAC 07.

This year's lunch-time series are presented in conjunction with Cadence, CoWare, Mentor Graphics, Synopsys, The MathWorks. Check out the full series details at http://www.doulos.com.

Last minute registrations available at the Doulos booth #2863. Lunch provided.

Doulos is the global leader for the development and delivery of world-class training solutions for SoC, FPGA and ASIC design and verification methodology."

45th DAC Call for Papers

DAC is the premier conference devoted to Design Automation (DA) and the application of DA tools in designing electronic systems. Four types of submissions are invited: regular papers, special topic sessions, panels, and tutorials. Submissions must be made electronically at www.dac.com. **Panel and tutorial suggestions, and special session submissions are due no later than 5:00 pm MST, November 1, 2007; Regular Papers are due no later than 5:00 pm MST, November 19, 2007.**

Topics of Interest

DAC 2008 is seeking papers that deal with design tools, design methods, design techniques, and embedded design in a number of categories described below.

Design Tools papers describe contributions to the research and development of design tools and their supporting algorithms.

Design Methods and case studies papers describe innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art design projects.

Design Papers describe the use of design tools and methods from the perspective of a specific design project. They include a brief description of the design and discussion of: methodology, flow, innovative use of tools, the limits of current tools, and what new tool capabilities are required for future designs.

Embedded Systems are characterized by mixed hardware and software components with limited resources. Increases in software content introduce new system design issues. Embedded design papers describe tools, methods, and case studies for applications with specific embedded system content.

The theme topic for DAC 2008 is Wireless, and papers that specifically refer to the theme will be highlighted at the conference.

All Submissions must be made electronically at the DAC website **www.dac.com** *Regular Paper Submissions Are Due Before 5 pm MST, November 19, 2007*

Regular paper submissions MUST (1) be in PDF format only, (2) contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission, (3) be no more than 6 pages (including the abstract, figures, tables, and references), double columned, 9pt or 10pt font, and (4) MUST NOT include name(s) or affiliation(s) of the author(s) anywhere on the manuscript or abstract, and any references to the author(s)'s own previous work or affiliations in the bibliographic citations must be in the third person. Format templates are available on the DAC web site for your convenience, but are not required. Submissions not adhering to these rules, or those previously published or simultaneously under review by another conference, will be rejected. DAC will work cooperatively with other conferences and symposia in the field to check for double submissions. Additional submission guidelines are available on the DAC website (after September 3, 2007). All regular papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage. Authors of accepted papers must sign a copyright release form for their paper. Acceptance notices will be available by logging in on the DAC website after February 25, 2008. Complete author kits will be sent via email by March 7, 2008.

Special session submissions must include descriptions of suggested papers and speakers, and the importance of the special session to the DAC audience. DAC reserves the right to restructure all special sessions. **Special Session Submissions Are Due Before 5 pm MST, Nov. 1, 2007**

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panel and tutorial proposals. **Panel and Tutorial Submissions Are Due Before 5 pm MST, Nov. 1, 2007**

Students are invited to submit descriptions of original electronic designs, either circuit level or system level. **Student Design Contest paper submissions** must (1) be in PDF format only, (2) contain the title of the project, (3) contain an abstract of approximately 60 words, (4) a complete description of the project, and (5) be no more than 6 pages (including the abstract, maximum of 10 figures/tables and references), double columned, 9pt or 10pt font. The submission should clarify the originality, distinguishing features, and measured performance of the design. Three categories of designs - operational, system and conceptual - are eligible for awards. For operational designs, proof-of-implementation is required, while for conceptual designs, complete simulation and test plan is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2006. Submitted designs should not have received awards in other contests. Selected designs will be presented at the conference (and at ISSCC in February 2008). Additional contest rules are available on the DAC web site. **Student Design Contest Submissions Are Due Before 5 pm MST, Dec. 5, 2007**

45th DAC Call for Papers

Submitters are required to specify a category from the 18 listed below. Categories:

1. System-Level Design and Co-Design
1.1 System specification, modeling, simulation, and performance analysis
1.2 Scheduling, HW-SW partitioning
1.3 IP and platform-based design, IP protection
1.4 System-on-Chip (SoC) and Multi-processor SoC (MPSoC)
1.5 Application-specific processor design tools

2. System-Level Communication and Networks on Chip
2.1 Modeling and performance analysis
2.2 Communications-based design
2.3 Architectural synthesis, mapping, routing, scheduling
2.4 Optimization for energy, fault-tolerance, reliability
2.5 Interfacing and software issues
2.6 NoC Design methodologies and CAD flows, case studies and prototyping

3. Embedded HW Design and Applications
3.1 Case studies of embedded system design
3.2 Flows and methods for specific applications and design domains

4. Embedded SW Tools and Design
4.1 Retargetable compilation
4.2 Memory/cache optimization
4.3 Real-time single- and multi-processor scheduling, linking, loading
4.4 Real-time operating system

5. Power Analysis and Low-Power Design
5.1 System level power design and thermal management
5.2 Embedded low-power approaches: partitioning, scheduling, and resource management
5.3 High-level power estimation and optimization
5.4 Gate-level power analysis and optimization
5.5 Device, circuit techniques for low-power design

6. Verification
6.1 Functional, transaction-level, RTL, and gate-level modeling and verification of hardware design
6.2 Dynamic simulation, equivalence checking, formal (and semi-formal) verification model and property checking
6.3 Emulation and hardware simulators or accelerator engines
6.4 Modeling languages and related formalisms, verification plan development and implementation
6.5 Assertion-based verification, coverage-analysis, constrained-random testbench generation

7. High-Level Synthesis
7.1 High-level, behavioral, algorithmic, and architectural synthesis, "C" to gates tools and methods
7.2 HW-SW interface synthesis, communication and network synthesis
7.3 Synthesis of digital circuits above the RTL level
7.4 Resource scheduling, allocation, and synthesis

8. Beyond Die-Integration and Package/Hybrid/Board Design
8.1 Chip-package-board codesign
8.2 System-in-Package, 3D design, stacked devices
8.3 Beyond-the-die communication, high-speed I/O, optical communication
8.4 Analysis and optimization (signal integrity, physical layout, simulation) beyond the die

9. Logic Synthesis and Circuit Optimization
9.1 Combinational, sequential, and asynchronous logic synthesis
9.2 Library mapping, cell-based design and optimization
9.3 Transistor and gate sizing and resynthesis
9.4 Interactions between logic design and layout or physical synthesis

10. Circuit Simulation and Interconnect Analysis
10.1 Electrical-level circuit simulation
10.2 Model-order reduction methods for linear systems
10.3 Interconnect and substrate modeling and extraction
10.4 High-frequency and electromagnetic simulation of circuits
10.5 Thermal and electrothermal simulation

11. Timing Analysis and Design for Manufacturability
11.1 Design for yield, defect tolerance, cost issues, and impacts of DFM
11.2 Process technology development, characterization, and modeling
11.3 Deterministic static timing analysis and verification
11.4 Statistical performance analysis and optimization
11.5 Design for resilience under manufacturing variations

12. Physical Design and Manufacturability
12.1 Physical floorplanning, partitioning, placement
12.2 Buffer insertion, routing, interconnect planning
12.3 Physical verification and design rule checking
12.4 Automated synthesis of clock networks
12.5 Reticle enhancement, lithography-related design optimizations

13. Signal Integrity and Design Reliability
13.1 Signal integrity, capacitive and inductive crosstalk
13.2 Reliability modeling and analysis
13.3 Novel clocking and power delivery schemes
13.4 Power grid robustness analysis and optimization
13.5 Soft-errors and single-event upsets (SEUs)
13.6 Thermal Reliability

14. Analog/Mixed-Signal and RF
14.1 Analog, mixed-signal, and RF design methodologies
14.2 Automated synthesis and macromodeling
14.3 Analog, mixed-signal and RF simulation and optimization

15. FPGA Design Tools and Applications
15.1 Rapid prototyping
15.2 Logical synthesis and physical design techniques for FPGAs
15.3 Configurable and reconfigurable computing

16. Testing
16.1 Test quality/reliability, current-based test, delay test, low power test
16.2 Digital fault modeling, automatic test generation, fault simulation
16.3 Digital design-for-test, test data compression, built-in self test
16.4 Memory test and repair, FPGA testing
16.5 Fault tolerance and on-line testing
16.6 Analog/mixed-signal/RF testing, System-in-Package (SiP) testing
16.7 Board- and system-level test, System-on-Chip (SoC) testing
16.8 Silicon debug, diagnosis, post-silicon design validation

17. New and Emerging Design Technologies, including but not restricted to
17.1 MEMS, sensors, actuators, imaging devices
17.2 Nano-technologies, nano-wires, nano-tubes
17.3 Quantum computing
17.4 Biologically based or biologically inspired systems
17.5 New transistor structures and devices, new or radical process technologies

18. Special Theme Topic: Wireless
18.1 Emerging technologies for the design, verification, test and implementation of wireless systems
18.2 Power-aware and energy-efficient wireless protocols, algorithms and associated design techniques and methodologies
18.3 Embedded software design challenges for wireless applications and its impact on ESL design solutions
18.4 Promising analog and mixed signal design techniques for wireless systems including but not limited to advanced Antenna and RF design solutions

DAC Program Committee

Technical Program Co-Chair, Design Methods
Leon Stok
IBM Corp.
Hopewell Junction, NY

Technical Program Co-Chair, Design Tools
Sachin Sapatnekar
Univ. of Minnesota
Minneapolis, MN

Brian Bailey
Consultant
Oregon City, OR

Kaustav Banerjee
Univ. of California
Santa Barbara, CA

Kia Bazargan
Univ. of Minnesota
Minneapolis, MN

John Berrie
Zuken
Almondsbury, UK

Clive D. Bittlestone
Texas Instruments Inc.
Dallas, TX

Dennis Brophy
Mentor Graphics
Wilsonville, OR

Yu Cao
Arizona State Univ.
Tempe, AZ

Krishnendu Chakrabarty
Duke Univ.
Durham, NC

Yao-Wen Chang
National Taiwan Univ.
Taipei, Taiwan

Shih-Chieh Chang
Tsinghua Univ.
Hsinchu, Taiwan

Karam S. Chatha
Arizona State Univ.
Tempe, AZ

Howard Chen
IBM Corp.
Yorktown Heights, NY

Wu-Tung Cheng
Mentor Graphics Corp.
Wilsonville, OR

Eli Chiprout
Intel Corp.
Hillsboro, OR

Jordi Cortadella
Universitat Politecnica Catalunya
Barcelona, Spain

Anirudh Devgan
Magma Design Automation, Inc.
Austin, TX

Rainer Doemer
Univ. of California
Irvine, CA

Adam Donlin
Xilinx, Inc.
San Jose, CA

Stephen Edwards
Columbia Univ.
New York, NY

Petru Eles
Linkoping Univ.
Linkoping, Sweden

Peter Feldmann
IBM Corp.
Yorktown Heights, NY

Alberto Ferrari
Parades E.E.I.G.
Rome, Italy

Harry Foster
Mentor Graphics Corp.
Addison, TX

Jon Friedman
The Mathworks, Inc.
Natick, MA

Patrick Girard
LIRMM Univ.
Montpellier, France

Helmut Graeb
Technical Univ. of Munich
Munich, Germany

Patrick Groeneveld
Magma Design Automation, Inc.
Santa Clara, CA

Nagib Hakim
Intel Corp.
Santa Clara, CA

Bill Halpin
Synplicity, Inc.
Sunnyvale, CA

Masanori Hashimoto
Osaka Univ.
Suita, Japan

Kazumi Hatayama
STARC
Yokohama, Japan

Michael Heimlich
Applied Wave Research, Inc.
Pelham, NH

Fook-Luen Heng
IBM Corp.
Yorktown Heights, NY

Joerg Henkel
Univ. of Karlsruhe
Karlsruhe, Germany

Jiang Hu
Texas A&M Univ.
College Station, TX

Alan Hu
Univ. of British Columbia
Vancouver, BC, Canada

Yehea Ismail
Northwestern Univ.
Evanston, IL

Niraj Jha
Princeton Univ.
Princeton, NJ

Ryan Kastner
Univ. of California
Santa Barbara, CA

Nam Sung Kim
Intel Corp.
Hillsboro, OR

Wido Kruijtzer
NXP Semiconductors
Eindhoven, Netherlands

Luciano Lavagno
Politecnico Di Torino
Torino, Italy

Jinfeng Liu
Synopsys, Inc.
Mountain View, CA

Patrick Lysaght
Xilinx, Inc.
San Jose, CA

Jean Christophe Madre
Synopsys, Inc.
Montbonnot, France

DAC Program Committee

Rabi Mahapatra
Texas A&M Univ.
College Station, TX

Radu Marculescu
Carnegie Mellon Univ.
Pittsburgh, PA

Diana Marculescu
Carnegie Mellon Univ.
Pittsburgh, PA

Malgorzata Marek-Sadowska
Univ. of California
Santa Barbara, CA

Erich Marschner
Cadence Design Systems, Inc.
Ellicott City, MD

Peter Marwedel
Univ. of Dortmund
Dortmund, Germany

Anmol Mathur
Calypto Design Systems, Inc.
Santa Clara, CA

Raj Mitra
Texas Instruments Inc.
Bangalore, India

Vincent Mooney
Georgia Institute of Tech.
Atlanta, GA

Rajeev Murgai
Fujitsu Labs of America, Inc.
Sunnyvale, CA

Farid Najm
Univ. of Toronto
Toronto, ON, Canada

Ravi Nanavati
Bluespec, Inc.
Waltham, MA

Sani Nassif
IBM Corp.
Austin, TX

Sule Ozev
Duke Univ.
Durham, NC

Davide Pandini
STMicroelectronics
Agrate Brianza, Italy

Barry Pangrle
Atrenta, Inc.
San Jose, CA

Li-Shiuan Peh
Princeton Univ.
Princeton, NJ

Dusan Petranovic
Mentor Graphics Corp.
San Jose, CA

Joel Phillips
Cadence Berkeley Labs
Berkeley, CA

Juan R. Pimentel
Kettering Univ.
Flint, MI

Ruchir Puri
IBM Corp.
Yorktown Heights, NY

Antal Rajnak
Mentor Graphics Corp.
Vienna, Austria

Jaijeet Roychowdhury
Univ. of Minnesota
Minneapolis, MN

Rob Rutenbar
Carnegie Mellon Univ.
Pittsburgh, PA

Louis Scheffer
Cadence Design Systems, Inc.
San Jose, CA

Sandeep Shukla
Virginia Tech Univ.
Blacksburg, VA

Tajana Simunic Rosing
Univ. of California
San Diego, CA

Eli Singerman
Intel Corp.
Haifa, Israel

Nick Smith
Mentor Graphics Corp.
Newbury, UK

Fabio Somenzi
Univ. of Colorado
Boulder, CO

Ankur Srivastava
Univ. of Maryland
College Park, MD

Haihua Su
IBM Corp.
Austin, TX

Madhavan Swaminathan
Georgia Institute of Tech.
Atlanta, GA

Andres Takach
Mentor Graphics Corp.
Wilsonville, OR

Steven Teig
Tabula Inc.
Santa Clara, CA

Geert Van Der Plas
IMEC
Leuven, Belgium

Janet Wang
Univ. of Arizona
Tucson, AZ

Hai Zhou
Northwestern Univ.
Evanston, IL

Vladimir Zolotov
IBM Corp.
Yorktown Heights, NY

Mark Zwolinski
Univ. of Southampton
Southampton, UK

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Andrew B. Kahng
Panel Chair
Univ. of California
La Jolla, CA

Francine M. Bacchini
Francine Bacchini, Inc.
San Jose, CA

Dennis Brophy
Mentor Graphics Corp.
Wilsonville, OR

Rich Goldman
Synopsys, Inc.
Mountain View, CA

Haruhisa Kashiwagi
STARC
Yokohama, Japan

Shishpal Rawat
Intel Corp.
Folsom, CA

Rob A. Rutenbar
Carnegie Mellon Univ.
Pittsburgh, PA

Lori Kate Smith
ARM Ltd.
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Limor Fix
Stategy Committee Chair
Intel Research
Pittsburgh, PA

Dennis Brophy
Mentor Graphics Corp.
Wilsonville, OR

Anne Cirkel
Mentor Graphics Corp.
Wilsonville, OR

Craig Cochran
Jasper Design Automation, Inc.
Mountain View, CA

Jason Cong
Univ. of California
Los Angeles, CA

Nitin Deo
Clear Shape Technologies, Inc.
Santa Clara, CA

Georges Gielen
Katholieke University Leuven
Leuven, Belgium

Kim Johnsen
Mountain View, CA

Robert Jones
Intel Corp.
Hillsboro, OR

Andrew B. Kahng
Univ. of California
San Diego, CA

Steven P. Levitan
Univ. of Pittsburgh
Pittsburgh, PA

Diana Marculescu
Carnegie Mellon Univ.
Pittsburgh, PA

Gabe Moretti
Gabe on EDA
Venice, FL

Mindy Palmer
CoWare, Inc.
San Jose, CA

Pam Parrish
San Jose, CA

Kaushik Roy
Purdue Univ.
West Lafayette, IN

Sachin Sapatnekar
Univ. of Minnesota
Minneapolis, MN

Ellen Sentovich
Cadence Berkeley Labs.
Berkeley, CA

Gary Smith
Gary Smith EDA
Santa Clara, CA

Leon Stok
IBM Corp.
Hopewell Junction, NY

Steve Trimberger
Xilinx, Inc.
San Jose, CA

Nancy Weiss
Synplicity, Inc.
Sunnyvale, CA

Yaron Wolfsthal
IBM Corp.
Haifa, Israel

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Boulder, CO

Yervant Zorian
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Fremont, CA

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Tutorial Chair
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Mountain View, CA

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Carnegie Mellon Univ.
Pittsburgh, PA

Stan Liao
Stretch, Inc.
Sunnyvale, CA

Anand Raghunathan
NEC-Labs America, Inc.
Princeton, NJ

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William J. Bowhill
DAC/ISSCC SDC Co-Chair
Intel Corp.
Hudson, MA

Byunghoo Jung
DAC/ISSCC SDC Co-Chair
Purdue Univ.
West Lafayette, IN

Alan Mantooth
DAC/ISSCC SDC Co-Chair
Univ. of Arkansas
Fayetteville, AR

John Edmondson
NVIDIA Corp.
Bedford, MA

Claude Gauthier
Advanced Micro Devices, Inc.
Santa Clara, CA

Jim Goodman
Advanced Micro Devices, Inc.
Ottawa, Canada

Francis Jeung
ASTRI-WMT
Shatin, Hong Kong

William Kuhn
Kansas State Univ.
Manhattan, KS

Chidamber Kulkarni
Xilinx, Inc.
San Jose, CA

Kumar Lakshmikumar
Conexant Systems, Inc.
Reb Bank, NJ

Bang-Won Lee
ATlab Inc.
KyungGi-DO, South Korea

Dan Leibholz
Advanced Micro Devices, Inc.
Boxborough, MA

John W. Lockwood
Washington Univ., St. Louis
St. Louis, MO

Liam Madden
Advanced Micro Devices, Inc.
Sunnyvale, CA

Saraju P. Mohanty
Univ. of N. Texas
Denton, TX

Mehmet Soyuer
IBM Corp.
Yorktown Heights NY

Bud Taddiken
Microtune, Inc.
Plano, TX

Marc Tiebout
Infineon Technologies AG
Villach, Austria

Alice Wang
Texas Instruments Inc.
Dallas, TX

Peter R. Wilson
Univ. of Southampton
Southhampton, UK

Hoi-Jun Yoo
KAIST
Daejeon, South Korea

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Exhibitor Liaison Chair
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Fremont, CA

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Mentor Graphics Corp.
Oro Valley, AZ

Donna Castillo
Cadence Design Systems, Inc.
San Jose, CA

Anne Cirkel
Mentor Graphics Corp.
Wilsonville, OR

Michelle Clancy
Cayenne Communication
Washington, NC

Craig Cochran
Jasper Design Automation, Inc.
Mountain View, CA

Nanette V. Collins
Public Relations Consultant
Boston, MA

Nitin Deo
Clear Shape Technologies, Inc.
Santa Clara, CA

George Harper
Bluespec, Inc.
Waltham, MA

Steven P. Levitan
Univ. of Pittsburgh
Pittsburgh, PA

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Gabe on EDA
Venice, FL

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CoWare, Inc.
San Jose, CA

Dave Reed
Blaze DFM, Inc.
Sunnyvale, CA

Nancy Weiss
Synplicity, Inc.
Sunnyvale, CA

Lee Wood
MP Associates, Inc.
Boulder, CO