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Important Information At-A-Glance

Exhibit Hours

Monday, July 24 .....9:00 am to 6:00 pm
Tuesday, July 25 .....9:00 am to 6:00 pm
Wednesday, July 26 .....9:00 am to 6:00 pm
Thursday, July 27 .....9:00 am to 1:00 pm

Registration Hours

The registration desk is located in the North Lobby of The Moscone Center, and is open during the following hours:

Sunday, July 23.....8:30 am to 6:00 pm
Monday, July 24 .....7:00 am to 6:00 pm
Tuesday, July 25.....7:00 am to 6:00 pm
Wednesday, July 26.....7:00 am to 6:00 pm
Thursday, July 27 .....7:00 am to 6:00 pm

Tutorial Registration **Friday, July 28, 7:00 am to 6:00 pm**

Tutorial registration is located in the Esplanade Lobby in the South Hall.

DACnet-2006

DACnet stations are located in the Esplanade Lobby in the South Hall, and in the Concourse Hallway between the North and South Halls.

The 43rd Design Automation Conference Week in Review

Sunday, July 23	Monday, July 24	Tuesday, July 25	Wednesday, July 26	Thursday, July 27	Friday, July 28
• UML for SoC Design Workshop	• FREE Monday Exhibits • Keynote Address • Full-Day Tutorials • Pavilion Panels • Hands-on Tutorials • Workshops • Exhibit Floor Happy Hour *(5:00 pm - 6:00 pm)*	• General Session • Keynote Address • Technical Sessions • Management Day • Pavilion Panels • Hands-on Tutorial • Exhibits • SIGDA Ph.D. Forum	• Technical Sessions • MEGa Theme • Pavilion Panels • Hands-on Tutorials • Exhibits • DAC Party *(AT&T Ballpark)*	• Keynote Address • Best Paper Awards • Technical Sessions • Pavilion Panels • Hands-on Tutorials • Exhibits	• Full-Day Tutorials

Technical Program Highlights

This year DAC is celebrating its 43rd year with a technical program that includes nearly 200 papers, panels, tutorials, and keynote presentations covering a wide range of design issues. The program covers sessions in eleven topic areas: Business, System Level and Embedded, MEGa, Low Power and Power, Analog and Circuit Interconnect, Reliability and DFM, Verification and Test, Synthesis and FPGA, Physical Design, Beyond the Die, and New and Emerging Technologies.

In each of these areas the sessions will cover aspects of both design methodology and design tools. The themed sessions for the 43rd DAC focus on multimedia, entertainment and games. The theme is woven into the keynote addresses, technical sessions and panels, and pavilion panels. Management Day on Tuesday, July 25, includes sessions and functions discussing topics at the intersection of technology and business for design management.

Hands-on Tutorials - details on pgs. 50 - 53

Hands-on Tutorials are three-hour tutorials presented by exhibitors to demonstrate their solutions to issues in Low Power Design.

Management Day - details on pgs. 5, 7, 19, 20, 23, 25

DAC has dedicated a full day of keynotes, panels and special presentations by experts on business topics that affect technology decisions and directions. Management Day includes:

General Session Keynote Address
Session 1: PANEL: How Will the Fabless Model Survive
EDA Business Forum Luncheon
Session 100: Decision-Making for Complex SoCs in Consumer Electronic Products
Session 150: Tradeoffs and Choices for Emerging SoCs in High-End Applications

MEGa (Multimedia, Entertainment, and Games) - details on pg. 5

The themed sessions for the 43rd DAC focus on multimedia, entertainment and games. The theme is woven into the keynote addresses, technical sessions and panels, and pavilion panels. These sessions will highlight CAD challenges for multimedia designs, and look at next generation MEGa designs and power constraints of consumer devices.

Tutorials - details on pgs. 17, 42 - 45

Monday, July 24 • 9:00 am - 5:00 pm

1) Practical Aspects of Coping with Variability: An Electrical View
2) ESL Design Methodology Using SystemC

Friday, July 28 • 9:00 am - 5:00 pm

3) Real DFM Solutions, Tools Methodologies and Successes
4) Surviving and Thriving in the World of Chip and Package Co-Design
5) SystemVerilog: Language Tutorial and Industrial Verification Experience
6) Tools for Hybrid Embedded Systems: Modeling, Verification, and Design
7) From Basic to Advanced Techniques for Silicon Debug and Diagnosis

MONDAY KEYNOTE - details on pg. 6

Monday, July 24 - 2:00 pm Gateway Ballroom

Joe Costello - *Chairman of the Board, Orb Networks, Inc.*

GENERAL SESSION AND KEYNOTE - details on pgs. 7, 19

Tuesday, July 25 - 8:30 am Gateway Ballroom

Hans Stork - *Senior Vice President and Chief Technology Officer, Director of Silicon Technology Department, Texas Instruments Inc.*

THURSDAY KEYNOTE - details on pg. 8

Thursday, July 27 - 12:45 pm Gateway Ballroom

Alessandro Cremonesi - *Strategy and System Technology Group Vice-President and Advanced System Technology General Manager, STMicroelectronics*

Exhibitor Highlights

Exhibit Floor

Monday – Wednesday, July 24-26, 9:00 am – 6:00 pm
Thursday, July 27, 9:00 am – 1:00 pm
The 43rd DAC Exhibition is located in the North (Booths 3000-4367) and in the South (Booths 101-2323) Halls of The Moscone Center

The DAC Exhibit floor is bursting with over 240 vendors offering products for all phases of the electronic design process including EDA tools, IP cores, embedded system and system-level tools, silicon vendors, and a host of new design-for-manufacturing companies. The DAC show floor features its unique exhibit booth and private suite combination, which gives you the freedom to deeply explore the products on the show floor and find a solution that is right for your design. Visit the DAC exhibition and find out how you can improve performance and shorten the time-to-market on your next product..

Children under the age of 14 will NOT be allowed in the exhibit hall.

Exhibits-Only Registration

- Free Monday Exhibits-Only Passes - Attend the exhibition free of charge Monday, July 24.
- $60 Exhibits-Only registration will allow you to attend exhibits Monday through Thursday.

DAC Pavilion

DAC has an exciting line-up of panels and presentations in the DAC Pavilion, booth 2228 on the exhibit floor. The DAC Pavilion sessions are open to all attendees at no charge and feature 18 provocative technical, business and strategy discussions. See pages 9-12 for details.

New Exhibitors at DAC

DAC has always been the best place to see the industry's newest companies, and this year is no exception. With over 50 new exhibitors, DAC is the place to be to find out what the hot startups are up to. Among the companies participating in DAC for the first time are:

Advanced Circuit Engineers, LLC
Algotronix Ltd.
Altos Design Automation
ArchPro Design Automation Inc.
Barth Electronics, Inc.
Catalytic Inc.
CebaTech, Inc.
Certess Inc.
Certicom Corp.
Coupling Wave Solutions
Fenix Design Automation B.V.
Formal Sciences Inc.
Fortelink Inc.
Helic S.A.
Imperas, Inc.
INFINISCALE
Ingot Systems
Innovative Silicon Inc.
Institution of Engineering and Technology (The)
Invarium
Liga Systems, Inc.
Lizotech, Inc.
Lynguent, Inc.
Magwel NV
Malico Inc.
MunEDA-ChipMD
National Instruments Corp.
NSCore, Inc.
Oasis Tooling, Inc.
OneSpin Solutions GmbH
Perfectus Technology Inc.
Polyscale Computing Inc.
Rio Design Automation Inc.
Semifore, Inc.
Silistix, Inc.
SimPlus Verification
Solido Design Automation Inc.
Space Codesign
SynCira Corp.
Takumi Technology Corp.
TurboTools Corp.
Tuscany Design Automation, Inc.
UniquelCs, LLC
Uniquify
Western Scientific, Inc.

Management Day/MEGa Sessions

Management Day - Tuesday, July 25

DAC's Management Day is where the technology and the business of IC and system design intersect. This full day of sessions is designed for managers and executives of semiconductor, communications and consumer electronics companies. Participants meet, interact with, and learn from peers who are facing the issues of how to make the right business and technology decisions in the dynamic world of electronic design. The Management Day $75 registration fee includes the 11th Annual EDA Business Forum luncheon, and the wrap-up cocktail party.
Minimum Conference Registration required: Exhibits Only

Management Day Sessions include:

General Session Keynote Address - Gateway Ballroom • 8:30 am - 10:15 am

Structuring Process and Design for Future Mobile Communication Devices

Hans Stork - Senior Vice President and Chief Technology Officer, Texas Instruments Inc.

Session 1: PANEL: - Rm: 306/308 • 10:30 am - 12:00 pm

How Will the Fabless Model Survive?
Chair: Don Clark - *Wall Street Journal*

EDA Business Forum Luncheon - Rm: 124/125 - 12:00 pm - 1:00 pm

Management Day Session 100 - Rm: 301 - 2:00 pm - 4:00 pm
Decision-Making for Complex SoCs in Consumer Electronic Products
Chair: Ron Wilson - *EDN*

- 100.1 ***Qualcomm: Lessons Learned at the 65nm Node***
- 100.2 ***Low Power Challenges in Wireless ICs***
- 100.3 ***Consumer Electronics Development Tradeoffs in the High-Tech Startup***
- 100.4 ***Architecture Planning Criteria for a System-in-a-Package Portable Multimedia Platform***

Management Day Session 150 - Rm: 301 - 4:30 pm - 6:30 pm
Tradeoffs and Choices for Emerging SoCs in High-End Applications
Chair: Nic Mokhoff - *EE Times, Manhasset, NY*

- 150.1 ***Assessing Process Nodes and IP for SoC Development***
- 150.2 ***Open-IP: How Your Selection of IP Drives Your ASIC Success***
- 150.3 ***Yield, Manufacturability and Test: The Criteria to Judge the Right Design Investment***

Cocktail Reception - Rm: 302 - 6:00 pm - 6:30 pm

MEGa Sessions: Multimedia, Entertainment, and Games

For 2006, the 43rd DAC is presenting MEGa Sessions: the design challenges and design technology requirements for creating advanced multimedia, entertainment, and game (MEGa) products. The MEGa theme is woven into all three keynote addresses and is a full-track of sessions on Wednesday, July 26th. The presentations include a special session highlighting selected papers from ISSCC in the multimedia area, with presentations from Renesas/DoCoMo, MediaTek, National Chiao-Tung University, and Samsung, and continues with two complementary events: an invited session on CAD challenges for leading-edge multimedia designs, followed by a panel on design challenges for next generation multimedia, entertainment, and game platforms. These two sessions include experts from STMicroelectronics, IBM, nVidia, PixelWorks, Qualcomm, and Intel. The sessions conclude with four papers on power-constrained design for multimedia.

Complementing the MEGa sessions will be Pavilion Panels, taking place throughout the week on the exhibit floor. These include presentations on Inside the iPod, technology requirements for 3D graphics in feature films, and a discussion on the Xbox 360 and getting chips into high-volume products.

All full-conference attendees are invited to attend the MEGa technical sessions, and all registrants are invited to attend the DAC Pavilion sessions in Booth 2228 on the exhibit floor.

Monday Keynote

2:00 pm • Gateway Ballroom

iPod or Iridium - Which One Are You Going To Be?

Joe Costello
Chairman of the Board, Orb Networks, Inc.

Abstract: An incredible amount of time, resources and investment is being made by EDA, chip, and electronics companies to win in the exploding multi-media, gaming, and entertainment applications markets. With the 2006 DAC conference doing a much-needed "deep dive" into how the semiconductor industry meets technical challenges, Joe Costello, Chairman of Orb Networks, Inc., will turn the spotlight away from technology and onto today's macro consumer trends.

During this session, Joe challenges participants with this fundamental question: are you going in the right direction? As you bend your minds with the complexity of implementing modern day systems and chips, are you racing toward the right finish line? What are consumers really looking for? What will convergence really lead to and are you positioned to take advantage of all it will bring our industry and our world? Join Joe as he reveals lessons learned and offers a simple view of the future of electronics.

Biography: Joe Costello is chairman, co-founder, and an investor in Orb Networks, Inc. He is highly regarded for his business acumen and bold moves in the high-tech industry. In 1997, *Chief Executive Magazine* named Costello the top performing CEO of all publicly traded companies in North America. He also made *Upside Magazine's* 1997 "Elite 100" list of the top executives leading the digital revolution. He serves as CEO and chairman of think3, a developer of computer-aided design software used throughout the product development process. He is also chairman of other privately-held companies that include Readio, Abazab and SpeakESL. In addition, Costello is on the board of Mercury Interactive, a publicly-held company. Prior to think3, Costello played a pivotal role as president and CEO at Cadence Design Systems, Inc. for more than a decade. Under his leadership, Cadence became the world's leading supplier of electronic EDA software and services, and one of the ten highest-grossing software vendors in the world. Costello holds a bachelor of science degree in mathematics and physics from Harvey Mudd College, a master of science degree in physics from Yale University, and a master of science degree in physics from the University of California, Berkeley.

8:30 am • Gateway Ballroom

Tuesday Keynote

Structuring Process and Design for Future Mobile Communication Devices

Hans Stork
Senior Vice President and Chief Technology Officer, Director of Silicon Technology Department, Texas Instruments Inc.

Abstract: The density and speed of sub-50nm CMOS technology enables the design of multi-functional SoCs for highly integrated, mobile communication devices. At the same time, process variations, power issues, and complexity of scope are challenging even the most advanced simulation capabilities. The growing design complexity is addressed by rapidly improving modeling of systematic manufacturing variations and design sensitivities. Physical design is becoming more structured to allow for process optimized design rules and efficient automation. While challenges remain in the scaling and optimization of analog and I/O functions, highly integrated, mobile communication devices are a major driving force for continued economies of scaling.

Biography: With a doctorate from Stanford University, Dr. Stork joined TI in 2001 from Hewlett-Packard, where he served as Director of the Internet Systems and Storage Lab at HP Laboratories, and earlier as the Director of the ULSI Research Lab. He began his professional career at IBM's T.J. Watson Research Center, where he researched advanced bipolar technology and circuits, and later SiGe (silicon germanium) technology, finally assuming responsibility for the Exploratory Device and Technology programs at IBM Research.

Dr. Stork has written or co-authored approximately 90 papers and holds five patents. He was elected IEEE Fellow in 1994 for his contributions to SiGe devices and technology. He is a fellow member of the IEEE Electron Devices Society, where he has served on and chaired a number of committees. Dr. Stork joined the Sematech board of directors in 2002 after several years service on the organization's Executive Technical Advisory Board, has been a board member of the Semiconductor Research Corporation since 1999, and serves on the Semiconductor Industry Association's (SIA) Technology Strategy Committee. Additionally, he served as a technical advisor to government efforts on high-performance computing benchmarks and the national security issues emerging from Internet computing. Born in Soest, The Netherlands, Dr. Stork received the Ingenieur degree in electrical engineering from Delft University of Technology, Delft, The Netherlands.

Thursday Keynote

12:45 pm • Gateway Ballroom

The Challenges of Convergence

Alessandro Cremonesi
Strategy and System Technology Group Vice-President and Advanced System Technology General Manager, STMicroelectronics

Abstract: In this talk, the trends of the major application fields in the era of convergence are analyzed. The emphasis is on the challenges the semiconductor industry will have to face to address these new trends and opportunities.

Applications are becoming increasingly complex and the need to guarantee the coexistence of a wider range of applications on a single chip makes system-level integration a real challenge. Most of the applications will run on platforms designed for portable products, pushing the industry to emphasize power budgets for new designs, both at silicon and at system level. From the platform architecture perspective, multiprocessing is already a reality, and the industry will have to find new paradigms to handle the increased complexity at the system, embedded software, and at the silicon implementation levels.

The talk concludes with future perspectives from the viewpoint of ST's advanced research organization.

Biography: Alessandro Cremonesi received a Doctorate in Electronics Engineering from the University of Pavia, Italy, in 1984. After a period of research activity in the opto-electronics field at the University of Pavia, he joined STMicroelectronics working in different fields from telecommunications to audio/video digital signal processing and multimedia applications. At present, Alessandro Cremonesi is V.P. of Strategy and System Technology Group and General Manager of Advanced System Technology (AST) Group at STMicroelectronics with the responsibility of the Corporate System R&D and the Corporate Strategic Marketing activities across 14 different STMicroelectronics Labs worldwide.

DAC Pavilion Panels – Booth# 2228

DAC has an exciting line-up of panels and presentations in the DAC Pavilion (Booth 2228) on the exhibit floor. The DAC Pavilion sessions are open to all attendees and feature provocative technical, business, and strategy discussions.

Monday, July 24 • 9:30 am - 10:30 am Track: **Business**

Dataquest at DAC with Gary Smith: EDA Trends and What's Hot at DAC

Moderator: **Shishpal Rawat** - *Intel Corp., Folsom, CA*
Panelist: **Gary Smith** - *Gartner Dataquest, San Jose, CA*

A retrospective of the ever popular annual Sunday Gartner Dataquest EDA and semiconductor industry presentation followed by a review of the hot products at DAC for 2006 and a Q&A .

Monday, July 24 • 11:00 am - 12:00 pm Track: **Business**

What Will it Take to Break the $4B Revenue Cap?

Moderator: **Kathryn Kranen** - *Jasper Design Automation, Inc., Mountain View, CA*
Panelists: **Lucio Lanza** - *Lanza techVentures, Palo Alto, CA*
Nick Pappas - *Canaccord Adams, San Francisco, CA*
Jim Hogan - *Private Investor, Santa Cruz, CA*

Today's design teams are facing challenges 10x greater than just 18 months ago. Can EDA keep up, or has it become the limiting factor for chip design? Some believe ESL and DFM have the potential to drive future growth beyond the $4B revenue cap into double digits. This panel will discuss and debate the emergence of new tools and technologies, business partnerships and business models to explore what the future holds for the EDA industry.

Monday, July 24 • 1:00 pm - 2:00 pm Track: **Business**

Ask the CTO

Moderator: **Kurt Keutzer** - *Univ. of California, Berkeley, CA*
Panelists: **Raul Camposano** - *Synopsys, Inc., Mountain View, CA*
Ted Vucurevich - *Cadence Design Systems, Inc., San Jose, CA*

Continuing in the tradition of the popular "Ask the CTO" panels, this year's group will answer your toughest questions about your critical SoC design challenges. This year we will expand the focus to examine what's driving these design issues (and solutions), including leading-edge consumer gaming and multimedia, traditionally some of the most demanding applications.

Monday, July 24 • 3:00 pm - 4:00 pm Track: **MEGa**

Inside the iPod

Moderator: **Aurangzeb Khan** - *Cadence Design Systems, Inc., San Jose, CA*
Panelist: **Chris Crotty** - *iSuppli Corp., El Segundo, CA*

The iPod energized the personal audio player market, becoming the latest in "must-have" consumer products. Apple's strategy includes quickly bringing new products to market, addressing multiple price points and form factors tailored for different market segments, while creating an optimized supply-chain. The iPod is a brilliant combination of off-the-shelf parts, ASICs, and IP. This panel gives attendees a unique perspective into the electronics product value chain behind Apple's number one selling product.

Monday, July 24 • 4:15 pm - 5:15 pm Track: **Business**

Mass Book Signing

Moderator: **Lee Wood** - *MP Associates, Inc., Boulder, CO*

Authors of popular electronic design or design automation books in 2006 are invited to participate in a book signing session in the DAC Pavilion. The session is designed to give attendees the opportunity to meet the authors and have copies signed of popular technical books published in 2005/2006. Publishers of the invited authors' books will be available with copies for sale.

The 43rd Design Automation Conference • July 24 – 28, 2006 • San Francisco, CA

DAC Pavilion Panels – Booth# 2228

Tuesday, July 25 • 10:15 am - 11:00 am Track: **Verification & Test**

The Do's and Don'ts of Verification

Moderator: **Alan Hu** - *Univ. of British Columbia, Vancouver, BC, Canada*
Panelists: **Hillel Miller** - *Freescale Semiconductor, Inc., Herzlia Pituach, Israel*
Narendra Konda - *NVIDIA Corp., San Jose, CA*
Mike Beaver - *Transmeta Corp., Santa Clara, CA*

The pain of verification is relentless. Companies designing increasingly complex SoCs are spending considerable time and applying more and more resources to tackle the challenges of verification. Today, many companies still rely heavily upon simulation to address their functional verification needs, yet most would agree that simulation alone is simply not enough. Promising new hardware methods are proliferating -- acceleration, emulation and FPGA prototyping -- and there is growing usage of formal techniques. How do you decide what to use, and when? This panel brings together a few experts in verification to examine how to get the most out of your verification environment. Verification veterans will discuss what they are doing that works and what doesn't. Learn what leading edge companies are doing to resolve the verification challenge.

Tuesday, July 25 • 11:30 am - 12:15 pm Track: **Business**

Design Team Collaboration: Tools Challenge or Organization Responsibility

Moderator: **Penny Herscher** - *firstRain, Foster City, CA*
Panelists: **Marty Deneroff** - *DE Shaw Research & Dev., New York, NY*
Prasad Subramanian - *eSilicon Corp., Murray Hill, NJ*
Taguchi Hirofumi - *Matsushita Electric Industrial Co., Ltd., Kyoto, Japan*

Expanding system chip complexity is driving increasing specialization. Multi-site/multinational design teams are rapidly becoming the norm for 90 and 65nm SoC design. Systems designers, chip integrators, RTL designers, layout engineers, and verification engineers are feeling the pressure to synchronize development efforts across these multidiscipline groups. How should existing design practices evolve?

Tuesday, July 25 • 1:00 pm - 1:45 pm Track: **Business**

Exporting in the Hallway

Moderator: **Walden C. Rhines** - *Mentor Graphics Corp., Wilsonville, OR*
Panelists: **Larry Disenhof** - *Cadence Design Systems, Inc., Chelmsford, MA*
Douge Martin - *Mentor Graphics Corp., Wilsonville, OR*
Erik Oliver - *Rambus, Los Altos, CA*

When you employ a "non-US person" in the US, and allow them access to your software or your customer's IP, you are effectively exporting this technology to their country of citizenship. Have you just broken a law? Pending proposals in Washington may restrict exports to China – will this affect the industry? As companies broaden their global sales and operations, they need to stay abreast of coming changes in export regulations. Working through the EDA Consortium, this panel's team members have successfully rewritten US and international export regulations, easing these regulations as they affect the industry. The panelists will provide the latest news from Washington -- what you don't know "can" hurt you. Organized by EDAC.

Tuesday, July 25 • 2:00 pm - 2:45 pm Track: **Business**

Shattering the Glass Ceiling: A Decade of Growth for Women

Moderator: **Peggy Aycinena** - *EDA Confidential, San Mateo, CA*
Panelists: **Mary Jane Irwin** - *Pennsylvania State Univ., University Park, PA*
Jan Willis - *Cadence Design Systems, Inc., San Jose, CA*
Ellen J. Yoffa - *IBM Research, Hawthorne, NY*
(Winner 2006 Marie R. Pistilli Women in EDA Achievement Award)

The Workshop for Women in Design Automation is celebrating 11 years. Are women in the electronics industry better off? What strategies do today's women leaders use to break through the 'glass ceiling'? This panel will interview three of today's most successful women for their business acumen and insights into where women will go next in the next decade.

Tuesday, July 25 • 4:00 pm - 4:45 pm Track: **Interconnect Reliability & DFM**

The Fabless Model: Is DFM Our Salvation or Demise?

Moderator: **Dennis Wassung** - *Canaccord Adams, Boston, MA*
Panelists: **Walter Ng** - *Chartered Semiconductor Manufacturing, Inc., Milpitas, CA*
Matt Nowak - *Qualcomm, San Diego, CA*
Thomas Blaesi - *SIGMA-C Software AG, Santa Clara, CA*

At 90nm and below, iterations put the quest for timely, reasonable yields in peril. Despite urgent need for exchange of critical information, fabs and fabless companies still struggle to overcome obstacles preventing that exchange. So who controls the yield – fabs or fabless companies? Panelists will examine enablers for critical data exchange between the two and if EDA can bring salvation.

DAC Pavilion Panels – Booth# 2228

Wednesday, July 26 • 10:00 am - 10:45 am

Student Design Contest Award Presentations

Moderators: **Alan Mantooth** - *Univ. of Arkansas, Fayetteville, AR*
Bill Bowhill - *IBM Corp., Hudson, MA*

Presentation of winners of the Student Design Contest, organized by the Design Automation Conference and the International Solid State Circuits Conference (ISSCC).

Wednesday, July 26 • 11:15 am - 12:00 pm Track: **MEGa**

The Xbox 360 Uncloaked: Doing What it Takes to Get Chips into High-Volume Consumer Electronics

Moderator: **Jayaram Bhasker** - *eSilicon Corp., Allentown, PA*
Panelist: **Dean Takahashi** - *San Jose Mercury News, San Jose, CA*

Dean Takahashi, author of "The Xbox 360 Uncloaked," will talk about a case study in the video game business on how Microsoft designed its newest video game console and what it required from the chip vendors in order to get the project finished on time. Vendors such as IBM and ATI Technologies had to embrace new business models to win Microsoft's business.

Wednesday, July 26 • 1:00 pm - 2:00 pm Track: **MEGa**

AMD/DreamWorks - Fueling Technology Innovation

Moderator: **Rich Friedrich** - *Hewlett-Packard, Palo Alto, CA*
Panelists: **Randy Allen** - *Advanced Micro Devices, Inc., Austin, TX*
Ed Leonard - *DreamWorks Animation SKG, Glendale, CA*

With increasing demand to release multiple high-quality 3D computer-generated films every year, you need serious hardware computing power and faster, inherently more complex chips to render in record time. Join us for a special presentation by Ed Leonard, Chief Technology Officer of DreamWorks Animation SKG, and Randy Allen, AMD Corporate Vice President, and discover what technology innovations are required to fuel their animation needs to deliver one fantastic adventure after another, year after year.

Wednesday, July 26 • 2:15 pm - 3:15 pm Track: **System Level & Embedded**

ESL: Software Engineers Are from Pluto and Hardware Engineers Are from Mercury: Can ESL Bridge the Gap?

Moderator: **John Blyler** - *ChipDesign Magazine, Portland, OR*
Panelists: **Maurizio Vitale** - *Philips Semiconductors, Pittsburgh, PA*
Michael Uhner - *MIPS Technologies, Inc., Mountain View, CA*
Kazu-Yoshi Kikuta - *D-Clue Technologies CO. Ltd., Yokohama, Japan*

Hardware engineers talk RTL. Software engineers talk C/C++. Communication is not just a translation problem. Software engineers use system processing, traffic, and storage behavior as their development context, while the hardware engineers' context is bit- and nanosecond-accurate implementation. Hardware and software must be co-developed with system design intent as context. So, what do the software guys need from the hardware guys? The panel will answer this question in plain English.

Wednesday, July 26 • 4:00 pm - 4:45 pm Track: **Business**

The Accidental Pirate

Moderator: **Sanjay Srivastava** - *Denali Software, Palo Alto, CA*
Panelists: **Scott Baeder** - *Cadence Design Systems, Inc., Chelmsford, MA*
Randy Ohara - *Intel Corp., Santa Clara, CA*
Lynn Sweetwood - *Macrovision, Schramsburg, IL*

It is estimated that 36% of the world's software is pirated. With the continuing globalization of EDA software usage, IP design reuse, and technology advances that enables a worldwide virtual design network, the potential for piracy of software and IP increases. This panel will illicit and discuss the challenges facing the EDA, IP and design community as it relates to piracy, and talk about what can be done to address or mitigate the issues raised. Organized by EDAC.

DAC Pavilion Panels – Booth# 2228

Thursday, July 27 • 10:00 am - 10:45 am Track: **System Level & Embedded**

Developing Consumer SoCs - IP and Automation or Sticks and Duct Tape?

Moderator: **Ed Sperling** - *Electronic News, San Jose, CA*
Panelists: **Kevin Walsh** - *Synopsys, Inc., Mountain View, CA*
Sanjay Dave - *ATI Research, Santa Clara, CA*
Nir Sever - *Zoran Microelectronics, Haifa, Israel*

The competing consumer market requirements of: more features, lower cost and earlier to market make building SoCs for consumer products a daunting task. EDA automation and IP offer the promise of being able to pull together many pre-designed blocks quickly and easily into the SoC of your dreams. Are you dreaming? Is the challenge the same for startups and established companies? The panelists will discuss their experience, good and bad, in assembling SoCs from third party and in-house IP to create innovative, industry-leading consumer products.

Thursday, July 27 • 11:00 am - 11:45 am Track: **Business**

Wireless USB - the Next Ubiquitous Connectivity Standard?

Moderator: **Jim Lipman** - *SoC Central and TechOnline, Livermore, CA*
Panelists: **Joachim Kunkel** - *Synopsys, Inc., Mountain View, CA*
Jon Rosdahl - *Samsung Electronics, Highland, UT*
Sean Coffey - *Realtek Semiconductor Corp., San Francisco, CA*

What are the biggest challenges involved in adding wireless connectivity to SoC designs? Which building blocks need to be available? How does a strong certification/standards group help to ensure quality end-products? Panelists discuss the Wireless USB ecosystem and what combination of IP, SoC technology and certification will be needed to make Wireless USB the next ubiquitous connectivity standard.

Thursday, July 27 • 12:00 pm - 12:45 pm Track: **System Level & Embedded**

Troubleshooting the Multi-Processor SoC Design Flow

Moderator: **Jim Turley** - *Embedded Systems Design, Pacific Grove, CA*
Panelists: **Max Domeika** - *Intel Corp., Hillsboro, OR*
Grant Martin - *Tensilica, Santa Clara, CA*
Serge Leef - *Mentor Graphics Corp., Wilsonville, OR*

To create and verify a multi-processor system, designers must move data between cores, orchestrate shared and local resource allocation, and often implement multiple operating systems. With much functionality now implemented in application software, it has become a critical component in hardware verification. New methodologies are required, but how should they work? Are IP providers, especially the embedded processor IP companies, best-placed to offer solutions? How can the hardware and software worlds unite to conquer this complex design problem?

Friday, July 28

TUTORIAL 3 - REAL DFM SOLUTIONS – TOOLS, METHODOLOGIES, AND SUCCESSES

Rm: 304

Organizer: **Andrew B. Kahng** - *Univ. of California at San Diego, La Jolla, CA*
Presenters: **Nagaraj NS** - *Texas Instruments Inc., Dallas, TX*
Jean-Pierre Schoellkopf - *STMicroelectronics, Crolles, France*
Mike Smayling - *Applied Materials, Sunnyvale, CA*
Ban P. Wong - *Chartered Semiconductor, Milpitas, CA*
Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*

TUTORIAL 4 - SURVIVING AND THRIVING IN THE WORLD OF CHIP AND PACKAGE CO-DESIGN

Rm: 305

Organizers: **Chung-Kuan Cheng** - *Univ. of California at San Diego, La Jolla, CA*
Howard Chen - *IBM Corp., Yorktown Heights, NY*
Presenters: **Paul Harvey** - *IBM Corp., Austin, TX*
Howard Chen - *IBM Corp., Yorktown Heights, NY*
Lei He - *Univ. of California, Los Angeles, CA*
Chung-Kuan Cheng - *Univ. of California at San Diego, La Jolla, CA*
Kaushik Sheth - *Rio Design Automation, Inc., Santa Clara, CA*

TUTORIAL 5 - SYSTEMVERILOG: LANGUAGE TUTORIAL AND INDUSTRIAL VERIFICATION EXPERIENCE

Rm: 307

Organizer: **Johny Srouji** - *IBM Corp., Austin, TX*
Presenters: **Johny Srouji** - *IBM Corp., Austin, TX*
Karen Pieper - *Synopsys, Inc., Sunnyvale, CA*
Tom Fitzpatrick - *Mentor Graphics Corp., Groton, MA*
John Havlicek - *Freescale Semiconductor, Inc., Austin, TX*
Matt Maidment - *Intel Corp., Portland, OR*
Cliff Cummings - *Sunburst Design, Inc., Portland, OR*

TUTORIAL 6 - TOOLS FOR HYBRID EMBEDDED SYSTEMS: MODELING, VERIFICATION, AND DESIGN

Rm: 302

Organizer: **Luca Carloni** - *Columbia Univ., New York, NY*
Presenters: **Hilding Elmqvist** - *Dynasim AB, Lund, Sweden*
George Pappas - *Univ. of Pennsylvania, Philadelphia, PA*
Pieter J. Mosterman - *The MathWorks, Inc., Natick, MA*
Alessandro Pinto - *Univ. of California, Berkeley, CA*
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

TUTORIAL 7 - FROM BASIC TO ADVANCED TECHNIQUES FOR SILICON DEBUG AND DIAGNOSIS

Rm: 306/308

Organizer: **Srikanth Venkataraman** - *Intel Corp., Hillsboro, OR*
Presenters: **Srikanth Venkataraman** - *Intel Corp., Hillsboro, OR*
Miron Abramovici - *DAFCA Inc., Framingham, MA*
Robert Aitken - *ARM, Sunnyvale, CA*

Topics and Related Sessions

Business

Sessions: 1, 6, 100, 150

System Level and Embedded

Sessions: 2, 4, 9, 16, 21, 22, 31, 39, 49, 52

MEGa

Sessions: 17, 23, 29, 35

Low Power and Power

Sessions: 8, 11, 13, 27, 33, 34, 37, 55

Analog and Circuit

Sessions: 3, 15, 40, 51, 57

Interconnect, Reliability and DFM

Sessions: 5, 10, 12, 26, 44, 45, 58, 59

Verification and Test

Sessions: 7, 19, 20, 25, 42, 46, 48, 60, 61

Synthesis and FPGA

Sessions: 14, 28, 30, 32, 36, 38, 54

Physical Design

Sessions: 18, 24, 43, 62

Beyond the Die

Sessions: 50, 56

New and Emerging Technologies

Sessions: 41, 47, 53

General Session/Keynote Address

Tuesday, July 25 • 8:30 am - 10:15 am **Gateway Ballroom**

Opening Remarks: **Ellen Sentovich** - General Chair, 43rd DAC

Awards Presented By: **Diana Marculescu**
ACM/SIGDA Representative

Alan Mantooth
IEEE/CASS/CANDE Representative

Awards/Scholarships

- **Marie R. Pistilli Women in EDA Achievement Award**
- **P.O. Pistilli Undergraduate Scholarships (ACSEE)**
- **DAC/ISSCC Student Design Contest - Best Overall Award**
- **DAC Graduate Scholarships**
- **ACM/TODAES Best Paper Award**
- **ACM Distinguished Service Award**
- **Phil Kaufman Award**
- **IEEE/CASS Education Award**
- **IEEE/CASS Industrial Pioneer Award**
- **IEEE/CASS Donald O. Pederson Award**
- **IEEE/CASS CSVT Tranactions Best Paper Award**
- **IEEE/CASS VLSI Transaction Best Paper Award**
- **2006 IEEE Fellows**

Keynote Address:

Structuring Process and Design for Future Mobile Communication Devices

Hans Stork - *Senior Vice President and Chief Technology Officer, Director of Silicon Technology Department, Texas Instruments Inc.*

Tuesday July 25, 2006
10:30 am - 12:00 pm

All speakers are denoted in bold
S - denotes short paper
ß - denotes best paper candidate
- session of special interest to designers
- indicates videoed session

SESSION 1

Rm: **306/308**

PANEL: HOW WILL THE FABLESS MODEL SURVIVE?

Chair: Don Clark - *Wall Street Journal, San Francisco, CA*
Organizer: Riko Radojcic

The fabless model was traditionally enabled through clean interfaces — both in technical and business terms — between foundries and fabless semiconductor companies. However, with advanced geometry and analog/mixed-signal process nodes, the technical challenges have been greatly magnified, so that successful semiconductor design requires intimate co-optimization of design and manufacturing, infringing upon those clean interfaces. The panel presents views to these challenges and specifically how companies are planning to address them.

Panelists:

Thomas Hartung - *X-Fab Semiconductor Foundries AG, Erfurt, Germany*
Ana Hunter - *Samsung Semiconductor Inc., San Jose, CA*
Felicia James - *Cadence Design Systems, Inc., San Jose, CA*
Mark T. Bohr - *Intel Corp., Hillsboro, OR*
Brad Paulsen - *TSMC NA, San Jose, CA*
Nick Yu - *Qualcomm Inc., San Diego, CA*

SESSION 2

Rm: **307**

SPECIAL SESSION: WHY DOESN'T MY SYSTEM WORK?

Chair: Bart Vermeulen - *Philips Research, Eindhoven, Netherlands*
Organizer: Erik Jan Marinissen

Industry data shows that over 60% of complex chip design projects do require one or more respins, and that silicon debug has become the most time-consuming part of the development cycle of a new SoC. In this special session, industry experts discuss the in-system silicon debug problem and emerging solutions for it. The first speaker talks from the perspective of a design/debug engineer, with a host of experience of debugging actual microprocessor products. The second speaker discusses on-chip design-for-debug hardware required to create access to chip-internal signals. The third speaker describes the software that helps the debug process by visualization and translation to higher levels.

2.1 The Good, the Bad, and the Ugly of Silicon Debug
Doug Josephson - *Intel Corp., Fort Collins, CO*

2.2 A Reconfigurable Design-for-Debug Infrastructure for SoCs
Miron Abramovici, Paul Bradley, Kumar Dwarakanath, Peter Levin, Gerard Memmi, Dave Miller - *DAFCA Inc., Framingham, MA*

2.3 Visibility Enhancement for Silicon Debug
Yu-Chin Hsu, Furshing Tsai, Wells Jong, Ying-Tsai Chang - *Novas Software, Inc., San Jose, CA*

SESSION 3

Rm: **305**

HIERARCHICAL SYNTHESIS FOR MIXED-SIGNAL DESIGNS

Chair: Gerd Vandersteen - *IMEC/VUB, Heverlee, Belgium*
Organizers: Geert Van Der Plas, Koen Lampaert

This session describes the application of hierarchical synthesis and optimization techniques to the design of mixed-signal systems. The first two papers use hierarchical optimization techniques to design a charge pump phase-locked loop and a delta-sigma A/D converter. The third paper describes new methods to generate yield-aware pareto surfaces that link performance tradeoffs and their yield impacts, for use in hierarchical circuit design.

ß-3.1 A CPPLL Hierarchical Optimization Methodology Considering Jitter, Power and Locking Time
Jun Zou, Daniel Mueller, Helmut Graeb, Ulf Schlichtmann - *Technische Universitaet Muenchen, Munich, Germany*

3.2 Hierarchical Bottom-up Analog Optimization Methodology Validated by a Delta-Sigma A/D Converter Design for the 802.11a/b/g Standard
Tom Eeckelaert, Raf Schoofs, Georges Gielen, Michiel Steyaert, Willy Sansen - *Katholieke Univ., Heverlee, Belgium*

3.3 Generation of Yield-Aware Pareto Surfaces for Hierarchical Circuit Design Space Exploration
Saurabh K. Tiwary - *Carnegie Mellon Univ., Pittsburgh, PA*
Pragati K. Tiwary - *BIT Mesra, Ranchi, India*
Rob A. Rutenbar - *Carnegie Mellon Univ., Pittsburgh, PA*

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Tuesday July 25, 2006
10:30 am - 12:00 pm

SESSION 4

Rm: **304**

PROCESSOR AND COMMUNICATION CENTRIC SOC DESIGN

Chair: Johannes Stahl - *CoWare, Inc., San Jose, CA*
Organizers: Brian Bailey, Rainer Leupers

Multi-processor systems-on-chip (MPSoCs) are becoming a necessary way to balance performance, power and reliability while maintaining the maximum degree of flexibility. The first paper proposes the use of bus scenarios for an optimized time budget assignment to system tasks. The second paper proposes a new approach to implement custom processor instruction set extensions. The third paper focuses on optimization of scratch-pad memory hierarchies for MPSoC architectures, while the last paper deals with handling both transient and permanent faults in a tiled architecture, targeting single program, multiple data applications.

4.1 A Real Time Budgeting Method for Module-Level-Pipelined Bus Based System Using Bus Scenarios

Tadaaki Tanimoto - *Renesas Technology Corp., Kodaira Tokyo, Japan*
Seiji Yamaguchi, Akio Nakata, Teruo Higashino - *Osaka Univ., Suita Osaka, Japan*

4.2 Exploiting Forwarding to Improve Data Bandwidth of Instruction-Set Extensions

Ramkumar Jayaseelan, Haibin Liu, Tulika Mitra - *National Univ. of Singapore, Singapore*

4.3s Multiprocessor System-on-Chip Data Reuse Analysis for Exploring Customized Memory Hierarchies

Ilya Issenin - *Univ. of California, Irvine, CA*
Erik Brockmeyer, Bart Durinck - *IMEC, Leuven, Belgium*, Nikil Dutt - *Univ. of California, Irvine, CA*

4.4s Modeling a Fault-Tolerant Multiprocessor SoC with Run-time Fault Recovery

Xinping Zhu - *Northeastern Univ., Boston, MA*
Wei Qin - *Boston Univ., Boston, MA*

SESSION 5

Rm: **303**

PRACTICAL APPLICATIONS OF DFM

Chair: Nagib Hakim - *Intel Corp., Santa Clara, CA*
Organizer: Michael Orshansky

Design for manufacturing is starting the transition from a purely back-end application of resolution enhancement techniques to a rich set of tools and analysis techniques to improve the yield and manufacturability of a variety of different integrated circuit components. This session shows three interesting applications: SRAM, where the impact of manufacturing variability is paramount; systematic yield detractors, which are often found to be specific layout constructs, and; path delay variation, which are a major source of timing yield loss.

5.1 Statistical Analysis of SRAM Cell Stability

Kanak B. Agarwal, Sani R. Nassif - *IBM Corp., Austin, TX*

5.2 Criticality Computation in Parameterized Statistical Timing

Jinjun Xiong - *Univ. of California, Los Angeles, CA*
Vladimir Zolotov - *IBM Corp., Yorktown Heights, NY*
Natesan Venkateswaran - *IBM Corp., Hopewell Junction, NY*
Chandu Visweswariah - *IBM Corp., Yorktown Heights, NY*

5.3s Mixture Importance Sampling and Its Application to the Analysis of SRAM Designs in the Presence of Rare Failure Events

Rouwaida N. Kanj - *IBM Corp., Austin, TX*
Rajiv V. Joshi - *IBM Corp., Yorktown Heights, NY*
Sani R. Nassif - *IBM Corp., Austin, TX*

5.4s An Up-stream Design Auto-fix Flow for Manufacturability Enhancement

Jie Yang - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Ethan Cohen - *Advanced Micro Devices, Inc., Austin, TX*
Cyrus Tabery, Norma Rodriguez - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Mark Craig - *Advanced Micro Devices, Inc., Austin, TX*

Tuesday July 25, 2006
2:00 pm - 4:00 pm

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SESSION 6

Rm: **306/308**

PANEL: THE IC NANOMETER RACE: WHAT WILL IT TAKE TO WIN?

Chair: Walden C. Rhines - *Mentor Graphics Corp., Wilsonville, OR*
Organizer: Laura Parker

Creating ICs in the nanometer age is a high-stakes race that few companies can afford to compete in — and even fewer can win. Hear how senior technologists from the world's top technology companies are striving to improve their chances of success. Will leakage constraints force power-sensitive applications to stay with older technologies, or will there be a bifurcation to a new process technology? Will ballooning capital equipment expenses delay new capacity or price out design rules for mainstream applications? Will silicon-on-insulator and new device structures like FinFETs force rethinking of design, modeling and simulation methodologies? And which EDA technologies, delivered when, will be critical for victory? These senior technologists, from some of the biggest companies in the high tech industry, will discuss and debate how they think the overall industry will successfully transition to the nanometer age. Specific examples from the technologists' broad exposure to industry trends and competitors will help illustrate their forecasts and predictions.

Panelists:

Dennis Buss - *Texas Instruments Inc., Dallas, TX*
Philippe Magarshack - *STMicroelectronics, Crolles Cedex, France*
Fu-Chieh Hsu - *Taiwan Semiconductor Mfg. Co., Hsinchu, Taiwan*
Gadi Singer - *Intel Corp., Santa Clara, CA*
Ho-Kyu Kang - *Samsung Electronics Co., Ltd., Seoul, Korea*

SESSION 7

Rm: **307**

SPECIAL SESSION: BRIDGING THE SYSTEM TO RTL VERIFICATION GAP

Chair: Brian Bailey - *Verification Consultant, Oregon City, OR*
Organizer: Anmol Mathur

System-level models in C/C++ or SystemC are gaining widespread acceptance for developing golden functional reference models, as vehicles for micro-architecture exploration and as platforms for software development. Transaction-level models are used to provide a communication-accurate view of a design that simulates 100 to 1000 times faster than RTL. Since the high-level models can be simulated with real applications, the design team can often get a high level of confidence in the functional correctness of this model. Design teams are often spending 30-50% of their overall design cycle in this phase to generate the functional reference model and decide on the micro-architecture.

7.1 Use of C/C++ Models for Architecture Exploration and Verification of DSPs
David Brier - *Texas Instruments Inc., Dallas, TX*
Raj S. Mitra - *Texas Instruments Inc., Bangalore, India*

7.2 Maintaining Consistency Between SystemC and RTL System Designs
Christopher Lennard - *ARM, Cambridge, UK*
Alistair Bruce - *ARM, Sheffield, UK*
Andrew Nightingale, Nizar Romdhane - *ARM, Cambridge, UK*
M M Kamal Hashmi, Steve Beavis - *Spiratech Ltd., Manchester, UK*

7.3 SystemC Transaction Level Models and RTL Verification
Stuart Swan - *Cadence Design Systems, Inc., Redwood City, CA*

7.4 Towards a C++-Based Design Methodology Facilitating Sequential Equivalence Checking
Venkat Krishnaswamy - *Calypto Design Systems, Inc., Santa Clara, CA*
Phillipe Georgelin - *ST Microelectronics, Crolles, France*

SESSION 8

Rm: **305**

LEAKAGE, POWER ANALYSIS AND OPTIMIZATION

Chair: Nam Sung Kim - *Intel Corp., Hillsboro, OR*
Organizers: Naehyuck Chang, Sanu Mathew

This session covers topics related to leakage power modeling and optimization, ranging from leakage power analysis in the presence of variations and the use of charge recycling for MTCMOS circuits, to using sleep transistors and input vector generation for leakage reduction.

ß-8.1 Charge Recycling in MTCMOS Circuits: Concept and Analysis
Ehsan Pakbaznia - *Univ. of Southern California, Los Angeles, CA*
Farzan Fallah - *Fujitsu Labs. Ltd., Sunnyvale, CA*
Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

8.2 Projection-Based Statistical Analysis of Full-Chip Leakage Power with Non-Log-Normal Distributions
Xin Li, Jiayong Le, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

8.3s Physical Design Methodology of Power Gating Circuits for Standard-Cell-Based Design
Hyung-Ock Kim, Youngsoo Shin - *KAIST, Daejeon, South Korea*
Hyuk Kim, Iksoo Eo - *ETRI, Daejeon, South Korea*

8.4s Challenges in Sleep Transistor Design and Implementation in Low-Power Designs
Kaijian Shi - *Synopsys, Inc., Dallas, TX*
David Howard - *ARM Ltd., Cambridge, UK*

8.5s A Fast Simultaneous Input Vector Generation and Gate Replacement Algorithm for Leakage Power Reduction
Lei Cheng, Liang Deng, Deming Chen, Martin D.F. Wong - *Univ. of Illinois, Urbana, IL*

8.6s Timing Driven Power Gating
De-Shiuan Chiou, Shih-Hsin Chen, Shih-Chieh Chang - *National Tsing-Hua Univ., Hsinchu, Taiwan*
Chingwei Yeh - *National Chung Cheng Univ., Chiayi, Taiwan*

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SESSION 9

Rm: **304**

MPSOC DESIGN METHODOLOGIES AND APPLICATIONS

Chair: Dan Gajski - *Univ. of California, Irvine, CA*
Organizers: Peter Marwedel, Tajana Simunic

Multi-processor systems-on-chip (MPSoC) pose many new challenges to the design of embedded systems. The first two papers highlight design methdologies for two application extremes: a high-performance biomedical monitoring and reconfigurable low-power RFID tags. The next two papers discuss design tradeoffs between P2P vs. NoC interconnect, and between circuit-switching and packet-switching schemes.

ß- 9.1 A Multiprocessor System-on-Chip for Real-Time Biomedical Monitoring and Analysis: Architectural Design Space Exploration

Iyad Al Khatib - *KTH, Kista, Sweden*
Francesco Poletti - *Univ. of Bologna, Bologna, Italy*
Davide Bertozzi - *Univ. of Ferrara, Ferrara, Italy*
Luca Benini - *Univ. of Bologna, Bologna, Italy*
Mohamed Bechara, Hasan Khalifeh - *American Univ. of Beirut, Beirut, Lebanon*
Axel Jantsch - *Royal Institute of Tech., Stockholm, Sweden*
Rustam Nabiev - *Karolinska, Stockholm, Sweden*

9.2 An Automated, Reconfigurable, Low-Power RFID Tag

Alex K. Jones, Raymond R. Hoare, Swapna R. Dontharaju, Shenchih Tung, Ralph Sprang, Josh Fazekas, James T. Cain, Marlin H. Mickle - *Univ. of Pittsburgh, Pittsburgh, PA*

9.3 Design Space Exploration and Prototyping for On-Chip Multimedia Applications

Hyung Gyu Lee - *Seoul National Univ., Seoul, South Korea*
Umit Y. Ogras - *Carnegie Mellon Univ., Pittsburgh, PA*
Naehyuck Chang - *Seoul National Univ., Seoul, South Korea*
Radu Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

9.4 Evaluation and Design Tradeoffs Between Circuit-Switched and Packet-Switched NoCs for Application-Specific SoCs

Kuei-Chung Chang, Jih-Sheng Shen, Tien-Fu Chen - *National Chung Cheng Univ., Chia-Yi, Taiwan*

SESSION 10

Rm: **303**

STATISTICAL TIMING ANALYSIS

Chair: Chandu Visweswariah - *IBM Corp., Yorktown Heights, NY*
Organizers: David Blaauw, Hai Zhou

Static timing analysis continues to be a major source of innovation at the algorithmic and modeling levels. This session has four excellent papers in this area that will provide users and practitioners with a first hand view of new developments in academia and in industry.

10.1 Refined Statistical Static Timing Analysis Through Learning Spatial Delay Correlations

Ben Lee, Li-C Wang - *Univ. of California, Santa Barbara, CA*
Magdy S. Abadir - *Freescale Semiconductor, Inc., Austin, TX*

10.2 Statistical Timing Analysis with Correlated Non-Gaussian Parameters Using Independent Component Analysis

Jaskirat Singh - *Univ. of Minnesota, St. Paul, MN*
Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

10.3 Statistical Timing Based on Incomplete Probalistic Descriptions of Parameter Uncertainty

Wei-Shen Wang - *Univ. of Texas, Austin, TX*
Vladik Kreinovich - *Univ. of Texas, El Paso, TX*
Michael Orshansky - *Univ. of Texas, Austin, TX*

10.4 Probabilistic Interval-Valued Computation: Toward a Practical Surrogate for Statistics Inside CAD Tools

Amith Singhee, Claire F. Fang, James D. Ma, Rob A. Rutenbar - *Carnegie Mellon Univ., Pittsburgh, PA*

SESSION 100

Rm: **301**

DECISION-MAKING FOR COMPLEX SOCS IN CONSUMER ELECTRONIC PRODUCTS

Chair: Ron Wilson - *EDN, San Mateo, CA*
Organizer: Yervant Zorian

Consumer electronics chips are the technology drivers today. They require different types of optimizations and thus the need to adopt emerging solutions to meet such requirements. Optimizing for high volume production, low power, and shrinking sizes necessitate adequate tradeoff analysis and technical/business decision making by management. The lead managers in this session will discuss today's emerging solutions and their economic impact.

100.1 Qualcomm Lessons Learned at the 65nm Node

Charlie Matar, **Riko Radojcic** - *Qualcomm CDMA Technologies, San Diego, CA*

100.2 Low Power Challenges in Wireless ICs

Rene Delgado - *Freescale Semiconductor, Inc., Austin, TX*

100.3 Consumer Electronics Development Tradeoffs in the High-Tech Startup

Dawn Fitzgerald - *Aurora Enterprises, Boston, MA*

100.4 Architecture Planning Criteria for a System-in-Package Portable Multimedia Platform

Mario Manninger - *austriamicrosystems AG, Unterpremstaetten, Austria*

Tuesday July 25, 2006
4:30 pm - 6:30 pm

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SESSION 11

Rm: **306/308**

PANEL: ENTERING THE HOT ZONE — CAN YOU HANDLE THE HEAT AND BE COOL?

Chair: Daya Nadamuni - *Gartner Dataquest, San Jose, CA*
Organizer: Michelle Clancy

Electronic gadgets are becoming more pervasive at the office and in the home where they can no longer be equipped with large fans or vents. One of the biggest challenges is putting more functionality into a smaller space and managing heat dissipation. Lack of voltage scaling for future generations has forced designers to be more innovative to handle heat dissipation challenges. This panel discusses the breakthroughs required to address the power and thermal concerns for IC package and system designers, and the necessary cooperation between these teams and EDA companies.

Panelists:

Javier De La Cruz - *eSilicon Corp., Sunnyvale, CA*
Uming Ko - *Texas Instruments Inc., Dallas, TX*
Simon Burke - *ATI Technologies, Inc., Santa Clara, CA*
Rajit Chandra - *Gradient Design Automation, Santa Clara, CA*
Andrew Yang - *Apache Design Solutions, Inc., Mountain View, CA*
Sribalan Santhanam - *PA Semi, Santa Clara, CA*

SESSION 12

Rm: **307**

SPECIAL SESSION: RELIABILITY CHALLENGES FOR 65NM AND BEYOND

Chair: David Yeh - *Texas Instruments/SRC, Research Triangle Park, NC*
Organizers: Joel Phillips, Nagaraj NS

The intent of this special session: 1) Give the EDA community a comprehensive perspective on the problem, explaining what can go wrong (HCI, NBTI, EM, TDDB, SER, ESD, etc.), what will be the major challenges at 65nm and beyond, and how reliability interacts with other design constraints. For example, NBTI not only hurts the reliability of the circuit, but also reduces yield due to the high-temp burn-in process, and higher temperature density due to integration density worsens both EM and NBTI issues. 2) Survey design-in-reliability; what can designers do to build in reliability in products. 3) Present a tools perspective, including the primary effects (HCI, NBTI, EM) for which EDA tools are available, types of tools (dynamic simulation vs. static rule checking), necessary reliability infrastructure and flows that have worked in practice. Finally, new and developing areas of interest, missing pieces, and future opportunities will be discussed. 4) The topics covered in the special session will ensure no rehash of traditional topics and good flow of theory and practice. The session ensures a good balance of key physics phenomena, EDA tools and practical design flows.

12.1 Reliability Challenges for 45nm and Beyond
Joe McPherson - *Texas Instruments Inc., Dallas, TX*

12.2 Design Tools for Reliability Analysis
Zhihong Liu, Bruce W. McGaughy, James Z. Ma - *Cadence Design Systems, Inc., San Jose, CA*

12.3 Design in Reliability for Communication Designs
Uday B. Reddy - *Intel Corp., Folsom, CA*
Murty Dasaka, Pavan Kaipa - *Intel Corp., Bangalore, India*

12.4 Practical Aspects of Reliability Analysis for IC Designs
Thomas Pompl, Christian Schlunder, Martina Hommel, Heiko Nielen, Jens Schneider - *Infineon Tech. AG, Germany*

SESSION 13

Rm: **305**

POWER GRID ANALYSIS AND DESIGN

Chair: Sani R. Nassif - *IBM Corp., Austin, TX*
Organizers: Farid N. Najm, Vikram Jandhyala

Design and verification of the power grid have become critical steps for achieving timing success and noise free operation in high-performance integrated circuits. This session presents a sequence of excellent papers that cover a spectrum of issues in this area. It starts with a detailed study of power grid design issues covering inductance and decoupling capacitors in large microprocessor design. Subsequent papers cover detailed power grid simulation, variational analysis of the grid parasitics, and budgeting techniques for the decoupling capacitance.

ß-13.1 Power Grid Physics and Implications for CAD
Eli Chiprout - *Intel Corp., Hillsboro, OR*
Sanjay Pant - *Univ. of Michigan, Ann Arbor, MI*

ß-13.2 Fast Analysis of Structured Power Grid by Triangularization Based Structure Preserving Model Order Reduction
Hao Yu, Yiyu Shi, Lei He - *Univ. of California, Los Angeles, CA*

13.3 Stochastic Variational Analysis of Large Power Grids Considering Intra-die Correlations
Praveen Ghanta, Sarma Vrudhula, Sarvesh Bhardwaj - *Arizona State Univ., Tempe, AZ*, Rajendran Panda - *Freescale Semiconductor, Inc., Austin, TX*

13.4 A Fast On-Chip Decoupling Capacitance Budgeting Algorithm Using Macromodeling and Linear Programming
Min Zhao, Rajendran Panda, Savithri Sundareswaran, Shu Yan, Yuhong Fu - *Freescale Semiconductor, Inc., Austin, TX*

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SESSION 14

Rm: **304**

ADVANCES IN FORMAL SOLVERS

Chair: Jeremey Levitt - *Mentor Graphics Corp., San Jose, CA*
Organizers: Alan Hu, Anmol Mathur

The session focuses on advances in Boolean and word-level solvers at the heart of formal verification tools. The first paper describes a distributed approach to dynamic variable ordering for BDDs. The next paper describes the use of SAT for redundancy removal using output don't-cares for simplifying circuit descriptions for simplifying Boolean reasoning. The third paper presents word-level techniques for efficient solution of difference logic. The final paper in this session proposes a novel framework for extracting illegal states of a sequential circuit and using them during SAT-based induction.

14.1 Distributed Dynamic BDD Reordering
Ziv Nevo - *IBM Corp., Haifa, Israel*
Monica C. Farkash - *IBM Corp., Austin, TX*

ß- **14.2 SAT Sweeping with Local Observability Don't-Cares**
Qi Zhu, Nathan B. Kitchen - *Univ. of California, Berkeley, CA*
Andreas Kuehlmann - *Cadence Berkeley Labs, Berkeley, CA*
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

14.3 Predicate Learning and Selective Theory Deduction for a Difference Logic Solver
Chao Wang, Aarti Gupta, Malay Ganai - *NEC-Labs America, Princeton, NJ*

14.4 Fast Illegal State Identification for Improving SAT-Based Induction
Vishnu C. Vimjam, Michael S. Hsiao - *Virginia Tech., Blacksburg, VA*

SESSION 15

Rm: **303**

GATE MODELING AND MODEL ORDER REDUCTION

Chair: Peter Feldmann - *IBM Corp., Yorktown Heights, NY*
Organizers: Charlie Chung-Ping Chen, Joel Phillips

The first half of this session features advances in modeling for timing analysis, presenting improved models for multi-input switching and statistical computations for current-based models. The second half of the session presents advances related to reduced-order modeling. Two papers discuss detailed technical issues related to passivity preserving modeling, and the final paper features new ideas about handling large numbers of model inputs.

15.1 A Multi-port Current Source Model for Multiple Input Switching Effects in CMOS Library Cells
Chirayu S. Amin, Chandramouli Kashyap, Noel Menezes, Kip Killpack, Eli Chiprout - *Intel Corp., Hillsboro, OR*

15.2s Statistical Logic Cell Delay Analysis Using a Current-Based Model
Hanif Fatemi, Shahin Nazarian, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

15.3s Multi-Shift Quadratic Alternating Direction Implicit Iteration for High-Speed Positive-Real Balanced Truncation
Ngai Wong - *Univ. of Hong Kong, Hong Kong*
Venkataramanan Balakrishnan - *Purdue Univ., West Lafayette, IN*

15.4 A Fast Passivity Test for Descriptor Systems via Structure-Preserving Transformations of Skew-Hamiltonian/Hamiltonian Matrix Pencils
Ngai Wong, Chung Kwan Chu - *Univ. of Hong Kong, Hong Kong*

15.5 Model Order Reduction of Linear Networks With Massive Ports via Frequency-Dependent Port Packing
Peng Li, Weiping Shi - *Texas A&M Univ., College Station, TX*

SESSION 150

Rm: **301**

TRADEOFFS AND CHOICES FOR EMERGING SOCS IN HIGH-END APPLICATIONS

Chair: Nic Mokhoff - *EE Times, Manhasset, NY*
Organizer: Yervant Zorian

Design and manufacturing flows and methodologies are directly impacted by the demand for emerging SoCs with increasing performance and parallelism. Moving to new semiconductor technology nodes can significantly affect the choices of suppliers. This session will provide an overview of changing needs and corresponding management decision criteria to make the right choices from a pool of alternate options for flows, methodologies and suppliers.

150.1 Assessing Process Nodes and IP for SoC Development
Ken Wagner - *PMC-Sierra, Inc., Burnaby, BC, Canada*

150.2 Open-IP: How Your Selection of IP Drives Your ASIC Success
Rajesh Shah - *Open-Silicon, Milpitas, CA*

150.3 Yield, Manufacturability and Test: The Criteria to Judge the Right Design Investment
Rajesh Galivanche - *Intel Corp., Santa Clara, CA*
Kee Sup Kim - *Intel Corp., Folsom, CA*

150.4 Management Day Cocktail Party

Wednesday July 26, 2006
8:30 am - 10:00 am

All speakers are denoted in bold
S - denotes short paper
ß - denotes best paper candidate
- session of special interest to designers
- indicates videoed session

SESSION 16

Rm: **306/308**

SPECIAL SESSION: MPSOC DESIGN TOOLS

Chair: Pierre Paulin - *STMicroelctronics, Nepean, ON, Canada*
Organizer: Sumit Gupta

This session discusses the problems associated with the design and verification of SoCs that have instantiations of multiple processors and the requirements that this places on software tools. We will discuss issues pertaining to system-level modeling and application partitioning and mapping as it pertains to the challenges faced by MPSoC designers. Specifically, we will present the problems faced by MPSoC designers and why and how these problems are unique to multi-processor systems. We will discuss issues related to real-time operating system (RTOS) requirements, application partitioning, inter-processor communication, multi-processor design, et cetera. We will follow this with how software design tools can help alleviate some of these problems, what parts of the design flow can be fully automated, and what parts can be aided by design tools. We will also discuss the state of design tools in the industry and academia today and what pieces of the puzzle are missing.

16.1 Overview of the MPSoC Design Challenge

Grant E. Martin - *Tensilica, Inc., Santa Clara, CA*

16.2 Programming Models and HW-SW Interfaces Abstraction for Multi-Processor SoC

Ahmed A. Jerraya - *TIMA/CNRS, Grenoble, France*
Frederic Petrot - *TIMA/INPG, Grenoble, France*
Aimen Bouchhima - *TIMA, Grenoble, France*

16.3 System-Level Exploration Tools for MPSoC Designs

Simon Davidmann, Peter Flake, Frank Schirrmeister - *Imperas, Inc., Palo Alto, CA*

SESSION 17

Rm: **307**

SPECIAL SESSION: HIGHLIGHTS OF ISSCC: MULTIMEDIA

Chair: Wanda Gass - *Texas Instruments Inc., Dallas, TX*
Organizers: Andrew B. Kahng, Ingrid Verbauwhede

This is the now-traditional best of ISSCC session at DAC. This year, we selected the best of multimedia-related papers at ISSCC as part of our theme day session offerings.

17.1 Design of a 125uW, Fully Scalable MPEG-2 and H.264/AVC Video Decoder for Mobile Applications

Tsu-Ming Liu, Ching-Che Chung, Chen-Yi Lee - *National Chiao-Tung Univ., Hsinchu, Taiwan*
Ting-An Lin, Sheng-Zen Wang - *MediaTek, Inc., Hsinchu, Taiwan*

17.2 Memory in the Multimedia Era

Changhyun Kim - *Samsung Electronics Co, Ltd., Gyeonggi-do, Korea*

17.3s A CMOS SoC for 56/18/16 CD/DVD-dual/RAM Applications

Jyh-Shin Pan, Hao-Cheng Chen, **Bing-Yu Hsieh**, Hong-Ching Chen, Roger Lee, Ching-Ho Chu, Yuan-Chin Liu, Chuan Liu, Lily Huang, Chang-Long Wu, Meng-Hsueh Lin, Chun-Yiu Lin, Shang-Nien Tsai, Jenn-Ning Yang, Chang-Po Ma, Yung Cheng, Shu-Hung Chou, Hsiu-Chen Peng, Peng-Chuan Huang, Benjamin Chiu, Alex Ho - *MediaTek Inc., Hsinchu, Taiwan*

17.4 Hierarchical Power Distribution and Power Management Scheme for a Single Chip Mobile Processor

Toshihiro Hattori, Takahiro Irita, Masayuki Ito, Eiji Yamamoto, Hisashi Kato, Go Sado, Tetsuhiro Yamada, Kunihiko Nishiyama, Hiroshi Yagi, Takao Koike, Yoshihiko Tsuchihashi, Motoki Higashida, Hiroyuki Asano, Izumi Hayashibara, Ken Tatezawa, Yasuhisa Shimazaki, Naozumi Morino, Yoshihiko Yasu, Tadashi Hoshi, Yujiro Miyairi, Kazumasa Yanagisawa, Kenji Hirose, Saneaki Tamaki, Shinichi Yoshioka - *Renesas Technology Corp., Tokyo, Japan*
Toshifumi Ishii, Yusuke Kanno, Hiroyuki Mizuno, Tetsuya Yamada, Naohiko Irie - *Hitachi, Ltd, Tokyo, Japan*
Reiko Tsuchihashi, Nobuto Arai, Tomohiro Akiyama, Koji Ohno - *NTT DoCoMo, Inc, Yokosuka, Japan*

SESSION 18

Rm: **305**

BUFFER INSERTION

Chair: Charles J. Alpert - *IBM Corp., Austin, TX*
Organizers: Dirk Stroobandt, Louis Scheffer

Buffer insertion is important for coping with timing constraints but the sheer number of buffers needed poses problems. The first paper deals with the large circuit sizes in an efficient way. The other two papers acknowledge that buffer insertion should also take slew constraints into account.

18.1 Buffer Insertion in Large Circuits with Constructive Solution Search Techniques

Mandar Waghmode, Zhuo Li, Weiping Shi - *Texas A&M Univ., College Station, TX*

18.2 Low-Power Repeater Insertion with Both Delay and Slew Rate Constraints

Yuantao Peng, **Xun Liu** - *North Carolina State Univ., Raleigh, NC*

18.3 Fast Algorithms For Slew Constrained Minimum Cost Buffering

Shiyan Hu - *Texas A&M Univ., College Station, TX*
Charles J. Alpert - *IBM Corp., Austin, TX*
Jiang Hu - *Texas A&M Univ., College Station, TX*
Shrirang Karandikar - *IBM Corp., Austin, TX*
Zhuo Li, Weiping Shi - *Texas A&M Univ., College Station, TX*
C. N. Sze - *IBM Corp., Austin, TX*

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session of special interest to designers -
indicates videoed session -

Wednesday July 26, 2006

8:30 am - 10:00 am

SESSION 19

Rm: **304**

TESTING AND VALIDATION FOR TIMING DEFECTS

Chair: Cecilia Metra - *Univ. of Bologna, Bologna, Italy*
Organizers: Erik Jan Marinissen, Gordon Roberts

With increasing operation frequencies of ICs, testing and validation of timing defects are becoming more important and challenging.

19.1 A Flexible and Scalable Methodology for GHz-Speed Structural Test

Vikram Iyengar, Gary Grise, Mark Taylor, Rudy Farmer - *IBM Corp., Essex Junction, VT*

ß-19.2 Timing-Based Delay Test for Screening Small Delay Defects

Nisar Ahmed, **Mohammad Tehranipoor** - *Univ. of Maryland, Baltimore, MD*
Vinay Jayaram - *Texas Instruments Inc., Dallas, TX*

19.3 Hold Time Validation on Silicon and the Relevance of Hazards in Timing Analysis

Amit Majumdar - *Stratosphere Solutions, Inc., Sunnyvale, CA*
Wei-Yu Chen, Jun Guo - *Sun Microsystems, Inc., Sunnyvale, CA*

SESSION 20

Rm: **303**

ADVANCED TOPICS IN PROCESSOR AND SYSTEM VERIFICATION

Chair: Jon Michelson - *Cisco Systems, Inc., San Jose, CA*
Organizers: Avi Ziv, Harry Foster

The session presents four papers on dynamic verification and real-time fault detection in processors and systems-on-chip. The first two papers present various interesting aspects of successful verification of complex microprocessor (the Merom processor from Intel) and system-on-a-chip, (the Cell processor from Sony, Toshiba, IBM). The third paper describes methods for real-time detection and recovery from functional bugs, and the last paper deals with stimuli generation for a processor-based multimedia system-on-a-chip.

20.1 Practical Methods in Coverage-Oriented Verification of the Merom Microprocessor

Alon Gluska - *Intel Corp., Haifa, Israel*

20.2 Verification of the Cell Broadband Engine Processor

Kanna Shimizu, Sanjay Gupta - *IBM Corp., Austin, TX*
Tatsuya Koyama - *Sony Computer Entertainment Inc., Tokyo, Japan*
Takashi Omizo - *Toshiba Corp., Ohme, Japan*
Jamee Abdulhafiz - *IBM Corp., Austin, TX*
Yukio Watanabe - *Toshiba Corp., Kawasaki, Japan*
Larry McConville, Todd Swanson - *IBM Corp., Austin, TX*

20.3s Shielding Against Design Flaws with Field Repairable Control Logic

Ilya Wagner, Valeria Bertacco, Todd Austin - *Univ. of Michigan, Ann Arbor, MI*

20.4s Scheduling-based Test-case Generation for Verification of Multimedia SoCs

Amir Nahir, Avi Ziv - *IBM Corp., Haifa, Israel*
Roy Emek - *Consultant, Tel Aviv, Israel*
Nir Ronen, Tal Keidar - *Zoran Corp., Haifa, Israel*

SESSION 21

Rm: **301**

SOFTWARE FOR REAL-TIME APPLICATIONS

Chair: Mahmut Kandemir - *Pennsylvania State Univ., University Park, PA*
Organizers: Lothar Thiele, Vincent Mooney

Real-time applications stress power and execution time constraints. These papers address approaches for real-time estimation and optimization of power, worst-case execution time, and context switch costs. Novel techniques critical for embedded software will be presented with application scenarios and exciting results.

21.1 Rapid and Low-Cost Context-Switch through Embedded Processor Customization for Real-Time and Control Applications

Xiangrong Zhou, Peter D. Petrov - *Univ. of Maryland, College Park, MD*

21.2 Efficient Detection and Exploitation of Infeasible Paths for Software Timing Analysis

Ting Chen, Tulika Mitra, Abhik Roychoudhury, **Vivy Suhendra**, - *National Univ. of Singapore, Singapore*

21.3 Leakage-Aware Intraprogram Voltage Scaling for Embedded Processors

Po-Kuan Huang, Soheil Ghiasi - *Univ. of California, Davis, CA*

Wednesday July 26, 2006
10:30 am - 12:00 pm

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SESSION 22

Rm: **306/308**

PANEL: BUILDING A STANDARD ESL DESIGN AND VERIFICATION METHODOLOGY: IS IT JUST A DREAM?

Chair: Gary Smith - *Gartner DataQuest, San Jose, CA*
Organizer: Francine Bacchini

Industry cooperation established standards to support electronic system level (ESL) design and verification. But where is the common, standard ESL methodology itself? Leading ESL adopters devise their own custom methodologies, but is a standard ESL methodology — open to all — possible? ESL users and suppliers will look at what is being done today and debate the issues around what is needed.

Panelists:

Anoosh Hosseini - *Cisco Systems, Inc., Milpitas, CA*
Ashish Parikh - *PixelWorks, Inc., Campbell, CA*
Pascal Urard - *STMicroelectronics, Crolles Cedex, France*
Emil Girczyc - *Summit Design, Inc., Los Altos, CA*
Simon Bloch - *Mentor Graphics Corp., San Jose, CA*
H. Tony Chin - *HD Lab Inc., Yokohama, Japan*

SESSION 23

Rm: **307**

INVITED SESSION: CAD CHALLENGES FOR LEADING-EDGE MULTIMEDIA DESIGNS

Chair: Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*
Organizer: Andrew B. Kahng

Multimedia designs are among the most complex leading-edge integrated circuits that are made today. In this session, CAD architects for three industry-leading multimedia products will discuss new challenges that arise across the CAD flow – from system and architecture level through physical implementation – as we approach billion-transistor devices. The first talk will focus on system-level specification and codesign of embedded software for a multimedia processor. The second talk will discuss new time and space challenges for verification methodologies, which must be met to address the requirements of graphics processor time-to-market pressures. The third talk will discuss CAD challenges unique to a pioneering high-speed, multi-core processing engine for gaming and entertainment platforms.

23.1 Addressing the Challenge of Low Power, High Performance and Scalable Multimedia Acceleration in the Nomadik Processor
Patrick Blouet - *STMicroelectronics, Crolles, France*

23.2 Next-Generation Multimedia Designs: Verification Needs
Ira Chayut - *NVIDIA, Santa Clara, CA*

23.3 CAD Challenges for Designing a High Frequency Multi-Core SoC Implementation of a First-Generation CELL Processor
Dac Pham - *IBM Corp., Austin, TX*

SESSION 24

Rm: **305**

ROUTING

Chair: Dinesh Gaitonde - *Xilinx, Inc., Mountain View, CA*
Organizers: Patrick Groeneveld, Phiroze Parakh

The first paper in this session introduces a global router with significantly better solution quality. The second paper presents an efficient delay-update technique for network topologies. The third paper presents an innovative method for steiner tree construction via RC network-analysis. Finally, the fourth paper pesents a fast timing-driven steiner tree algorithm.

ß-24.1 BoxRouter: A New Global Router Based on Box Expansion and Progressive ILP
Minsik Cho, David Z. Pan - *Univ. of Texas, Austin, TX*

24.2 Steiner Network Construction for Timing Critical Nets
Shiyan Hu, Qiuyang Li, **Jiang Hu**, Peng Li - *Texas A&M Univ., College Station, TX*

24.3s Circuit Simulation Based Obstacle-Aware Steiner Routing
Yiyu Shi, Paul Mesa, Hao Yu, Lei He - *Univ. of California, Los Angeles, CA*

24.4s Timing-Driven Steiner Trees are (Practically) Free
Charles J. Alpert - *IBM Corp., Austin, TX*
Andrew B. Kahng - *Blaze DFM, Inc., Sunnyvale, CA*
C. N. Sze - *IBM Corp., Austin, TX*
Qinke Wang - *Univ. of California at San Diego, La Jolla, CA*

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Wednesday July 26, 2006
10:30 am - 12:00 pm

SESSION 25

Rm: **304**

THE TEST BIN

Chair: Roni Khazaka - *McGill Univ., Montreal, Canada*
Organizers: Cecilia Metra, Erik Jan Marinissen

The first paper is on software-based test for microprocessors. The second paper is on re-ordering test patterns to improve diagnostic resolution. The third paper proposes on-chip DFT for impedance matching of I/Os.

25.1 Systematic Software-Based Self-Test for Pipelined Processors

Mihalis Psarakis, Dimitris Gizopoulos, Miltiadis Hatzimihail - *Univ. of Piraeus, Piraeus, Greece*,
Antonis Paschalis - *Univ. of Athens, Athens, Greece*
Anand Raghunathan, Srivaths Ravi - *NEC Labs. America, Princeton, NJ*

25.2 A Test Pattern Ordering Algorithm for Diagnosis with Truncated Fail Data

Gang Chen, Sudhakar M. Reddy - *Univ. of Iowa, Iowa City, IA*
Irith Pomeranz - *Purdue Univ., West Lafayette, IN*
Janusz Rajski - *Mentor Graphics Corp., Wilsonville, OR*

25.3 DFT for Controlled-Impedance I/O Buffers

Ahmad Alyamani - *King Fahd Univ. of Petroleum and Minerals, Dhahran, Saudi Arabia*

SESSION 26

Rm: **303**

PANEL: VARIATION-AWARE ANALYSIS: SAVIOR OF THE NANOMETER ERA?

Chair: William H. Joyner, Jr. - *IBM Corp./SRC, Research Triangle Park, NC*
Organizer: Shishpal Rawat

VLSI engineers have traditionally used a variety of CAD analysis tools (e.g. SPICE) to deal with variability. As we go into deep sub micron issues, the analysis is becoming harder due to many secondary effects becoming primary. Panelists will debate the variability trend and present the order of importance of many variability trends (Vdd, Vt, Interconnect, Leff, Gate Width) and their impact on design tools and methodologies.

Panelists:

Vijay Pitchumani - *Intel Corp., Santa Clara, CA*
Clive D. Bittlestone - *Texas Instruments Inc., Dallas, TX*
Sani R. Nassif - *IBM Corp., Austin, TX*
Norma Rodriquez - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*
Riko Radojcic - *Qualcomm CDMA Technologies, San Diego, CA*

SESSION 27

Rm: **301**

LOW POWER AND ULTRA-LOW VOLTAGE DESIGN

Chair: Chris Kim - *Univ. of Minnesota, Minneapolis, MN*
Organizers: Diana Marculescu, Trevor Mudge

This session covers topics related to physical leakage models, subthreshold circuit design, and low power voltage assignment.

27.1 A Fully Physical Model for Leakage Distribution under Process Variations in Nanoscale Double-Gate CMOS

Hari Ananthan, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

27.2 A PLA Based Asynchronous Micropipelining Approach for Subthreshold Circuit Design

Nikhil Jayakumar, Rajesh Garg - *Texas A&M Univ., College Station, TX*
Bruce Gamache - *Univ. of Colorado, Boulder, CO*
Sunil Khatri - *Texas A&M Univ., College Station, TX*

27.3s Subthreshold Logical Effort: A Systematic Framework for Optimal Subthreshold Device Sizing

John Keane, Tae-Hyoung Kim, Hanyong Eom, Sachin Sapatnekar, Chris Kim - *Univ. of Minnesota, Minneapolis, MN*

27.4s Timing-Constrained and Voltage-Island-Aware Voltage Assignment

Huaizhi Wu - *Cadence Design Systems, Inc., San Jose, CA*
Martin D.F. Wong - *Univ. of Illinois, Urbana-Champaign, Urbana , IL*
I-Min Liu - *Atoptech, Inc., Santa Clara, CA*

Wednesday July 26, 2006
2:00 pm - 4:00 pm

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SESSION 28

Rm: **306/308**

HIGH-LEVEL EXPLORATION AND OPTIMIZATION

Chair: Rishiyur S. Nikhil - *Bluespec, Inc., Waltham, MA*
Organizers: Reinaldo Bergamaschi, Rishiyur S. Nikhil

This session presents five papers which advance the state-of-the-art in high-level synthesis optimization and design space exploration. The first paper presents a new scheduling formulation based on a system of difference constraints. The second paper presents a novel approach for considering clock skew during high-level synthesis. The third and fourth paper present efficient design exploration approaches for high-level design, and the fifth paper presents a method for fast estimation of controller delay from high-level specifications.

28.1 An Efficient and Versatile Scheduling Algorithm Based On SDC Formulation
Jason Cong, **Zhiru Zhang** - *Univ. of California, Los Angeles, CA*

ß-**28.2 Register Binding for Clock Period Minimization**
Shih-Hsu Huang, Chun-Hua Cheng, Yow-Tyng Nieh, Wei-Chieh Yu - *Chung Yuan Christian Univ., Chung Li, Taiwan*

28.3 Towards Automatic Exploration of Arithmetic Circuit Architectures
Ajay K. Verma, **Paolo Ienne** - *EPFL, Lausanne, Switzerland*

28.4s Design Space Exploration Using Time and Resource Duality with the Ant Colony Optimization
Gang Wang, Wenrui Gong, Brian DeRenzi, Ryan Kastner - *Univ. of California, Santa Barbara, CA*

28.5s Rapid Estimation of Control Delay from High-Level Specifications
Gagan R. Gupta - *Univ. of Wisconsin, Madison, WI*
Madhur Gupta - *Purdue Univ., West Lafayette, IN*
Preeti R. Panda- *Indian Institute of Tech., New Delhi, India*

SESSION 29

Rm: **307**

PANEL: DESIGN CHALLENGES FOR NEXT-GENERATION MULTIMEDIA, GAME AND ENTERTAINMENT PLATFORMS

Chair: Bryan Lewis - *Gartner Dataquest, San Jose, CA*
Organizer: Andrew B. Kahng

Multimedia, game, and entertainment devices have pushed the leading edge of performance, complexity, power, form-factor, design cycle time, and other key aspects of ASIC design for the past several technology nodes. This panel brings together experts who are defining the next generation of gaming, mobile TV, digital home, display, and multimedia processing platforms, to answer such questions as:

- What are the underlying chip architectures and roadmaps for key multimedia/entertainment platforms?
- What are the key design and technology challenges (or "brick walls") for next-generation products, and how will these challenges be addressed?
- What other challenges arise from complex supplier/competitor relationships, standards, and other aspects of a globalized market?
- Where will we see the next "convergence" in devices and platforms?

The panelists will also present insights into other aspects of today's multimedia/entertainment platforms: CAD and design methodologies, design enablement (compilers, programming models, etc.), design for IP reuse (configurability, derivatives), and IP management in a world of "co-opetition".

Panelists:

John Cohn - *IBM Corp., Essex Junction, VT*
Chris Malachowsky - *NVIDIA Corp., Santa Clara, CA*
Richard Tobias - *Pixelworks, Inc., Campbell, CA*
Jeong-Taek Kong, Sr. - *Samsung Electronics Co., Ltd., Giheung, Korea*
Brendan Traw - *Intel Corp., Hillsboro, OR*

SESSION 30

Rm: **305**

CAD FOR FPGAS

Chair: William N.N. Hung - *Synplicity, Inc., Sunnyvale, CA*
Organizers: Bill Halpin, Steven Teig

FPGAs have relied on computer-aided design techniques for logic synthesis and physical design since their inception. This session provides novel design tools and methods for solving these "traditional" problem areas, including retiming, clustering, technology mapping and placement.

ß-**30.1 Architecture-Aware FPGA Placement Using Metric Embedding**
Padmini Gopalakrishnan, Xin Li, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

30.2 Efficient SAT-based Boolean Matching for FPGA Technology Mapping
Sean A. Safarpour - *Univ. of Toronto, Toronto, ON, Canada*
Gregg Baeckler, Richard Yuan - *Altera Corp., San Jose, CA*
Andreas Veneris - *Univ. of Toronto, Toronto, ON, Canada*

30.3 Optimal Simultaneous Mapping and Clustering for FPGA Delay Optimization
Joey Y. Lin - *Magma Design Automation, Inc., Los Angeles, CA*
Deming Chen - *Univ. of Illinois, Urbana, IL*
Jason Cong - *Univ. of California, Los Angeles, CA*

30.4 Simultaneous Time Slack Budgeting and Retiming for Dual-Vdd FPGA Power Reduction
Yu Hu, Yan Lin, Lei He - *Univ. of California, Los Angeles, CA*
Tim Tuan - *Xilinx Corp., San Jose, CA*

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Wednesday July 26, 2006

2:00 pm - 4:00 pm

SESSION 31

Rm: **304**

SECURE SYSTEMS

Chair: Catherine Gebotys - *Univ. of Waterloo, Waterloo, Canada*
Organizers: Pai Chou, Peter Marwedel

The papers in this session address a critical area in system design: security. VIRTUS enables security through processor virtualization. Network security processor design gives flexibility and scalability for cryptographic functions. A methodology for exploring the security processing software architecture on SoCs is the topic of the third paper. IMPRES presents a HW/SW technique for improving processor security and reliability. Ciphering and integrity checking of data exchanged between a SoC and its external memory is the addressed in the last paper.

ß- **31.1 VIRTUS: A New Processor Virtualization Architecture for Security-Oriented Next-Generation Mobile Terminals**
Hiroaki Inoue - *NEC Corp., Sagamihara, Japan*
Akihisa Ikeno, Masaki Kondo - *NEC Informatec Systems, Ltd., Kawasaki, Japan*
Junji Sakai, Masato Edahiro - *NEC Corp., Sagamihara, Japan*

31.2 A Network Security Processor Design Based on an Integrated SoC Design and Test Platform
Chen-Hsing Wang, Chih-Yen Lo, Min-Sheng lee, Jen-Chieh Yeh, Chih-Tsun Huang, Cheng-Wen Wu - *National Tsing-Hua Univ., Hsinchu, Taiwan*

31.3 Software Architecture Exploration for High-Performance Security Processing on a Multiprocessor Mobile SoC
Divya Arora - *Princeton Univ., Princeton, NJ*
Srivaths Ravi, Anand Raghunathan, Murugan Sankaradass - *NEC-Labs America, Princeton, NJ*
Niraj Jha - *Princeton Univ., Princeton, NJ*
Srimat T. Chakradhar - *NEC-Labs America, Princeton, NJ*

31.4s IMPRES: Integrated Monitoring for Processor REliability and Security
Roshan G. Ragel - *Univ. of New South Wales, Sydney, Australia*
Sridevan Parameswaran - *Univ. of New South Wales, Kensington, Australia*

31.5s A Parallelized Way to Provide Data Encryption and Integrity Checking on a Processor-Memory Bus
Reouven Elbaz - *LIRMM/STMicroelectronics, Montpellier, France*
Lionel Torres, Gilles Sassatelli - *LIRMM, Montpellier, France*
Pierre Guillemin, Michel Bardouillet, Albert Martinez - *STMicroelectronics, Rousset, France*

SESSION 32

Rm: **303**

LOGIC SYNTHESIS I

Chair: Davide Pandini - *STMicroelectronics, Milano, Italy*
Organizers: James Hoe, Rajeev Murgai

This session presents new ideas in combinational logic synthesis. It offers a fresh look at classical topics such as symmetry detection, boolean matching, and rewriting-based logic optimization. It also visits emerging areas such as gate sizing for finFETs and technology mapping for leakage current.

32.1 Symmetry Detection for Large Boolean Functions Using Circuit Representation, Simulation and Satisfiability
Jin S. Zhang - *Portland State Univ., Portland, OR*
Alan Mishchenco, Robert Brayton - *Univ. of California, Berkeley, CA*,
Malgorzata Chrzanowska-Jeske - *Portland State Univ., Portland, OR*

32.2 Exploiting K-Distance Signature for Boolean Matching and G-Symmetry Detection
Kuo-Hua Wang - *Fu Jen Catholic Univ., Taipei, Taiwan*

32.3 Gain-Based Technology Mapping for Minimum Runtime Leakage under Input Vector Uncertainty
Ashish K. Singh, Murari Mani - *Univ. of Texas, Austin, TX*
Ruchir Puri - *IBM Corp., Yorktown Heights, NY*
Michael Orshansky - *Univ. of Texas, Austin, TX*

32.4s Gate Sizing for FinFETs vs 32nm Bulk MOSFETS
Brian G. Swahn, Soha Hassoun - *Tufts Univ., Medford, MA*

32.5s DAG-Aware AIG Rewriting: A Fresh Look at Combinational Logic Synthesis
Alan Mishchenko, Satrajit Chatterjee, Robert K. Brayton - *Univ. of California, Berkeley, CA*

SESSION 33

Rm: **301**

LOW-POWER, THERMAL-AWARE ARCHITECTURES

Chair: Kevin Skadron - *Univ. of Virginia, Charlottsville, VA*
Organizers: Diana Marculescu, Naehyuck Chang

This session covers topics related to energy aware architectures for OFDM transmitter design and control, and low power hearing aid design, as well as thermal management and energy estimation at architecture level.

33.1 Energy-Scalable OFDM Transmitter Design and Control
Björn Debaillie, Bruno Bougard, Gregory Lenoir, Gerd Vandersteen, Francky Catthoor - *IMEC, Leuven, Belgium*

33.2 Systematic Temperature Sensor Allocation and Placement for Microprocessors
Rajarshi Mukherjee, Seda Ogrenci Memik - *Northwestern Univ., Evanston, IL*

33.3 HybDTM: A Coordinated Hardware-Software Approach for Dynamic Thermal Management
Amit Kumar - *Princeton Univ., Princeton, NJ*
Li Shang - *Queen's Univ., Kingston, ON, Canada*
Li-Shiuan Peh, Niraj K. Jha - *Princeton Univ., Princeton, NJ*

33.4s A Systematic Method For Functional Unit Power Estimation in Microprocessors
Wei Wu, Lingling Jin, Jun Yang, Pu Liu, Sheldon X.-D. Tan - *Univ. of California, Riverside, CA*

33.5s Low-Power Architectural Tradeoffs in a VLSI Implementation of an Adaptive Hearing Aid Algorithm
Felix Buergin, Flavio Carbognani, Martin Hediger, Hektor Meier, Robert Meyer-Piening, Rafael Santschi, Norbert Felber, Hubert Kaeslin, Wolfgang Fichtner - *ETH Zurich, Zurich, Switzerland*

Wednesday July 26, 2006
4:30 pm - 6:30 pm

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SESSION 34

Rm: **306/308**

LOW POWER SYSTEM LEVEL DESIGN

Chair: Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*
Organizers: Diana Marculescu, Sanu Mathew

This session addresses topics related to low power system level design, ranging from extending the lifetime of fuel cell-based systems and power management, to network-on-chip based architectures and multi-Vdd systems.

34.1 Extending the Lifetime of Fuel Cell Based Hybrid Systems

Jianli Zhuo, Chaitali Chakrabarti - *Arizona State Univ., Tempe, AZ*
Naehyuck Chang - *Seoul National Univ., Seoul, South Korea*
Sarma Vrudhula - *Arizona State Univ., Tempe, AZ*

34.2 High-Level Power Management of Embedded Systems with Application-Specific Energy Cost Functions

Youngjin Cho, Naehyuck Chang - *Seoul National Univ., Seoul, South Korea*
Chaitali Chakrabarti, Sarma Vrudhula - *Arizona State Univ., Tempe, AZ*

34.3 Communication Latency Aware Low Power NoC Synthesis

Yuanfang Hu, Yi Zhu - *Univ. of California at San Diego, La Jolla, CA*
Hongyu Chen - *Synopsys, Inc., Mountain View, CA*
Ronald Graham, Chung-Kuan Cheng - *Univ. of California at San Diego, La Jolla, CA*

34.4 Optimal Study of Resource Binding with Multi-Vdds

Deming Chen - *Univ. of Illinois, Urbana, IL*
Jason Cong, Yiping Fan - *Univ. of California, Los Angeles, CA*
Junjuan Xu - *Peking Univ., Beijing, China*

SESSION 35

Rm: **307**

POWER-CONSTRAINED DESIGN FOR MULTIMEDIA

Chair: Richard Tobias - *PixelWorks, Campbell, CA*
Organizers: Andrew B. Kahng, John Cohn

This session presents a variety of design objectives and design solutions related to power constraints for multimedia applications. The first paper addresses energy-efficient messaging. The next paper offers new approaches to dynamic voltage and frequency scaling-based energy saving for multimedia systems: the second paper uses signature-based workload estimation, and the third paper applies DVFS in the context of gaming systems. The session closes with two short papers on design techniques for power minimization in mobile displays.

35.1 SMERT: Energy-Efficient Design of a Multimedia Messaging System for Mobile Devices

Lin Zhong - *Rice Univ., Houston, TX*
Bin Wei - *AT&T Labs, Florham Park, NJ*
Mike Sinclair - *Microsoft Research, Redmond, WA*

35.2 Signature-Based Workload Estimation for Mobile 3D Graphics

Bren C. Mochocki - *Univ. of Notre Dame, Notre Dame, NJ*
Srihari Cadambi, Kanishka Lahiri - *NEC-Labs America, Princeton, NJ,*
Xiaobo S. Hu - *Univ. of Notre Dame, Notre Dame, IN*

35.3 Games are Up for DVFS

Yan Gu, Samarjit Chakraborty, Wei Tsang Ooi - *National Univ. of Singapore, Singapore*

35.4s Power Aware Mobile Display

Ali Iranli, Wonbok Lee, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

35.5s Power Minimization for LED-backlit TFT-LCDs

Wei-Chung Cheng - *National Chiao Tung Univ., Hsinchu, Taiwan*

SESSION 36

Rm: **305**

ELECTRICAL AND THERMAL ISSUES IN FPGAS

Chair: Rajeev Jayaraman - *Xilinx, Inc., San Jose, CA*
Organizers: Patrick Lysaght, Ryan Kastner

This session will explore a variety of electrical and thermal issues in deep nanometer FPGAs. The papers present new algorithms and architectures to reduce leakage power in embedded memories, reduce thermal emulation runtimes, reduce leakage due to process variation, and analyze the degradation of FPGAs caused by hot carrier effects.

36.1 Leakage Power Reduction of Embedded Memories on FPGAs Through Location Assignment

Yan Meng, Timothy Sherwood, Ryan Kastner - *Univ. of California, Santa Barbara, CA*

36.2 A Fast HW/SW FPGA-Based Thermal Emulation Framework for Multi-Processor System-on-Chip

David Atienza, Pablo G. Del Valle - *DACYA/UCM, Madrid, Spain*
Giacomo Paci, Francesco Poletti, Luca Benini - *DEIS/Univ. of Bologna, Bologna, Italy*
Giovanni De Micheli - *LSI/EPFL, Lausanne, Switzerland*
Jose M. Mendias - *DACYA/UCM, Madrid, Spain*

36.3 An Adaptive FPGA Architecture with Process Variation Compensation and Reduced Leakage

Georges Nabaa - *Actel Corp., Mountain View, CA*
Navid Azizi, Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*

36.4 FLAW: FPGA Lifetime AWareness

Suresh Srinivasan, Prasanth Mangalagiri, Karthik Sarpatwari, Yuan Xie, Vijaykrishnan Narayanan - *Pennsylvania State Univ., University Park, PA*

All speakers are denoted in bold
denotes short paper - S
denotes best paper candidate - ß
session of special interest to designers -
indicates videoed session -

Wednesday July 26, 2006
4:30 pm - 6:30 pm

SESSION 37

Rm: **304**

SPECIAL SESSION: BEYOND LOW-POWER DESIGN: ENVIRONMENTAL ENERGY HARVESTING

Chair: Kaushik Roy - *Purdue Univ., West Lafayette, IN*
Organizers: Pai Chou, Vijay Raghunathan

This session will feature renowned experts in the field of energy harvesting who will provide a comprehensive treatment of the area, drawing from state-of-the-art practice and emerging research directions at all levels of design abstraction including materials/devices, circuits, systems, and architecture/design. Environmental energy harvesting has emerged as a promising technique to enable near-perpetual system operation in several emerging applications (e.g., human bio-implants, ambient intelligence, wireless sensor networks). Further, it mitigates the cost and environmental impact of battery replacement and disposal. The session will cover all aspects of designing and optimizing an environmental energy harvesting system in a bottom-up manner, starting from devices/materials, circuits, systems/architecture, and finally harvesting aware system-level power management policies.

37.1 Solution Processed Infrared Photovoltaic Devices

Edward H. Sargent, **Dean D. MacNeil** - *Univ. of Toronto, Toronto, ON, Canada*

37.2 Circuits for Energy Harvesting Sensor Signal Processing

Rajeevan Amirtharajah - *Univ.of California, Davis, CA*
Jamie Collier - *Boston Scientific, Arden Hills, MN*
Jeff Siebert - *Intel Corp., Folsom, CA,*
Justin Wenck - *Univ. of California, Davis, CA*
Bicky Zhou - *Intel Corp., Santa Clara, CA*

37.3 Systems for Human Powered Mobile Computing

Joseph Paradiso - *Massachusetts Institute of Tech., Cambridge, MA*

37.4 Harvesting Aware Power Management for Sensor Networks

Aman Kansal, Jason Hsu, **Mani Srivastava**- *Univ. of California, Los Angeles, CA*
Vijay Raghunathan - *NEC-Labs America, Princeton, NJ*

SESSION 38

Rm: **303**

COMMUNICATION-DRIVEN SYNTHESIS

Chair: Luca Carloni - *Columbia Univ., New York, NY*
Organizer: Stephen Edwards

On-chip communication is ubiquituous and more challenging as chips get larger. The papers in this session address the problem of synthesizing more efficient, delay-tolerant communication structures.

38.1 Synthesis of Synchronous Elastic Architectures

Jordi Cortadella - *Universitat Politécnica de Catalunya, Barcelona, Spain*
Michael Kishinevsky, Bill Grundmann - *Intel Corp., Hillsboro, OR*

38.2 Statistical On-Chip Communication Bus Synthesis and Voltage Scaling Under Timing Yield Constraint

Sujan Pandey, Manfred Glesner - *Darmstadt Univ. of Tech., Darmstadt, Germany*

38.3 Optimization of Area under a Delay Constraint in Digital Filter Synthesis Using SAT-Based Integer Linear Programming

Levent Aksoy - *Istanbul Tech. Univ., Istanbul, Turkey*
Eduardo C. Costa - *Univ. Católica de Pelotas, Pelotas, Brazil*
Paulo Flores, Jose Monteiro - *INESC - ID / IST, Lisbon, Portugal*

38.4s Behavior and Communication Co-Optimization for Systems with Sequential Communication Media

Jason Cong, Yiping Fan, Guoling Han, **Wei Jiang**, Zhiru Zhang - *Univ. of California, Los Angeles, CA*

38.5s Synthesis of High-Performance Packet Processing Pipelines

Cristian Soviani - *Columbia Univ., New York, NY*
Ilija Hadzic - *Lucent Technologies, Murray Hill, NJ*
Stephen A. Edwards - *Columbia Univ., New York, NY*

SESSION 39

Rm: **301**

PARALLELISM AND MEMORY OPTIMIZATIONS

Chair: Steven Tjiang - *Google, Mountain View, CA*
Organizers: Steven Tjiang, Vincent Mooney

With the emergence of chip multiprocessors, parallelism and memory optimizations become critical for efficient deployment of embedded software. Broadly speaking, memory issues cross the software/hardware boundary, and so several papers in this session address memory optimization from the software and hardware perspectives. Novel and interesting techniques will pique the attendees' interests in this session.

ß-39.1 A Constraint Network Based Solution to Code Parallelization

Ozcan Ozturk, Guilin Chen, **Mahmut Kandemir**- *Pennsylvania State Univ., University Park, PA*

39.2 Buffer Memory Optimization for Video Codec Application Modeled in Simulink

Sang-Il Han - *Seoul National Univ., Seoul, South Korea*
Xavier Guerin - *TIMA Lab, Grenoble, France*
Soo-Ik Chae - *Seoul National Univ., Seoul, South Korea*
Ahmed A. Jerraya - *TIMA Lab, Grenoble, France*

39.3 Configurable Cache Subsetting for Fast Cache Tuning

Pablo Viana - *UFPE, Recife, Brazil*
Ann Gordon-Ross, Eamonn Keogh, Frank Vahid - *Univ. of California, Riverside, CA*
Edna Barros - *UFPE, Recife, Brazil*

39.4s High-Performance Operating System Controlled Memory Compression

Lei Yang - *Northwestern Univ., Evanston, IL*
Haris Lekatsas - *NEC-Labs America, Princeton, NJ*
Robert P. Dick - *Northwestern Univ., Evanston, IL*

39.5s A Cost-Effective Implementation of an ECC-Protected Instruction Queue for Out-of-Order Microprocessors

Vladimir Stojanovic, Iris Bahar, **Jennifer L. Dworak** - *Brown Univ., Providence, RI,*
Richard Weiss - *Evergreen State College, Olympia, WA*

Thursday July 27, 2006
8:30 am - 10:00 am

All speakers are denoted in bold
S - denotes short paper
ß - denotes best paper candidate
- session of special interest to designers
- indicates videoed session

SESSION 40

Rm: **306/308**

PANEL: TOMORROW'S ANALOG: JUST DEAD OR JUST DIFFERENT?

Chair: Georges Gielen - *Katholieke Univ., Leuven, Belgium*
Organizer: Rob A. Rutenbar

With the ongoing trend towards more and more digitization in applications ranging from multimedia to telecommunications, there is a big debate about whether there will remain a need for analog circuits in scaled technologies. Analog circuits do not seem to take advantage of nanometer CMOS; rather they suffer from it. So if the question is asked, "Will analog scale?", you get conflicting opinions. One camp argues for an almost-all-digital future. Analog/RF content should be limited, because it's difficult, expensive, risky, and can be done with DSP. The opposing camp counters that some critical circuits simply do not want (or need) to scale, and analog is only "risky" when you let digital designers do it. So, what is the future role of analog circuits in scaled CMOS, and can analog EDA tools help in this?

Panelists:

Shekhar Y. Borkar - *Intel Corp., Hillsboro, OR*
Charles G. Sodini - *Massachusetts Institute of Tech., Cambridge, MA*
Daniel Saias - *STMicroelectronics, Crolles Cedex, France*
Eric Naviasky - *Cadence Design Systems, Inc., San Jose, CA*
Robert W. Brodersen - *Univ. of California, Berkeley, CA*
Jue-Hsien Chern - *Mentor Graphics Corp., Wilsonville, OR*

SESSION 41

Rm: **307**

NANOTUBES AND NANOWIRES

Chair: Sankar Basu - *NSF, Arlington, VA*
Organizers: Igor L. Markov, Krishnendu Chakrabarty

Nanotechnology holds promise for higher device densities and lower fabrication costs. This session covers analysis of ballistic CNFETs, design of reconfigurable nano-CMOS, as well as crossbar-based nano-FPGAs.

41.1 NATURE: A Hybrid Nanotube/CMOS Dynamically Reconfigurable Architecture
Wei Zhang, Niraj K. Jha - *Princeton Univ., Princeton, NJ*
Li Shang - *Queen's Univ., Kingston, ON, Canada*

41.2 Modeling and Analysis of Circuit Performance of Ballistic CNFET
Bipul C. Paul - *Stanford Univ., Stanford, CA*
Shinobu Fujita, Masaki Okajima - *Toshiba Corp., San Jose, CA*
Thomas Lee - *Stanford Univ., Stanford, CA*

41.3s Topology Aware Mapping of Logic Functions onto Nanowire-based Crossbar Architectures
Wenjing Rao, Alex Orailoglu - *Univ. of California at San Diego, La Jolla, CA*
Ramesh Karri - *Polytechnic Univ., Brooklyn, NY*

41.4s A New Hybrid FPGA With Nanoscale Clusters and CMOS Routing
Reza M. Rad, **Mohammad Tehranipoor** - *Univ. of Maryland, Baltimore, MD*

SESSION 42

Rm: **305**

SIMULATION ASSISTED FORMAL VERIFICATION

Chair: Andrew Piziali - *Cadence Design Systems, Inc., Parker, TX*
Organizers: Harry Foster, Richard Ho

The papers in this session utilize simulation to improve the results of formal verification, both for model checking and for equivalence checking. One paper explores the verification of a serial protocol and bridge, one paper describes a technique for finding very long counter-examples (bugs) and our final paper utilizes simulation and data mining techniques to discover global constraints that can be used in a number of applications.

42.1 Directed-Simulation Assisted Formal Verification of Serial Protocol and Bridge
Saurav Gorai - *Mentor Graphics Corp., Noida, India*
Saptarshi Biswas, Lovleen Bhatia, Praveen Tiwari, **Raj S. Mitra** - *Texas Instruments Inc., Bangalore, India*

42.2 Guiding Simulation with Increasingly Refined Abstract Traces
Kuntal V. Nanshi, Fabio Somenzi - *Univ. of Colorado, Boulder, CO*

42.3 Mining Global Constraints for Improving Bounded Sequential Equivalence Checking
Weixin Wu, Michael Hsiao - *Virginia Tech., Blacksburg, VA*

All speakers are denoted in bold
denotes short paper - S
denotes best paper candidate - ß
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Thursday July 27, 2006

8:30 am - 10:00 am

SESSION 43

Rm: **304**

YIELD ANALYSIS AND IMPROVEMENT

Chair: Evanthia Papadopoulou - *IBM Corp., Yorktown Heights, NY*

Organizers: Fook-Luen Heng, Patrick Groeneveld

Yield analysis and improvement have gained more attention due to new defect mechanisms in the nano-technology era. The first paper is an early attempt to derive a mathematical model to predict yield based on process information. The second paper addresses double via insertion during the routing phase. The third paper solves the antenna avoidance problem by considering the actual antenna ratio constraint.

43.1 An IC Manufacturing Yield Model Considering Intra-Die Variations

Jianfeng Luo, Subarna Sinha, Qing Su, Jamil Kawa, Charles Chiang - *Synopsys, Inc., Mountain View, CA*

43.2 Novel Full-Chip Gridless Routing Considering Double-Via Insertion

Huang-Yu Chen, Mei-Fang Chiang, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*, Lumdo Chen, Brian Han - *UMC, Hsinchu Science Park, Taiwan*

43.3 Optimal Jumper Insertion for Antenna Avoidance under Ratio Upper-Bound

Jia Wang, Hai Zhou - *Northwestern Univ., Evanston, IL*

SESSION 44

Rm: **303**

APPROACHES TO SOFT ERROR MITIGATION

Chair: Subashish Mitra - *Stanford Univ., Stanford, CA*

Organizers: Dennis Sylvester, Haihua Su

This session describes new approaches to reducing soft error rates in modern ICs, particularly in combinational logic, but also in memory structures. The first paper details a symbolic framework to analyze error susceptibility that then drives selective gate sizing to harden the circuit with limited overheads. The second paper incorporates shadow gates on highly critical gates to achieve radiation hardening with acceptable area and delay penalties. The final paper proposes new content-addressable memory structures to achieve soft error rate improvements.

44.1 MARS-C: Modeling and Reduction of Soft Errors in Combinational Circuits

Natasa Miskov-Zivanov, Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

44.2 A Design Approach for Radiation-Hard Digital Electronics

Rajesh Garg, Nikhil Jayakumar, Sunil P. Khatri, Gwan Choi - *Texas A&M Univ., College Station, TX*

44.3 A Family of Cells to Reduce the Soft-Error-Rate in Ternary-CAM

Navid Azizi, Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*

SESSION 45

Rm: **301**

DESIGN/TECHNOLOGY INTERACTION

Chair: Jerry D. Hayes - *IBM Corp., Essex Junction, VT*

Organizer: Sani R. Nassif

Technology scaling has drastically exacerbated the complexity and amount of data required to achieve productive design/technology interaction. This session shows examples of the excellent work going on in the DFM community on ensuring the best possible coupling between the design and fabrication phases.

45.1 Process Variation Aware OPC with Variational Lithography Modeling

Peng Yu, Sean X. Shi, David Z. Pan - *Univ. of Texas, Austin, TX*

45.2 Modeling of Intra-die Process Variations for Accurate Analysis and Optimization of Nano-scale Circuits

Sarvesh Bhardwaj, Sarma Vrudhula, Praveen Ghanta, Yu Cao - *Arizona State Univ., Tempe, AZ*

45.3s Computation of Accurate Interconnect Process Parameter Values for Performance Corners under Process Variations

Frank Huebbers - *Northwestern Univ., Evanston, IL*
Ali Dasdan - *Yahoo, Sunnyvale, CA*
Yehea Ismail - *Northwestern Univ., Evanston, IL*

45.4s Standard Cell Characterization Considering Lithography Induced Variations

Ke Cao, Sorin Dobre - *Qualcomm Inc., San Diego, CA*
Jiang Hu - *Texas A&M Univ., College Station, TX*

Thursday July 27, 2006
10:30 am - 12:00 pm

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S - denotes short paper
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SESSION 46

Rm: **306/308**

PANEL: BUILDING A VERIFICATION TEST PLAN: TRADING BRUTE FORCE FOR FINESSE

Chair: Sharad Malik - *Princeton Univ., Princeton, NJ*
Organizer: Francine Bacchini

The pain of functional verification is intensifying. Building the right verification test plan can reduce this pain – trading brute force for finesse – while enabling greater predictability, more aggressive innovation and late stage spec changes made with confidence. Users and suppliers debate the optimal mix of formal, simulation, hardware acceleration and emulation, examining ways to ensure new features aren't dropped pre-tapeout from "inadequate verification".

Panelists:

Doron Stein - *Cisco Systems, Inc., Netanya, Israel*
Raj S. Mitra - *Texas Instruments Inc., Bangalore, India*
Janick Bergeron - *Synopsys, Inc., Ottawa, ON, Canada*
Harry D. Foster - *Mentor Graphics Corp., Addison, TX*
Andrew Piziali - *Cadence Design Systems, Inc., Parker, TX*
Catherine Ahlschlager - *Sun Microsystems, Inc., Sunnyvale, CA*

SESSION 47

Rm: **307**

SPECIAL SESSION: MORE MOORE'S LAW AND MORE THAN MOORE'S LAW

Chair: Igor L. Markov - *Univ. of Michigan, Ann Arbor, MI*
Organizers: Krishnendu Chakrabarty, Niraj Jha

This session presents a roadmap for nanoscale CMOS (more Moore's Law) as well as emerging nanoelectronics technologies that offer alternatives to CMOS (more than Moore's Law). The session starts with an industry perspective on mainstream and near-term CMOS technologies. This is followed by an academic perspective on carbon nanotube interconnects. The last talk in this session will present new developments in the design of nonvolatile memories.

47.1 Electronics Beyond Nano-scale CMOS

Shekhar Y. Borkar - *Intel Corp., Hillsboro, OR*

47.2 Are Carbon Nanotubes the Future of VLSI Interconnections?

Kaustav Banerjee, Navin Srivastava - *Univ. of California, Santa Barbara, CA*

47.3 The Zen of Nonvolatile Memories

Erwin Prinz - *Freescale Semiconductor, Inc., Austin, TX*

SESSION 48

Rm: **305**

FORMAL SPECIFICATION AND VERIFICATION TESTBENCH GENERATION

Chair: Michael Theobald - *D.E. Shaw Research, New York, NY*
Organizers: Alan Hu, Erich Marschner

Formal verification today typically involves verification of a design with respect to its specification. This session presents formal methods applied to earlier stages of the verification process, including formal methods for investigating the quality of a specification, and for generating testbenches from a specification.

48.1 Formal Analysis of Hardware Requirements

Ingo Pill - *Graz Univ. of Tech., Graz, Austria*
Simone Semprini, Roberto Cavada, Marco Roveri, - *ITC Irst, Povo, Italy*
Roderick Bloem - *Graz Univ. of Tech., Graz, Austria*
Alessandro Cimatti - *ITC Irst, Povo, Italy*

48.2 Cancelled

48.3 Test Generation Games from Formal Specifications (start time: 11:00 am)

Ansuman Banerjee, Bhaskar Pal, Sayantan Das, Abhijeet Kumar, Pallab Dasgupta - *Indian Institute of Tech., Kharagpur, India*

All speakers are denoted in bold
denotes short paper - S
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Thursday July 27, 2006
10:30 am - 12:00 pm

SESSION 49

Rm: **304**

ANALYSIS AND OPTIMIZATION ISSUES IN NoC DESIGN

Chair: Petru Eles - *Linkoping Univ., Linkoping, Sweden*
Organizers: Joerg Henkel, Radu Marculescu

Networks-on-Chip (NoCs) is one of the promising solutions for future multi-billion MPSoCs. To design such systems, the optimization of the communication infrastructure plays a crucial role. The papers selected for this session cover a broad range of techniques and optimization metrics which can support various communication scenarios. The first two papers improve the on-chip network performance by keeping the resource utilization low. More precisely, link scheduling and flow-control are exploited as means to optimize the overall network behavior. The last two papers present novel on-chip routing techniques which are meant to improve the resource utilization and provide support for fault-tolerant operation in presence of transient and permanent faults. By attending this session, the audience will get a deep insight into the most stringent issues in communication-centric design that system designers have to deal with in tomorrow's complex MPSoCs.

49.1 Optimal Link Scheduling on Improving Best-Effort and Guaranteed Services Performance in Network-on-Chip System
Lap Fai Leung, Chi Ying Tsui - *Hong Kong Univ. of Science & Tech., Hong Kong, Hong Kong*

49.2 Prediction-based Flow Control for Networks-on-Chip Traffic
Umit Y. Ogras, Radu Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

49.3s A Multi-Path Routing Strategy with Guaranteed In-Order Packet Delivery and Fault-Tolerance for Networks on Chip
Srinivasan Murali - *Stanford Univ., Stanford, CA*
David Atienza Alonso - *LSI-EPFL, Lausanne, Switzerland*
Luca Benini - *Univ. of Bologna, Bologna, Italy*
Giovanni De Micheli - *EPFL, Lausanne, Switzerland*

49.4s DyXY - A Proximity Congestion-Aware Deadlock-Free Dynamic Routing Method for Network-on-Chip
Ming Li, Qing-An Zeng, **Wen-Ben Jone**- *Univ. of Cincinnati, Cincinnati, OH*

SESSION 50

Rm: **303**

SPECIAL SESSION: KEY TECHNOLOGIES FOR BEYOND THE DIE

Chair: Mike Heimlich - *Applied Wave Research, Pelham, NH*
Organizer: Lei He

SIP (system-in-package) may reduce costs compared to SoC for heterogeneous integration. The first two papers discuss package-aware SoC design and system integration using silicon as carrier. The next two papers present high-speed links between chips in CMOS and optical technologies, respectively.

50.1 The Importance of Adopting a Package-Aware Chip Design Flow
Kaushik Sheth, Egino Sarto, Joel McGrath - *Rio Design Automation, Inc., Santa Clara, CA*

50.2 Silicon Carrier for Computer Systems
Chirag Patel - *IBM Corp., Yorktown Heights, NY*

50.3s 4.25 GB/S Laser Driver: Design Challenges and EDA Tool Limitations
Benjamin J. Sheahan - *Stanford Univ., Stanford, CA*
John W. Fattaruso, Jennifer Wong, Karlheinz Muth - *Texas Instruments Inc., Dallas, TX*
Boris Murmann - *Stanford Univ., Stanford, CA*

50.4 Power-Centric Design of High-Speed I/O
Hamid Hatamkhani - *Univ. of California, Los Angeles, CA*
Frank Lambrecht - *Rambus, Inc., Mountain View, CA*
Vladimir Stojanovic - *Massachusetts Institute of Tech., Cambridge, MA*
Chih-Kong Ken Yang- *Univ. of California, Los Angeles, CA*

SESSION 51

Rm: **301**

ANALOG DESIGN AND DESIGN ASSISTANCE

Chair: Peng Li - *Texas A&M Univ, College Station, TX*
Organizers: Helmut Graeb, Rob A. Rutenbar

This session presents a mix of design case studies, design automation and design assistance techniques for several difficult mixed-signal circuits and systems. The first paper presents a new low-power ADC that is the winner of the 2006 DAC-ISSCC student design contest. The second paper deals with application of optimization in LNA design, while the third paper presents a non-optimization design migration aid applied to a bias cell and a crystal oscillator. The fourth paper presents how to maintain model consistency during the design of a multi-mode multi-band transceiver front-end.

51.1 A 10.6mW/0.8pJ Power-Scalable 1GS/s 4b ADC in 0.18um CMOS with 5.8GHz ERBW
Pierluigi Nuzzo - *Univ. of Pisa, Pisa, Italy*
Geert Van der Plas - *IMEC, Leuven, Belgium*
Fernando De Bernardinis - *Univ. of Pisa, Pisa, Italy*
Liesbet Van der Perre, Bert Gyselinckx - *IMEC, Leuven, Belgium*
Pierangelo Terreni - *Univ. of Pisa, Pisa, Italy*

51.2 SoC-LNA: Synthesis and Optimization for Fully Integrated Narrow-Band CMOS Low Noise Amplifiers
Arthur Nieuwoudt, Tamer Ragheb, Yehia Massoud - *Rice Univ., Houston, TX*

51.3s Chameleon ART: A Non-Optimization Based Analog Design Migration Framework
Sherif Hammouda - *Mentor Graphics Corp., Cairo, Egypt*
Hazem Said - *Ain Shams Univ., Cairo, Egypt*
Mohamed Dessouky, Mohamed Tawfik - *Mentor Graphics Corp., Cairo, Egypt*
Quang Nguyen - *ON Semiconductor France SAS, Toulouse, France*
Wael Badawy - *Univ. of Calgary, Calgary, AB*
Hazem Abbas - *Mentor Graphics Corp., Cairo, Egypt*
Hussein Shahein - *Ain Shams Univ., Cairo, Egypt*

51.4s Ensuring Consistency During Front-End Design Using an Object-Oriented Interfacing Tool Called NETLISP
Michael Goffioul - *IMEC, Leuven, Belgium*
Gerd Vandersteen - *Vrije Universiteit Brussels, Brussels, Belgium*
Joris Van Driessche, Björn Debaillie, Boris Come - *IMEC, Leuven, Belgium*

Thursday July 27, 2006

2:00 pm - 4:00 pm

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S - denotes short paper
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SESSION 52

Rm: **306/308**

HIGH-PERFORMANCE SIMULATION OF TRANSACTION LEVEL AND DATAFLOW MODELS

Chair: Felice Balarin - *Cadence Berkeley Labs, Berkeley, CA*
Organizers: Adam Donlin, Andres R. Takach, Luciano Lavagno, Sandeep Shukla

High-performance simulation is a crucial requirement for ESL. The first two papers in this session address rapid simulation and throughput-driven optimization of buffer sizes in dataflow models. The remaining papers discuss three advanced SystemC ESL topics. The first is a generic approach to Transaction Level Modeling. The second layers multiple models of computation over the native SystemC kernel. Finally, a UML-SystemC modeling tool with full roundtrip capability is presented.

52.1 Efficient Simulation of Critical Synchronous Dataflow Graphs
Chia-Jui Hsu - *Univ. of Maryland, College Park, MD*
Suren Ramasubbu - *Agilent Technologies, Inc., Palo Alto, CA*
Ming-Yung Ko - *Univ. of Maryland, College Park, MD*
Jose Luis Pino - *Agilent Technologies, Inc., Palo Alto, CA*
Shuvra S. Bhattacharyya - *Univ. of Maryland, College Park, MD*

52.2 Exploring Tradeoffs in Buffer Requirements and Throughput Constraints for Synchronous Dataflow Graphs
Sander Stuijk, Marc Geilen, Twan Basten - *TU Eindhoven, Eindhoven, Netherlands*

52.3 GreenBus - A Generic Interconnect Fabric for Transaction Level Modeling
Wolfgang Klingauf, **Robert Guenzel** - *TU Braunschweig, Braunschweig, Germany*
Oliver Bringmann, Pavel Parfuntseu - *FZI Forschungszentrum Informatik, Karlsruhe, Germany*
Mark Burton - *GreenSocs, Cambridge, UK*

52.4s A Framework for Embedded System Specification under Different Models of Computation in SystemC
Fernando Herrera, Eugenio Villar - *Univ. of Cantabria, Santander, Spain*

52.5s A Model Driven Design Environment for Embedded Systems
Elvinia Riccobene - *Univ. of Milan, Crema, Italy*
Patrizia Scandurra - *Univ. of Catania, Catania, Italy*
Sara Bocchio, Alberto Rosti - *STMicroelectronics, Agrate Brianza, Italy*

SESSION 53

Rm: **307**

NANO- AND BIO-CHIP DESIGN

Chair: Ion Mandoiu - *Univ. of Connecticut, Storrs, CT*
Organizers: Igor L. Markov, Niraj Jha

This session presents chip design techniques for nano- and bio-technologies. The first paper leverages thermodynamics to select appropriate base pairs in DNA-driven self-assembly. The next two papers offer new design techniques for microfluidic biochips. The final paper in this session describes a 3D carbon nanotube capacitor.

53.1 Design Automation for DNA Self-Assembled Nanostructures
Constantin Pistol, Alvin Lebeck, Chris L. Dwyer - *Duke Univ., Durham, NC*

53.2 Automated Design of Pin-Constrained Digital Microfluidic Arrays for Lab-on-a-Chip Applications
William L. Hwang, **Fei Su**, Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

53.3s Placement of Digital Microfluidic Biochips Using the T-tree Formulation
Ping-Hung Yuh, Chia-Lin Yang, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

53.4s A High Density, Carbon Nanotube Capacitor for Decoupling Applications
Mark M. Budnik, Arijit Raychowdhury, Aditya Bansal, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

SESSION 54

Rm: **305**

LOGIC AND SEQUENTIAL SYNTHESIS

Chair: Maciej Ciesielski - *Univ. of Massachusetts, Amherst, MA*
Organizers: Adam Donlin, Jean Christophe Madre, Malgorzata Marek-Sadowska

Papers in this section address a broad spectrum of topics in logic synthesis. The first paper incorporates logic synthesis into the design flow of large asynchronous control circuits obtained from high-level specifications. The next three papers address various aspects of clock period optimization. The last paper proposes an approach to gate sizing for binning yield optimization.

54.1 State Encoding of Large Asynchronous Controllers
Josep Carmona, Jordi Cortadella - *Univ. Politécnica de Catalunya, Barcelona, Spain*

54.2 An Efficient Retiming Algorithm under Setup and Hold Constraints
Chuan Lin, Hai Zhou - *Northwestern Univ., Evanston, IL*

54.3s Extensive Slack Balance: An Approach to Make Front-end Tools Aware of Clock Skew Scheduling
Kui Wang, Lian Duan, Xu Cheng - *Peking Univ., Beijing, China*

54.4s Budgeting-Free Hierarchical Design Method for Large Scale and High-Performance LSIs
Yuichi Nakamura - *NEC Corp., Kawasaki, Japan*
Mitsuru Tagata - *NEC Corp., Hakusan, Japan*
Takumi Okamoto - *NEC Corp., Kawasaki, Japan*
Shigeyoshi Tawada, Ko Yoshikawa - *NEC Corp., Fuchu, Japan*

54.5 Variability Driven Gate Sizing for Binning Yield Optimization
Azadeh Davoodi, Ankur Srivastava - *Univ. of Maryland, College Park, MD*

All speakers are denoted in bold
denotes short paper - S
denotes best paper candidate - ß
session of special interest to designers -
indicates videoed session -

Thursday July 27, 2006
2:00 pm - 4:00 pm

SESSION 55

Rm: **304**

LOW-POWER CIRCUIT DESIGN

Chair: Ali Keshavarzi - *Intel Corp., Hillsboro, OR*
Organizers: Naehyuck Chang, Trevor Mudge

This session addresses various techniques related to low-power circuit design ranging from Elmore models for energy estimation, variation-aware SRAM cell or dynamic gates design, to standard cell leakage power optimization and low-power bus encoding.

55.1 Elmore Model for Energy Estimation in RC Trees

Quming Zhou, Kartik Mohanram - *Rice Univ., Houston, TX*

55.2 Self-Calibration Technique for Reduction of Hold Failures in Low-Power Nano-scaled SRAM

Swaroop Ghosh, Saibal Mukhopadhyay, Keejong Kim, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

55.3 A Novel Variation-Aware Low-Power Keeper Architecture for Wide Fan-in Dynamic Gates

Hamed F. Dadgour - *Univ. of California, Santa Barbara, CA*
Rajiv Joshi - *IBM Corp., Yorktown Heights, NY*
Kaustav Banerjee - *Univ. of California, Santa Barbara, CA*

55.4s Standard Cell Library Optimization for Leakage Reduction

Saumil S. Shah - *Univ. of Michigan, Ann Arbor, MI*
Puneet Gupta, Andrew B. Kahng - *Blaze DFM, Inc., Sunnyvale, CA*

55.5s Low-Power Bus Encoding Using An Adaptive Hybrid Algorithm

Avnish R. Brahmbhatt, Jingyi Zhang, **Qing Wu**, Qinru Qiu - *Binghamton Univ., Binghamton, NY*

SESSION 56

Rm: **303**

BEYOND-THE-DIE CIRCUIT AND SYSTEM INTEGRATION

Chair: Shauki Elassaad - *Emergent Design Solutions, Santa Clara, CA*
Organizers: John Berrie, Mike Heimlich

The first two papers cover performance, power and temperature tradeoffs in 3D integrated circuit design, from architecture and circuit points of view. The third paper addresses efficient high-density escape routing. The final two papers are concerned with system-level high-speed signal and power integrity, including pre-emphasis and equalisation analysis.

56.1 A Thermally-Aware Performance Analysis of Vertically Integrated (3D) Processor-Memory Hierarchy

Gian Luca Loi, **Banit Agrawal**, Navin Srivastava, Sheng-Chih Lin, Timothy Sherwood, Kaustav Banerjee - *Univ. of California, Santa Barbara, CA*

56.2 Exploring Compromises Among Timing, Power and Temperature in Three-Dimensional Integrated Circuits

Hao Hua, Chris Mineo, Kory Schoenfliess, Ambarish Sule, Samson Melamed, Ravi Jenkal, **Rhett Davis**, - *North Carolina State Univ., Raleigh, NC*

56.3 Efficient Escape Routing for Hexagonal Array of High Density I/Os

Rui Shi, Chung-Kuan Cheng - *Univ. of California at San Diego, La Jolla, CA*

56.4s System Level Signal and Power Integrity Analysis Methodology for System-In-Package Applications

Rohan Mandrekar, **Krishna Bharath**, Krishna Srinivasan, Ege Engin, Madhavan Swaminathan - *Georgia Institute of Tech., Atlanta, GA*

56.5s PELE: Pre-Emphasis and Equalization Link Estimator to Address the Effects of Signal Integrity Limitations

William Bereza, Yuming Tao, Shoujun Wang, Rakesh Patel, Tad Kwasniewski - *Altera Corp., Kanata, ON, Canada*

SESSION 57

Rm: **301**

NEW IDEAS IN ANALOG/RF MODELING AND SIMULATION

Chair: Luca Daniel - *Massachusetts Institute of Tech., Cambridge, MA*
Organizers: Koen Lampaert, Rob A. Rutenbar

Accurate macromodeling and fast simulation remain two of the highest priorities for all working analog designers. This session presents new ideas in both modeling and simulation, targeting a range of difficult and important circuits. The first paper presents a novel decomposition strategy for building nonlinear cell-level analog macromodels. The second paper develops a new technique for efficient extraction of phase macromodels for digitally controlled oscillator circuits. The third paper describes new, robust envelope-following methods for RF circuits. The final paper describes new table-lookup methods for very fast simulation and statistical modeling of sigma-delta designs.

57.1 A Multilevel Technique for Robust and Efficient Extraction of Phase Macromodels of Digitally Controlled Oscillators

Xiaolue Lai, Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*

57.2 Systematic Development of Nonlinear Analog Circuit Macromodels through Successive Operator Composition and Nonlinear Model Decoupling

Ying Wei, Alex Doboli - *State Univ. of New York, Stony Brook, NY*

57.3 A Robust Envelope Following Method Applicable to Both Non-Autonomous and Oscillatory Circuits

Ting Mei, Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*

57.4 Lookup Table Based Simulation and Statistical Modeling of Sigma-Delta ADCs

Guo Yu, Peng Li - *Texas A&M Univ., College Station, TX*

Thursday July 27, 2006
4:30 pm - 6:00 pm

All speakers are denoted in bold
S - denotes short paper
ß - denotes best paper candidate
- session of special interest to designers
- indicates videoed session

SESSION 58

Rm: **306/308**

ADVANCED METHODS FOR INTERCONNECT EXTRACTION, CLOCKS AND RELIABILITY

Chair: Arvind NV - *Texas Instruments Inc., Bangalore, India*
Organizers: Farid N. Najm, Nagaraj NS

This session covers clock skew minimization, parallel matrix compression for parasitic extraction and reliability design methods for NBTI and gate oxide reliability. The first paper covers a new formulation of clock skew minimization that uses a quadratic programming approach and considers subcritical skews in addition to the most critical skews. The next paper describes a parallel implmentation of the low-rank compression with linear cost reduction capacity with respect to the number of processors. Static and dynamic NBTI modeling and design methods to mitigate the NBTI effects are presented. In the final paper, a new dynamic reliability management scheme is described to balance the increasing throughput during periods of peak computational demand while ensuring the required reliability lifetime.

58.1 Clock Buffer and Wire Sizing Using Sequential Programming
Matthew R. Guthaus, Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*
Richard B. Brown - *Univ. of Utah, Salt Lake City, UT*

58.2 Modeling and Minimization of PMOS NBTI Effect for Robust Nanometer Design
Rakesh Vattikonda, Yu Kevin Cao, Wenping Wang - *Arizona State Univ., Tempe, AZ*

58.3s A Parallel Low-Rank Multilevel Matrix Compression Algorithm for Parasitic Extraction of Electrically Large Structures
Chuanyi Yang, Swagato Chakraborty, Dipanjan Gope, Vikram Jandhyala - *Univ. of Washington, Seattle, WA*

58.4s Reliability Modeling and Management in Dynamic Microprocessor-Based Systems
Eric Karl, David Blaauw, Dennis Sylvester, Trevor N. Mudge - *Univ. of Michigan, Ann Arbor, MI*

SESSION 59

Rm: **307**

PANEL: DFM WHERE'S THE PROOF OF VALUE?

Chair: Joe Brandenburg - *Consultant, Portland, OR*
Organizers: Linda Marchant, Shishpal Rawat

How can design teams employ new techniques and still stay within design budgets? How much effort does it require to be an early adopter? How does a design engineer get measurable results to compensate for his effort? The discussion uses the example of a fixed design budget and timeline, and panelists discuss how their tools fit into that budget and what the ROI (monetary, quality, reduced time-to-market, comprehensive yield enhancement) would be.

Panelists:

Joseph Sawicki - *Mentor Graphics Corp., Wilsonville, OR*
Andrew B. Kahng - *Blaze DFM, Inc., Sunnyvale, CA*
Atul Sharan - *Clear Shape Technologies., Inc., Sunnyvale, CA*
Naeem Zafar - *Pyxis Technology, Inc., Santa Clara, CA*
Mike Gianfagna - *Aprio Technologies, Inc., Santa Clara, CA*
Raul Camposano - *Synopsys, Inc., Santa Clara, CA*

SESSION 60

Rm: **305**

BOUNDED MODEL CHECKING AND EQUIVALENCE VERIFICATION

Chair: Gagan Hasteer - *Calypto Design Systems, Inc., Santa Clara, CA*
Organizers: Anmol Mathur, Avi Ziv

This session groups two papers on equivalence checking with two papers on bounded property checking. One equivalence paper compares very high-level descriptions to RTL, and the other extracts RTL from transistor models of FPGAs. The bounded property checking papers propose automatic heuristics for guiding BDD-based state-space exploration and deriving invariants to improve model checking efficiency.

60.1 Early Cutpoint Insertion for High-Level Software vs. RTL Formal Combinational Equivalence Verification
Xiushan Feng, Alan J. Hu - *Univ. of British Columbia, Vancouver, BC, Canada*

60.2s Transistor Abstraction for the Functional Verification of FPGAs
Guy Dupenloup, Thierry Lemeunier, Roland Mayr - *Altera Corp., San Jose, CA*

60.3s Automatic Invariant Strengthening to Prove Properties in Bounded Model Checking
Mohammad H. Awedh, Fabio Somenzi - *Univ. of Colorado, Boulder, CO*

60.4 Fast Falsification Based on Symbolic Bounded Property Checking
Prakash M. Peranandam, Pradeep K. Nalla, Juergen Ruf, Roland J. Weiss, Thomas Kropf, Wolfgang Rosenstiel - *Univ. of Tuebingen, Tuebingen, Germany*

All speakers are denoted in bold
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Thursday July 27, 2006

4:30 pm - 6:00 pm

SESSION 61

Rm: **304**

TEST RESPONSE COMPACTION AND ATPG

Chair: Anuja Sehgal - *Advanced Micro Devices, Inc., Sunnyvale, CA*

Organizers: Kazumi Hatayama, Patrick Girard

Increasing circuit complexity and new test methods for deep-submicron defects make the test data volume grow to an intractable size. After compressing the test stimuli, the current research wave addresses compaction of test responses. The last paper is an example of a new test method addressing deep-submicron defects.

61.1 Unknown-Tolerance Analysis and Test-Quality Control for Test Response Compaction Using Space Compactors

Mango Chia-Tso Chao, Tim Cheng - *Univ. of California, Santa Barbara, CA*
Seongmoon Wang, Srimat T. Chakradhar, Wen-long Wei - *NEC-Labs America, Princeton, NJ*

61.2 Test Response Compactor with Programmable Selector

Grzegorz Mrugalski, Janusz Rajski - *Mentor Graphics Corp., Wilsonville, OR*
Jerzy Tyszer - *Poznan Univ. of Tech., Poznan, Poland*

61.3s Fault Detection and Diagnosis with Parity Trees for Space Compaction of Test Responses

Harald Vranken, **Sandeep K. Goel** - *Philips Research Labs, Eindhoven, Netherlands*
Andreas Glowatz, Juergen Schloeffel, Friedrich Hapke - *Philips Semiconductors, Hamburg, Germany*

61.4s Multiple-Detect ATPG Based on Physical Neighborhoods

Jeffrey E. Nelson, Jason G. Brown, Rao Desineni, Ronald D. Blanton - *Carnegie Mellon Univ., Pittsburgh, PA*

SESSION 62

Rm: **303**

PLACEMENT

Chair: Bill Halpin - *Synplicity, Inc., San Jose, CA*

Organizers: Jiang Hu, Louis Scheffer

This session focuses on new placement techniques for integrated circuits. Included are a new method for floorplan repair after changes, improved approaches to cell flipping, and a new technique for timing driven incremental placement.

62.1 Constraint-Driven Floorplan Repair

Michael D. Moffitt, Aaron N. Ng, Igor L. Markov, Martha E. Pollack - *Univ. of Michigan, Ann Arbor, MI*

62.2 Optimal Cell Flipping in Placement and Floorplanning

Chiu-Wing Sham, Evangeline Young - *Univ. of Hong Kong, Hong Kong, China*
Chong-Nuen Chu - *Iowa State Univ., Ames, IA*

62.3 A New LP Based Incremental Timing Driven Placement for High Performance Designs

Tao Luo - *Univ. of Texas, Austin, TX*
David Newmark - *Advanced Micro Devices, Inc., Austin, TX*
David Z. Pan - *Univ. of Texas, Austin, TX*

Tutorials - Monday, July 24

TUTORIAL 1 - ESL DESIGN METHODOLOGY USING SYSTEMC

Rm: 305

Organizer: **Francine Bacchini** - *ThinkBold Corporate Communications, San Jose, CA*
Presenters: **Wolfgang Rosenstiel** - *Univ. of Tuebingen, Tubingen, Germany*
Jack Donovan - *ESLX, Inc., Austin, TX*
Maurizio Vitale - *Philips Semiconductors, Pittsburgh, PA*
Laurent Maillet-Contoz - *STMicroelectronics, Crolles, France*
Mike Meredith - *Forte Design Systems, San Jose, CA*
Vincent Viteau - *Summit Design, Inc., Cedex, France*

This tutorial is ideally suited to System Architects, Software Architects and Developers, and Hardware Design and Verification engineers. The aim of this electronic system-level (ESL) design methodology tutorial is to communicate to adopters and prospective adopters of ESL design the primary considerations involved in the establishment of an architecture-to-implementation design, verification, optimization and debug methodology, including embedded software development.

The use and re-use of transaction-level models (TLM) formulated in the SystemC language will be described and assessed in the context of their application to (1) architectural development and optimization, (2) early software development, (3) hardware and hardware/software verification, and (4) hardware implementation.

This tutorial will begin with an overview of the use models, followed by a "how to" exposition on the development of the virtual system platform (VSP) for early embedded software development. Two designers with ESL design methodology expertise – from STMicroelectronics and Philips – will then recount their experience in its use, offering practical development and deployment tips. The tutorial will then discuss implementation methodologies. The tutorial will conclude with an example of an ESL design, verification and debug flow from architecture to RTL, followed by Q&A.

TUTORIAL 2 - PRACTICAL ASPECTS OF COPING WITH VARIABILITY: AN ELECTRICAL VIEW

Rm: 304

Organizer: **Chandu Visweswariah** - *IBM Corp., Yorktown Heights, NY*
Presenters: **Xi-Wei Lin** - *Synopsys, Inc., Mountain View, CA*
Bora Nikolic - *Univ. of California, Berkeley, CA*
Peter A. Habitz - *IBM Corp., Burlington, NC*
Riko Radojcic - *Qualcomm CDMA Technologies, San Diego, CA*

This comprehensive tutorial on the electrical aspects of variability will be presented by leading industry practitioners and academic researchers. Emphasis will be placed on practical techniques and methodologies for analyzing and dealing with variability. The tutorial will consist of four main sections:

1) The tutorial begins with understanding exactly where the variability is coming from and classifying the sources of variability into systematic and random effects.

2) The second section focuses on test and characterization structures for both logic and array applications, and how to reflect variability in timing and power models, including speculation on emerging statistical timing model standards.

3) The next section is a practical introduction to statistical timing and optimization techniques, with a focus on timing methodology considerations to cope with variability while reducing timing pessimism.

4) The final section will concentrate on deployment of both physical and electrical DFM solutions and present a taxonomy of available DFM tools and the corresponding methodologies into which they fit.

This is a unique opportunity to learn about the latest developments from the experts!

Tutorials - Friday, July 28

TUTORIAL 3 - REAL DFM SOLUTIONS, TOOLS, METHODOLOGIES, AND SUCCESSES

Rm: 304

Organizer: **Andrew B. Kahng** - *Univ. of California at San Diego, La Jolla, CA*
Presenters: **Nagaraj NS** - *Texas Instruments Inc., Dallas, TX*
Jean-Pierre Schoellkopf - *STMicroelectronics, Crolles, France*
Mike Smayling - *Applied Materials, Sunnyvale, CA*
Ban P. Wong - *Chartered Semiconductor, Milpitas, CA*
Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*

Topics include: (i) Today's stress on "geometric DFM" over "electrical DFM", which misses out on value propositions such as performance robustness and more rapid power/timing closure. (ii) Benefits from statistical design (which requires new infrastructure for modeling, IP, signoff and tool infrastructure) versus benefits from "variation-aware design" (which exploits a link to the fab but is otherwise compatible with today's design and signoff flows). (iii) Opportunities for new "design synergy" – uniformity, structure, compensation, etc. – that can dramatically improve yield and manufacturability.

Entering the 65nm node, today's DFM tools attempt to satisfy several basic objectives. To address the failure of "WYSIWYG" in sub-100nm process nodes, "shape" (x-y dimension) and "thickness" (z dimension) simulation technologies are being deployed. To address "uncontrollable variation", statistical analysis technologies (SSTA, statistical extraction, etc.) are being investigated. And, well-established internal technologies for defect-oriented yield analysis (critical area, pattern hotspot finding) and optimization (via/contact doubling, wire spreading, etc.) are being commoditized. The order of tool deployment has been as one would expect: (1) geometric criteria (through process window hot-spots, etc.) before electrical criteria (leakage, timing variation, etc.); (2) library and IP development use models before full-chip use models; and (3) analyses before optimizations.

TUTORIAL 4 - SURVIVING AND THRIVING IN THE WORLD OF CHIP AND PACKAGE CO-DESIGN

Rm: 305

Organizers: **Chung-Kuan Cheng** - *Univ. of California at San Diego, La Jolla, CA*
Howard Chen - *IBM Corp., Yorktown Heights, NY*
Presenters: **Paul Harvey** - *IBM Corp., Austin, TX*
Howard Chen - *IBM Corp., Yorktown Heights, NY*
Lei He - *Univ. of California, Los Angeles, CA*
Chung-Kuan Cheng - *Univ. of California at San Diego, La Jolla, CA*
Kaushik Sheth - *Rio Design Automation, Inc., Santa Clara, CA*

Beyond the die, it takes a holistic approach to tackle the design problems at the package, board, and system levels. This tutorial will begin with an overview of the emerging packaging technologies and their impact on chip performance. Then we will provide a comprehensive list of simple, but often overlooked, design methods to help tutorial attendees get the most out of today's new packaging technologies. We will explain how statistical techniques can be employed to ensure that the design will work over the entire tolerance range without resorting to conservative and very expensive over-design practices. We will also discuss competing design objectives such as electrical, thermal, mechanical, reliability, and manufacturability requirements and illustrate co-design methods with numerous examples. The co-modeling of chip/package power distribution design will be presented to analyze and minimize transient power supply noise due to clock gating, power gating, frequency scaling, and other power management activities. We will describe the key components in a chip and package co-design flow with emphasis on package-aware chip I/O planning, structure-preserved model order reduction for large number of ports, and power integrity optimization with power domain partitioning and decoupling capacitor insertion. In addition, we will explore the scalability of the technologies and present advanced design techniques such as active and passive compensation for low-power and high-speed interconnect. Finally, this tutorial will highlight the short-term and long-term implications of ignoring the relationship between the chip, package and PCB. We will describe an effective means of bridging the gap between the designs of high-performance chips and packages, and a chip's integration with the rest of the electronic system. By adopting such a package-aware chip design flow, we can ensure design convergence and eliminate the ad-hoc iteration between chip and package designs.

Tutorials - Friday, July 28

TUTORIAL 5 - SYSTEMVERILOG: LANGUAGE TUTORIAL AND INDUSTRIAL VERIFICATION EXPERIENCE

Rm: 307

Organizer: **Johny Srouji** - *IBM Corp., Austin, TX*
Presenters: **Johny Srouji** - *IBM Corp., Austin, TX*
Karen Pieper - *Synopsys, Inc., Sunnyvale, CA*
Tom Fitzpatrick - *Mentor Graphics Corp., Groton, MA*
John Havlicek - *Freescale Semiconductor, Inc., Austin, TX*
Matt Maidment - *Intel Corp., Portland, OR*
Cliff Cummings - *Sunburst Design Inc., Portland, OR*

With the ever-increasing complexity of electronic systems and processors in the industry as driven by performance and functionality, design and verification are becoming more complex. As designs become packed with greater functionality and verification takes up more of the overall schedule, there is a need for a standard language to support all aspects of the design and verification process. SystemVerilog was developed to extend the Verilog HDL, the predominant language used for chip design for many years, specifically to address these needs.

This tutorial will provide a detailed overview of the IEEE 1800 SystemVerilog Hardware Design and Verification Language (HDVL), including practical examples of industrial experience using the language to develop complex designs. The tutorial will include a thorough description of the SystemVerilog definition, intent and potential while covering the design modeling, testbench automation, verification, assertions aspects of the language, and the programming interfaces. The practical sessions will include discussions of what has worked well, the impact on design and verification productivity and transition experiences from Verilog to SystemVerilog, as well as suggestions of possible future directions for the language.

TUTORIAL 6 - TOOLS FOR HYBRID EMBEDDED SYSTEMS: MODELING, VERIFICATION, AND DESIGN

Rm: 302

Organizer: **Luca Carloni** - *Columbia Univ., New York, NY*
Presenters: **Hilding Elmqvist** - *Dynasim AB, Lund, Sweden*
George Pappas - *Univ. of Pennsylvania, Philadelphia, PA*
Pieter J. Mosterman - *The MathWorks, Inc., Natick, MA*
Alessandro Pinto - *Univ. of California, Berkeley, CA*
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

This tutorial gives a detailed overview of the current landscape of tools for the specification, design, and validation of hybrid embedded systems.The basic principles of hybrid systems (systems that feature both continuous and discrete time components) modeling will be presented as the common theoretical underpinning for all the tools. The core of the tutorial will be live demonstrations of about a dozen tools that have been developed in the industry and academia.

For each tool, a brief presentation of its syntactic and semantic characteristics will be followed by a practical exposition of how to use it to model and design some simple, but challenging "running examples", thereby showing its advantages and limitations. This will provide a sound mechanism to compare the tools by illustrating their differences in terms of expressiveness, usability, power, and performance. Some industrial examples will be modeled, presented, and discussed.

Tutorials - Friday, July 28

TUTORIAL 7 - FROM BASIC TO ADVANCED TECHNIQUES FOR SILICON DEBUG AND DIAGNOSIS

Rm: 306/308

Organizer: **Srikanth Venkataraman** - *Intel Corp., Hillsboro, OR*
Presenters: **Srikanth Venkataraman** - *Intel Corp., Hillsboro, OR*
Miron Abramovici - *DAFCA Inc., Framingham, MA*
Robert Aitken - *ARM, Sunnyvale, CA*

- Design error diagnosis, silicon debug and defect diagnosis ranging from the basic concepts to advanced applications and new DFD techniques.
- Established diagnosis procedures including fault dictionaries, post-test fault simulation, and back tracing.
- Methods for locating defects such as opens, shorts, and leakage in transistor-level circuits, approximation techniques for identifying unmodeled faults, Iddq-based diagnosis, diagnosis for delay-faults, scan-chain diagnosis, test compression-based diagnosis BIST-based diagnosis, and design-for-diagnosability techniques.
- Silicon debug techniques, design-for-debug techniques, and error location procedures.
- Diagnosis for yield learning application and feedback for DFM techniques.
- Successful debug and diagnosis methods used in real industrial products, industrial experiences, and case studies.

UML for SoC Design Workshop

Sunday, July 23 • 9:00 am - 6:00 pm **Rm: 302**

REGISTRATION INSTRUCTIONS

Workshop registration is required.

$100 ACM/IEEE Members

$150 Non-Members

The program of the third workshop on the Unified Modeling Language™ (UML) for System-on-a-Chip (SoC) design includes papers from design teams and researchers around the globe. UML is attracting growing interest as a system level visual language to support the tasks of specifying, analyzing, designing, and verifying SoCs. The UML for SoC Design Workshop is meant to coordinate efforts, to initiate discussions, and to exchange experiences/information related to UML applied to SoC design and hardware aspects. A keynote by Dr. Sreeranga Rajan, Chair of the UML-SoC profile Standardization Committee at the Object Management Group™ (OMG), will open the workshop and provide the latest information about this standard extension to UML for SoC development. Other presentations will explore embedded system analysis, design, modeling, synthesis, and design flows supported by UML. The workshop is open to anyone interested in learning more about UML for SoC Design.

9:00 *Welcome and Introduction by the Workshop Organizers*
Y. Vanderperren - *Katholieke Univ., Leuven, Belgium*
J. Wolfe - *Mentor Graphics Corp., Mobile, AL*

9:15 *Keynote - UML for SoC: Where, When, and How?*
Sreeranga P. Rajan - *Fujitsu Labs, Sunnyvale, CA*

Session 1: Systems Modeling with UML

9:45 *UML Modeling and Configuration of Tile Based Networks-on-Chip*
Subhek Garg, Marcello Lajolo - *NEC, Princeton, NJ*

10:15 *UML-Based Modeling of Time-triggered Applications*
Kathy Dang Nguyen, Geoffrey Koh, P.S. Thiagarajan, Weng-Fai Wong - *Univ. of Singapore, Singapore*

10:45 Coffee Break

Session 2: UML-based SoC Design Space Exploration

11:00 *Multi-objective Design Space Exploration Based on UML*
Marcio F. da S. Oliveira, Eduardo Brião, Francisco Nascimento, Lisane Brisolara, Luigi Carro, Flávio Wagner - *Federal Univ. of Rio Grande do Sul, Porto Alegre, Brazil*

11:30 *A UML-Based Design Flow and Partitioning Methodology for Dynamically Reconfigurable Systems*
Chih-Hao Tseng, Pao-Ann Hsiung - *National Chung-Cheng Univ., Taiwan, Republic of China*

12:00 *Design Space Exploration Through Interactive Model Mappings for UML-based Specifications*
Tim Schattkowsky - *C-LAB, Paderborn, Germany*
Achim Rettberg - *Paderborn Univ., Paderborn, Germany*
Rainer Doemer - *Univ. of California, Irvine, CA*

12:30 Lunch - Rm: 304

Session 3: UML and SoC Languages

2:00 *Automatic Generation of Verification Properties for SoC Design from SysML-Diagrams*
Stefan Laemmermann, Roland Weiss, Juergen Ruf, Thomas Kropf, Wolfgang Rosenstiel - *Univ. of Tuebingen, Germany*

2:30 *SoC, UML and MDA - An Investigation*
Maha Ramanan - *Philips Semiconductors, Southampton, UK*

3:00 *A SoC Design Flow Based on UML 2.0 and SystemC*
Alberto Rosti, Sara Bocchio - *STMicroelectronics, Milano, Italy*
Elvinia Riccobene - *Univ. of Milano, Milano, Italy*
Patrizia Scandurra - *Univ. of Catania, Catania, Italy*

3:30 Coffee break and tool demos

Session 4: Models of Computations and UML for SoC

4:00 *Stereotyping for Register-level SoC Custom Logic Kernel Design: Integrating Algorithmic State Machines into UML*
James P. Davis, Achraf El Allali, Bryan D. Young, Salman Ali - *Univ. of South Carolina, Columbia, SC*

4:30 *Towards a Unified Behavioral Language*
Wolfgang Mueller, Henning Zabel - *C-LAB, Paderborn, Germany*

Session 5: Workshop Discussion

5:00 *Challenges with UML-Based SoC Design and State-of-the-Art Solution*
Y. Vanderperren - *Katholieke Univ., Leuven, Belgium*
J. Wolfe - *Mentor Graphics Corp., Mobile, AL*

6:00 *Workshop Wrap-up*

Second Integrated Design System Workshop

Monday, July 24 • 12:00 pm - 5:00 pm **Rm: 303**

Organizers: **John Darringer** - *IBM Corp.* **Rahul Goyal** - *Intel Corp.* **Alva Barney** - *Hewlett-Packard Co.* **Scott Peterson** - *LSI Logic Corp.* **Bill Bayer** - *Si2*

Objective - The era of "point tools" linked by files is long over. Streamlined integrated design systems are essential to meet today's business demands. Custom chip designers require them to integrate growing numbers of macros while insuring manufacturability. ASIC and SoC designers must have them to optimize multiple factors simultaneously to achieve "design closure". Product designers need them to exploit 3DIC and SiP package synergy and remain competitive.

What does it take to develop these effective integrated design systems? Vendors provide solutions for parts of a methodology, but most users want to exploit the best tools from multiple vendors and add proprietary applications to gain a competitive advantage. Progress has been made on standard APIs for sharing data, but much more is needed to enable design systems to keep pace with the industry.

This workshop brings together design system managers and design system providers from the industry's leading companies to assess the state of integrated design systems today, identify the top challenges remaining, discuss the potential solutions in the pipeline as well as those that are likely, just over the horizon. What new directions will integrated design systems move into next? What gains in productivity can be expected?

Each session will include a panel to probe deeper into the topics presented and allow your questions to be addressed and your comments be heard.

REGISTRATION INSTRUCTIONS

Workshop registration is required.
$50.00 - ACM/IEEE Members • $75.00 - Non-Members

12:00 pm Lunch

1:00 pm Part 1: Today's Challenges and Solutions

Moderator: **Scott Peterson** - *LSI Logic Corp., Bloomington, MN*

1:20 pm ***What are the Most Important Challenges for Integrating Design Systems Today?***

- **Thomas Harms** - *Infineon Technologies AG, Munich, Germany*
- **Philippe Magarshack** - *STMicroelectronics, Crolles Cedex, France*
- **Rahul Goyal** - *Intel Corp., Santa Clara, CA*

1:50 pm ***What is Coming to Address These Challenges?***

- **Antun Domic** - *Synopsys, Inc., San Jose, CA*
- **Ted Vucurevich** - *Cadence Design Systems, Inc., San Jose, CA*
- **George Janac** - *Silicon Navigator, Inc., Cupertino, CA*

2:20 pm ***PANEL – What are the Top Priorities and When Will They Be Fixed?***

Panel members selected from previous speakers.

3:00 pm Break

3:00 pm Part 2: Tomorrow's Opportunities

Moderator: **Richard Goering** - *EE Times, Ben Lomond, CA*

3:30 pm ***What are the Next Critical Areas to Address?***

Evolution of an Integrated Design System
- **Yoshi Inoue** - *Renesas Tech. Corp., Tokyo, Japan*

System-Level Design
- **Pat Sheridan** - *CoWare, Inc., San Jose, CA*

Design for Manufacturability
- **Juan-Antonio Carballo** - *IBM Corp., Austin, TX*

System in Package and 3D ICs
- **Bill Price** - *Philips Semiconductor, San Jose, CA*

IP Modeling
- **John Goodenough** - *ARM, Sunnyvale, CA*

4:20 pm ***PANEL: What Major Advances are Likely to Happen in the Next 4 Years?***

Panel members selected from previous speakers.

5:00 pm Adjourn

The 43rd Design Automation Conference • July 24 - 28, 2006 • San Francisco, CA

Workshop for Women in Design Automation

Working the 80/20 Rule for Success - Focusing in on What Matters

Monday, July 24 • 9:00 am - 12:45 pm **Rm: 302**

REGISTRATION INSTRUCTIONS
Workshop registration is required.
$50.00 ACM/IEEE Members
$75.00 Non-Members

The workshop's accomplished keynote speaker and panelists will provide insights into how to work the 80/20 rule for success. Showcasing their own real life examples and providing practical suggestions, workshop attendees will learn how these talented women "cracked the code" and learned how to focus on the 20% that mattered and enabled them to achieve the 80% results for career success and work/life balance.

Workshop Chair: **Daya Nadamuni** - *Chief Analyst and Research VP, Gartner Dataquest (pictured)*
Workshop Vice Chair: **Sabina Burns** - *Sr. Director, Corp Marketing and Communications, Virage Logic Corp.*

Steering Committee:
Nanette Collins - *Publicity Chair, 43rd DAC*
Marie R. Pistilli - *Co-Chair, Board of Directors, MP Associates, Inc.*
Telle Whitney - *President, Anita Borg Institute for Women & Technology*

SCHEDULE

9:00 am -10:00 am	**Continental Breakfast and Registration**
10:00 am -12:15 pm	**Keynote Speaker and Panel Discussion**
12:15 pm -12:45 pm	**Award Ceremony**
12:45 pm - 1:45 pm	**Lunch Reception**

Keynote **Reynette Au** - *Vice President Business Licensing, NVIDIA Corp.*

Reynette Au joined NVIDIA as Vice President of Business Licensing in November 2005. With more than 20 years of management experience in the semiconductor industry, she is responsible for building the company's IP licensing business and positioning it as a complementary and strategic partnership-building model across all NVIDIA businesses. Before joining NVIDIA, Reynette was Vice President, Marketing for Stretch Inc., the industry's first company to embed programmable logic within processor architecture to create a unique, software-configurable solution. Prior to this, she was president and Chief Executive Officer for Triscend Corp., which was sold to Xilinx Inc. in 2004; and Vice President, Marketing for ARM, where under her direction, the company significantly expanded the brand awareness of its popular microprocessor solutions and firmly established its market position as 'The Architecture for the Digital World'. She also held operational and program management positions at AMD and AT&T Microelectronics. Reynette earned a Bachelor of Science in Computer Science (BSCS) degree from the University of Denver.

Panel Discussion

Don't miss the opportunity to learn how prominent professionals in the industry have made career choices to achieve a rewarding personal and professional life experience. Each of us has the chance to influence our organization in fundamental ways if we have the tools. Building on the work described in the keynote the panelists will describe their own experience about the impact they have made on their organizations. We are pleased to have panelists from companies and organizations of very different sizes, product lines and focus. You can expect to walk away with concrete examples of changes that work.

Moderator: **Sabina Burns** - *Virage Logic Corp.*
Panelists: **Denise Brouillette** - *The Innovative Edge*
Eillen Sullivan - *Cadence Design Systems, Inc.*
Kathy Papermaster - *IBM Corp.*
Soha Hassoun - *Tufts Univ.*
Sofie Maxwell - *City and County of San Francisco Board of Supervisors - District 10*

Sponsored by:

Supported by:

Introduction to Chips and EDA for a Non-Technical Audience

Monday, July 24 • 10:00 am - 12:00 pm **Rm: 301**

How do they cram all those functions into that little cell phone? Will the next portable music player be so small that you can't see it? Squeezing more features into the electronic products we use every day means the electronics inside are getting more complex. Electronic Design Automation (EDA) makes this happen!

If you are new to the EDA or chip industry or have been in the industry for a while and want to get a little closer to technology, this workshop is for you. It will give you, the non-technical professional, a basic understanding of chip design and the amazing world of Electronic Design Automation.

Organizer
Pamela McDaniel - *Synopsys, Inc.*

Speaker
Karen Bartleson - *Synopsys, Inc., Mountain View, CA*

REGISTRATION INSTRUCTIONS
Workshop registration is required. • $10.00 - Registration fee.

This workshop provides:
- A simplified explanation of how chips are designed and manufactured
- An understanding of how essential EDA is to chip design
- An opportunity to see and touch the parts that make up chips and electronic products
- A non-threatening, fun event with working knowledge to take away

This workshop is for:
- Non-engineering staff from technology companies
- Analysts and media people unfamiliar with EDA and semiconductor industries
- Educators and students who are curious about chip technology and design automation
- Friends and relatives of technical people

Workshop objectives:
- Provide a basic understanding of EDA and semiconductors to non-technical people
- Present information in simple, easy-to-understand terms
- Use hands-on parts (wafers, chips, masks…) for enhanced experience
- Encourage people to join and invest in the EDA industry
- Address ongoing requests to help non-technical people understand the EDA industry

Please note:
This workshop is similar to the one presented at DAC 2005.
The workshop is for non-technical attendees.
Maximum class size: 50

Hands-on Tutorials

General Information

Hands-on Tutorials are three-hour tutorials presented by exhibitors to demonstrate their solutions to a particular issue. This year DAC is offering seven hands-on tutorials on Low Power Design. Demonstrations are done with the attendees working from workstations while the presenters lead the discussion. The tutorials are limited to the first 30 attendees with a student to workstation ratio of 2:1. Due to the proprietary nature of the discussions, presenting companies have the right to refuse access to employees or contractors of competitors. The cost per tutorial is $75 and attendees are encouraged to enroll in more than one tutorial. Attendees must register for a minimum of an exhibits only registration in order to be eligible to enroll in a Hands-on Tutorial.

Analysis and Optimization of Low Power Designs

Presented By: *Apache Design Solutions, Inc.*

Monday, July 24 **9:00 am - 12:00 pm** **Rm: 309**

As designs move to deep-sub-micron technologies, lowered supply voltage, reduced noise margins, and increasing leakage power necessitates extensive verification and analyses prior to tape-out. This tutorial provides hands-on experience in analysis and optimization of designs utilizing power-gating (MTCMOS) technology, a common low-power design technique for leakage control. The tutorial will use RedHawk-LP, Apache's full-chip dynamic power sign-off solution for low-power designs, to accurately analyze the behavior of their power-gated designs, including full-chip power-up and mixed-mode analysis. You will explore and determine the ideal timing intervals for ramp-up, as well as add or remove power-gating switches for optimal design performance. The tutorial will discuss the different operating modes of a power-gated design, and how a block transitioning from one state to another impacts the performance of other blocks in the design. In this tutorial, you will gain the hands-on experience needed to better understand and manage your low-power designs.

Hands-on Tutorials

Using Virtual System Prototypes to Optimize Architectures for Low Power and Other Key Attributes

Presented By: *VaST Systems Technology, StarCore LLC*

Monday, July 24 **2:00 pm - 5:00 pm** **Rm: 310**

Learning Objectives:

1. Review the challenges of software dominated, multi processor, embedded systems development and the need to embrace innovative ways to optimize the architecture for key constraints such as low power
2. Learn how Virtual System Prototype (VSP) driven development makes it easier to optimize complex SoC designs while also improving time to market and quality
3. Explore how to construct a VSP with general purpose and/or digital signal processor + interconnect fabric and then learn how this is used to:
   - Experiment with candidate architectures with respect to architectural constraints
   - Understand how to automatically create empirical data to be used to optimize SoC designs
   - Experience how the VSP can go on to be used as a golden reference model for the concurrent development of software and hardware

Low Power Design Using Predictive Development - Atrenta Solution in Action on a Next-Generation 3G Cell Phone Chip

Presented By: *Atrenta Inc., Freescale Semiconductor, Inc.*

Tuesday, July 25 **2:00 pm - 5:00 pm** **Rm: 309**

With the rapid growth of mobile and wireless applications, power management on chips has become a critical design factor. In an effort to minimize power consumption on a chip, engineers use power management techniques during design implementation in order to reduce dynamic and leakage power consumption. The power dimension to design closure adds significant design challenges besides the usual concerns over functionality, performance and die size.

This hands-on tutorial focuses on predictive development techniques to create designs that are low-power-aware from early design stages. Predictive development is Atrenta's new class of design automation solutions that turn the costly and error-prone activity of electronic development into a more predictable, manageable and reliable process.

Atrenta's SpyGlass LP™ provides a comprehensive set of low-power design techniques in order to address gated clock domains, multiple voltage domains, and power-down regions that may be present in a typical low power design. For example, the use of multiple voltage domains requires that signals crossing the voltage domain boundaries are level-shifted appropriately. The use of power-domains in power-sensitive designs requires that certain signals are isolated correctly under the power-down condition. The presence of multiple voltage and power domains leads to complex power and ground connectivity issues on the chip that needs to be checked.

This tutorial walks the user through the application of these techniques using SpyGlass LP on a representative design. The tutorial also covers a "real-life" customer experience using the Atrenta solution of a next generation cell phone chip at Freescale Semicondutor, Inc.

Hands-on Tutorials

Low Power by Using a Clockless Design Style

Presented By: *Handshake Solutions*

Wednesday, July 26 **9:00 am - 12:00 pm** **Rm: 309**

Handshake Technology is a clockless circuit style without the traditional centralized synchronous clock signal. Handshake Solutions offers access to this unique and proven technology through design tools, standard IP blocks and design services. We recently announced the clockless ARM996HS with nearly a factor three power reduction compared to its clock-gated counterpart. Also, a production proven ultra low-power 80C51 microcontroller subsystem is available for licensing.

Advantages of Handshake Technology based circuits are ultra low-power, low EMI and low peak currents. Our technology relies on an extremely disciplined design style, which allows safe design of self-timed (asynchronous) circuits. This unique silicon compilation approach puts the advantages of self-timed circuits in the hands of any designer. During this hands-on tutorial, the participants will be able to work with our design tools and experience how our high-level design entry language allows them to easily tryout different design alternatives. It also shows how high-level decisions influence important design aspects, like area, speed and power.

Reduce Leakage Power and Increase Battery Life by Implementing an Ideal Vt Selection Strategy

Presented By: *Prolific Inc., ARM*

Wednesday, July 26 **2:00 pm - 5:00 pm** **Rm: 309**

Do you run place-and-route? Do you use a multi-V_t library? Do you care about leakage power? Two leakage power reduction methods make sense for every design: proper library selection during place-and-route; and final-pass optimization to refine threshold voltage (V_t) cell selection from a multi-V_t library.

This tutorial provides an overview of how cell design and block design contribute various components of power, and describes importance of cell selection on final quality of results. The tutorial also examines the advantages and tradeoffs of running place-and-route tools using all low-V_t cells, all high-V_t cells, or mixed-V_t cells.

Participants will run Prolific's ProPower product, using ARM Physical IP Libraries and Synopsys' PrimeTime, to minimize leakage power. This method takes a fully placed-and-routed design, previously optimized by other leakage power reduction tools, and guarantees 25% to 70% improvement without impacting area, TNS, WNS, or active power of the design.

Hands-on Tutorials

Low Power and Power Management Design Using Multi-Voltage Design and Verification Tools

Presented By: *ArchPro Design Automation, Inc.*

Thursday, July 27 **9:00 am - 12:00 pm** **Rm: 309**

Power management is no longer a clock gating play. Complex SoCs need multiple voltage frequency points and multiple sleep states to deliver the best power-performance metrics. Voltage represents the most fundamental and effective control on power and peformance of CMOS. However, there is a small problem: existing EDA tools and design languages do not deal with variable voltage. The IC industry is rapidly adopting multi-voltage designs of various styles, but the EDA tools are just emerging. Further, many IC designers themselves don't comprehend that they are adopting multi-voltage and end up missing the complexity of their IC.

This tutorial explores the following topics (with live examples).

1. What are the various styles of multi-voltage designs and their implications?
a. How are power/performance tradeoffs made.
2. How does multi-voltage change the design flow?
3. How to verify a multi-voltage design? How do you measure coverage?
a. Common multi-voltage errors and how to debug them
4. How to automate the implementation of a multi-voltage design?
5. Voltage rules and their application all through the design flow
6. Impact on DFT, libraries and IP.

ArchPro tools along with industry standard tools will be used in the live exercises.

Low Power Design - Designer's Perspective

Presented By: *Virage Logic, Cadence Design Systems, Inc., Sandbridge Technologies*

Thursday, July 27 **2:00 pm - 5:00 pm** **Rm: 309**

Power reduction is becoming a mainstream requirement that is affecting most designs at 90nm and below. Typical low power design techniques such as clock gating and mixed-Vt optimization are not adequate enough, calling for more aggressive power reduction methods. In addition to impacting design implementation and library development, aggressive power saving techniques also affects testability and functional verification. This tutorial will demonstrate how an actual low power design requirement can be met by taking a design through implementation.

Attendees will take an example dual-tone multi-frequency design through physical implementation using the Cadence® Encounter® digital IC design platform low power design flow and Virage Logic Ultra-Low-Power Semiconductor IP. Advanced power reduction techniques such as multiple supply voltages to reduce power consumption in lower performance blocks and power gating to shut off idle blocks for dramatic power reduction will also be highlighted.

Sponsors

The 43rd Design Automation Conference is sponsored by IEEE/CASS /CANDE/CEDA (Institute of Electrical and Electronics Engineers/Circuits and Systems Society), the ACM/SIGDA (Association for Computing Machinery/Special Interest Group on Design Automation), and the EDA Consortium (Electronic Design Automation Consortium). Membership information is available on the sponsors web site or at the conference at the ACM and IEEE booths.

IEEE Circuits and Systems Society

The IEEE Circuits and Systems Society (CASS) is one of the largest societies within IEEE and in the world devoted to the analysis, design, and applications of circuits, networks, and systems. It offers its members an extensive program of publications, meetings and technical and educational activities, encouraging an active exchange of information and ideas. The Society's peer reviewed publication activities include: Trans. on CAD; Trans. on CAS-Part I (Regular Papers); Trans. on CAS-Part II (Express Briefs); Trans. on VLSI; Trans. on CAS for Video Technology; Trans. on Multimedia; and the new Transactions on Mobile Computing which is co-sponsored with IEEE sister societies. CASS also sponsors or co-sponsors a number of international conferences, which include the Design Automation Conference (DAC), the Int'l Conference on Computer-Aided Design (ICCAD) and the Int'l Symposium on Circuits and Systems (ISCAS). A worldwide comprehensive program of advanced workshops including a new series on "Emerging Technologies in Circuits and Systems", as well as our continuing education short courses bring to our worldwide membership the latest developments in cutting-edge technologies of interest to industry and academia alike. The IEEE/CASS has been serving its membership for over 50 years with such member benefits as:

- Discounts on all Society publications, conferences and workshops (including co-sponsored and sister society publications and conferences)
- The Society Magazine which includes articles on emerging technologies, society news and current events
- Opportunities to network with peers and experts within our 17 focused committee meetings, the local events of over 60 chapters and more than 20 annual conferences/workshops
- Opportunity to read and review papers, write articles and participate in the Society's government
- And all the personal and professional benefits of IEEE/CASS /CANDE membership

Computer Aided Network Design (CANDE)

is a joint technical committee of the IEEE Circuits and Systems Society and the Council on Electronic Design Automation. CANDE is dedicated to bringing design automation professionals together to further their education, to assist in building relationships, and to sponsor initiatives which grow the CAD/EDA industry. CANDE sponsors a workshop in the Fall to address emerging technologies and to provide an opportunity for the generation of new ideas. CANDE is the sponsoring technical committee from CASS for both DAC and ICCAD.

For more information, please contact the IEEE/CASS/CANDE.

Mail: IEEE/CASS
445 Hoes Ln.
Piscataway, NJ 08854
Phone: 732-465-5853
Email: cas-info@ieee.org
Web: www.ieee-cas.org

The Council on Electronic Design Automation (CEDA)

The Council on Electronic Design Automation (CEDA) is an IEEE Council recently formed by the IEEE Technical Activities Board. CEDA aims to bring together the EDA-related activities that run through many of the IEEE's societies, conferences and workshops. CEDA's responsibilities include sponsorship of several conferences and publications, such as ICCAD, DAC, and the Transactions on CAD and the sponsorship of a Distinguished Speaker Series. Members of CEDA include the IEEE Antennas and Propagation, Computer, Circuits and Systems, Electron Devices, Microwave Theory and Techniques, and Solid State Circuits Societies. For more information on CEDA or to sign up for CEDA newsletters, go to www.ieee-ceda.org.

Sponsors

ACM/SIGDA -The Resource for EDA Professionals

ACM/SIGDA (Special Interest Group on Design Automation) has a long history of supporting conferences and the EDA profession. In addition to sponsoring DAC, SIGDA sponsors ICCAD, DATE, and ASP-DAC, plus approximately 15 smaller symposia and workshops. SIGDA provides a broad array of additional resources to our members, to students and professors, and to the EDA profession in general. SIGDA organizes the University Booth and Ph.D. Forum at DAC and the CADathlon at ICCAD, and funds various scholarships and awards (including the IEEE/ACM William J. McCalla ICCAD Best Paper Award). Other benefits provided to SIGDA members include the SIGDA's E-Newsletter (containing information on upcoming conferences and funding opportunities), emailed to SIGDA members twice each month. The SIGDA E-Newsletter also includes SIGDA News which highlights most relevant events in EDA and semiconductor industry and the NEW "What is...?" column that brings to the attention of EDA professionals the most recent topics of interest in design automation.

SIGDA has pioneered electronic publishing of EDA literature, beginning with the DA Library in 1989, which captured 25 years of EDA literature onto an archival series of CDROMs. In the early 1990s, SIGDA published the first EDA conference proceedings on CDROMs, and now produces CDROM proceedings for most of the major EDA conferences and symposia each year. SIGDA also produces an annual DVD Compendium of those proceedings, and more recently, Multimedia Monographs based on talks at DAC and ICCAD. Finally, SIGDA provides strong support for the ACM journal TODAES (Transactions on Design Automation of Electronic Systems).

For further information on SIGDA's programs and resources, see http://www.sigda.org. In addition, SIGDA members may also want to consider joining our parent organization, ACM. ACM membership provides access to a variety of ACM products and resources, including discounts on conferences, subscriptions to ACM journals and magazines, and the ACM Digital Library, an invaluable IT resource. For further details, see ACM's home page at http://www.acm.org.

As an EDA professional, isn't it time YOU joined SIGDA?

The Association for Computing Machinery (ACM)

ACM is an educational and scientific society uniting the world's computing educators, researchers and professionals to inspire dialogue, share resources and address the field's challenges. ACM strengthens the profession's collective voice through strong leadership, promotion of the highest standards, and recognition of technical excellence. ACM supports the professional growth of its members by providing opportunities for life-long learning, career development, and professional networking. For more information, please visit http://www.acm.org

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Additionally, ACM has 34 Special Interest Groups (SIGs) that focus on different computing disciplines. More than half of all ACM members join one or more of these Special Interest Groups. The SIGs publish newsletters and sponsor important conferences such as SIGGRAPH, OOPSLA, DAC, SC and CHI, giving members opportunities to meet experts in their fields of interest and network with other knowledgeable members. http://www.acm.org/sigs

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Hours of operation are from 8:30 am - 4:30 pm Eastern Time.

Sponsors/Univ. Booth/Proceedings

SIGDA/DAC University Booth

Each year SIGDA organizes the University Booth. The booth is an opportunity for university researchers to display their results and to interact with visitors from industry. Priority is given to presentations that complement the conference technical program. Demos that highlight benchmark results are also encouraged. The Design Contest winners, DAC speakers, and PhD Forum participants are invited to give demonstrations presenting their work at the University Booth. The schedule of presentations will be published at the conference and will also be available on the SIGDA web site. We thank the Design Automation Conference for its continued support of this project.

EDA Consortium

The EDA Consortium is the international association of companies that provide tools and services that enable engineers to create the world's electronic products.

EDA Consortium addresses issues that are common to its members and the community they serve. Recent accomplishments include simplification of international EDA export regulation and publication of an industry Operating Systems Roadmap.

Companies that become EDA Consortium members are eligible for a 10% discount on DAC Exhibit Space. Visit www.edac.org or call 408-287-3322 today to learn more about EDA Consortium membership opportunities. Send an email to karla@edac.org to be added to the Consortium's executive event invitation list.

43rd DAC Proceedings

The 43rd DAC proceedings will contain nearly 200 papers, panels, and special sessions. DAC is offering each conference and student registrant 43 years of DAC proceedings on DVD. One hardbound copy of this year's proceedings will be available to registrants for $50 at the time of registration. If you wish to purchase additional copies, you may do so at the ACM kiosk located in the North Hall on the exhibit floor level via self-help on-line computer orders. After the conference, mail orders should be sent to ACM or IEEE. The addresses for mail orders are:

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Awards

Marie R. Pistilli Women in EDA Achievement Award

• **Ellen J. Yoffa** - *Director of Next Generation Web, IBM T.J. Watson Research Center, Yorktown Heights, NY*

For her significant contributions in helping women advance in the field of EDA technology.

The P.O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering

The objective of the P.O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under-represented groups (women, African American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship and SIGDA continues to administer the program for DAC. DAC normally funds two or more $4000 scholarships, renewable up to five years, to graduating high school seniors.

The 2006 winners are:

Katlyn DeLuca - attending University of Massachusetts, Lowell, MA

Eletha Flores - attending Massachusetts Institute of Technology, Cambridge, MA

For more information about the P.O. Pistilli scholarship, contact Dr. Cherrice Traver, ECE Dept., Union College, Schenectady, NY 12308. email: traverc@union.edu

DAC/ISSCC Student Design Contest Winners

Operational Chip Design Category: 1st Place (Best Overall)

A 10.6mW/0.8pJ Power-Scalable 1 GS/s 4b ADC in 0.18um CMOS with 5.8GHz ERBW

Pierluigi Nuzzo, Fernando De Bernardinis, Pierangelo Terreni - *University of Pisa*
Bert Gyselinckx, Liesbet Van der Perre, Geert Van der Plas - *IMEC*

Design Automation Conference Graduate Scholarships

Each year the Design Automation Conference sponsors several $24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in "design and test automation of electronic and computer systems". Each scholarship is awarded directly to a university for the Faculty Investigator to expend in direct support of one or more DA graduate students.

The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are: the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Prof. Jennifer L. Dworak - *Division of Engineering–Electrical Sciences and Computer Engineering, Brown University, Providence, RI*

Student: **Elif Alpaslan**

A Statistical Coverage Metric and Stimulus Generation Approach for Design Verification Based upon Structural Analysis of the Design and Stimulus

Prof. Daniel Kroening - *Computer Systems Institute, Swiss Institute of Technology, Zurich, Switzerland*

Student: **Vijay D'silva**

Automatic Detection of Multi-Cycle Paths in Large Circuits

Information on next year's DAC scholarship award program will be available on the DAC web site: http://www.dac.com.

Awards

The ACM Transactions on Design Automation of Electronic Systems (TODAES) 2006 Best Paper Award

Zero Cost Indexing for Improved Processor Cache Performance • Volume 11, Issue 1, January 2006, Pages 3-25

Tony Givargis - *University of California, Irvine, CA*

The Association for Computing Machinery/Special Interest Group on Design Automation (ACM/SIGDA) Distinguished Service Award

• **Robert A. Walker** - *Kent State University, Kent, OH*

For dedicated service as SIGDA Chair (2001 - 2005), and over a decade of service to SIGDA, DAC, and the EDA profession

2005 Phil Kaufman Award for Distinguished Contributions to EDA

• **Phil Moorby** - *Chief Scientist, Synopsys, Inc.*

Phil Moorby is the recipient of the prestigious EDA Consortium 2005 Phil Kaufman Award for industry contributions as the inventor of the Verilog hardware design language (HDL) which has become, and today remains, one of the world's most popular electronic design languages.

IEEE Circuits and Systems Society 2006 Education Award

• **Wayne Wolf** - *Princeton University, Princeton, NJ*

For outstanding education and leadership in VLSI systems and embedded computing

IEEE Circuits and Systems Society 2006 Industrial Pioneer Award

• **John A Darringer** - *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*

For the development of practical techniques and algorithms for automated logic synthesis, for their realization as usable tools, and for their successful application to high performance computing products

IEEE Circuits and Systems Society 2006 Donald O. Pederson Award

Embedded Deterministic Test • IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 23, no. 5, pp. 776-792, May 2004

Janusz Rajski – *Mentor Graphics Corp., Wilsonville, OR*
Jerzy Tyszer – *Poznan University of Technology, Poznan, Poland*
Mark Kassab – *Mentor Graphics Corp., Wilsonville, OR*
Nilanjan Mukherjee – *Mentor Graphics Corp., Wilsonville, OR*

IEEE Circuits and Systems Society 2006 CSVT Transactions Best Paper Award

Complexity Scalable Motion Compensated Wavelet Video Encoding • IEEE Transactions on Circuits and Systems for Video Technology, vol. 15, no. 8, pp. 982-993, August 2005

Deepak Srinivas Turaga – *Philips Research USA, Briarcliff Manor, NY*
Mihaela van der Schaar-Mitrea – *Philips Research USA, Briarcliff Manor, NY*
Beatrice Pesquet-Popescu – *Telecom Paris, Paris Cedex 13, France*

IEEE Circuits and Systems Society 2006 VLSI Transactions Best Paper Award

A Process-Tolerant Cache Architecture for Improved Yield in Nanoscale Technologies • IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, no. 1, pp. 27-38, January 2005

Amit Agarwal – *Intel Corp., Hillsboro, OR*
Bipul C. Paul – *Purdue University, West Lafayette, IN*
Hamid Mahmoodi – *San Francisco State University, San Francisco, CA*
Animesh Datta – *Purdue University, West Lafayette, IN*
Kaushik Roy – *Purdue University, West Lafayette, IN*

Awards

2006 IEEE Fellows

• **Charles Alpert** - *IBM Corp., Austin, TX*
For contributions to physical design automation of very large scale integrated (VLSI) circuits

• **Wolfgang Kunz** - *University of Kaiserlautern, Kaiserlautern, Germany*
For contributions to hardware verification, very large scale integrated (VLSI) circuit testing and logic synthesis

• **Resve Saleh** - *University of British Columbia, Vancouver, BC, Canada*
For contributions to mixed-signal integrated circuit simulation and design verification

• **Chuan-Jin Richard Shi** - *University of Washington, Seattle, WA*
For contributions to computer-aided design of mixed-signal integrated circuits

• **Martin Wong** - *University of Illinois at Urbana-Champaign, Urbana, IL*
For contributions to algorithmic aspects of computer-aided design (CAD) of very large scale integrated (VLSI) circuits and systems

Best Paper Candidates

Twelve papers were nominated by the Technical Program Committee as a DAC Best Paper Candidate; six in front-end design and six in back-end design. Final decisions will be made after the papers are presented at the conference. The awards for the best papers, one in front-end design and one in back-end design, will be presented at 12:45 on Thursday, July 27 in the Gateway Ballroom, just before the Keynote Address.

Session 3.1 A CPPLL Hierarchical Optimization Methodology Considering Jitter, Power and Locking Time

Session 8.1 Charge Recycling in MTCMOS Circuits: Concept and Analysis

Session 9.1 A Multiprocessor System-on-Chip for Real-Time Biomedical Monitoringand Analysis: Architectural Design Space Exploration

Session 13.1 Power Grid Physics and Implications for CAD

Session 13.2 Fast Analysis of Structured Power Grid by Triangularization BasedStructure Preserving Model Order Reduction

Session 14.2 SAT Sweeping Using Local Observability Don't-Cares

Session 19.2 Timing-Based Delay Test for Screening Small Delay Defects

Session 24.1 BoxRouter: A New Global Router Based on Box Expansion and Progressive ILP

Session 28.2 Register Binding for Clock Period Minimization

Session 30.1 Architecture-Aware FPGA Placement using Metric Embedding

Session 31.1 VIRTUS: A New Processor Virtualization Architecture forSecurity-Oriented Next-generation Mobile Terminals

Session 39.1 A Constraint Network Based Solution to Code Parallelization

Student Design Contest

DAC/ISSCC Student Design Contest

The Student Design Contest promotes excellence in the design of electronic systems by providing a competition for graduate and undergraduate students at universities and colleges. It is co-organized by ISSCC and DAC. This year we received over 50 submissions in three categories: Conceptual, Operational Chip, and Operational Systems. Operational designs are those which have been implemented and tested. Conceptual designs have not yet been fabricated and tested but must have been thoroughly simulated. Students compete for cash prizes donated by industrial supporters, as well as the DAC conference. winners have been invited to show their work at the University Booth on the show floor. Awards will be given at the DAC Pavilion on Wednesday, July 26, 2006 from 10:00 am - 10:45 am. The ceremony will include brief overview presentations from each winning project team.

DAC/ISSCC 2006 Student Design Contest Winners

Operational Chip Design Category:

1st Place **A 10.6mW/0.8pJ Power-Scalable 1 GS/s 4b ADC in 0.18um CMOS with 5.8GHz ERBW** **(Best Overall)**

Pierluigi Nuzzo, Fernando De Bernardinis, Pierangelo Terreni - *University of Pisa*
Bert Gyselinckx, Liesbet Van der Perre, Geert Van der Plas - *IMEC*

(tie) **2nd Place** **Increasing the Time Dynamic Range of Pulse Measurement Techniques in Digital CMOS**

Mona Safi-Harb, Gordon W. Roberts - *McGill University*

(tie) **2nd Place** **A DSP Enabled Microsystem for Cochlear Implants with Hybrid LC Clocking**

Eric D. Marsman, Robert M. Senger - *University of Michigan*
Richard B. Brown-*University of Utah*

3rd Place **A 160K Gates/4.5KB SRAM H.264 Video Decoder for HDTV Applications**

Chien-Chang Lin, Jia-Wei Chen, Hsiu-Cheng Chang, Chao-Ching Wang, Yi-Huan Ou-Yang, Ming-Chih Tsai, Yao-Chang Yang, Jiun-In Guo, Jinn-Shyan Wang - *National Chung ChengUniversity*

Conceptual Category:

1st Place **ASIC Implementation of LDPC Decoder Accelerating Message-Passing Schedule**

Kazunori Shimizu, Tatsuyuki Ishikawa, Nozomu Togawa, Takeshi Ikenaga, Satoshi Goto - *Waseda University*

Operational System Design Category:

1st Place **Demonstration of Uncoordinated Multiple Access in Optical Communications**

Herwin Chan, Andres I. Vila Cadaso, Juthika Basak, Miguel Griot, Wen-Yen Weng, Richard Wesel, B. Jalali, Eli Yablonovitch- *University of California, Los Angeles*
Ingrid Verbauwhede - *University of California, Los Angeles and K.U. Leuven, Belgium*

2nd Place **Illumimote: A High Performance Light Sensor Module for Wireless Sensor Networks**

Heemin Park, Jonathan Friedman, Mani B. Srivastava, Pablo Gutierrez, Vidyut Samanta, Jeff Burke - *University of California, Los Angeles*

3rd Place **An Ultra Low Power Wireless Micro-Sensor Node**

Denis Daly, Daniel Finchelstein, Nathan Ickes, Naveen Verma, Anantha Chandrakasan - *Massachusetts Institute of Technology*

Honorable Mention **Phase Delay Based Collision Avoidance RADAR for Smart Automobiles**

Babu L. Saincha - *Indian Institute of Information Technology*

Award Contributors:

Additional Meetings

SystemC Technology Symposium
Monday, July 24 • 12:00 pm - 1:30 pm **Rm: 200-212**

The Open SystemC Initiative (OSCI) invites you to learn how recent advancements in SystemC apply to you today and moving forward:

Hear from industry experts on recent SystemC advancements and using SystemC for doing real world system-level design. Status updates on the technology roadmap, IEEE 1666 and TLM will be presented. (complimentary lunch provided)

ACM/SIGDA Symposia/Workshop Leaders Luncheon
Monday, July 24 • 12:00 pm - 2:00 pm **Rm: 124**

Organizers of symposia and workshops sponsored by ACM/SIGDA, as well as ACM/SIGDA volunteers are invited to a lunch get-together. ACM staff and SIGDA Board Members will be available for detailing and explaining the steps of starting or organizing an event. A brief overview of other new ACM/SIGDA activities will be presented.

How Many Engineers Does It Take? The Real Issues in IP Integration
Monday, July 24 • 12:30 pm - 2:00 pm **Rm: 111**

Free lunch panel. IP integration and verification is only getting more complex, expensive, and risky. IP suppliers, integrators, EDA vendors, and foundries must work together in a streamlined fashion to ensure IP success. But are they? Varying degrees of IP quality coupled with a host of business and technical issues makes IP integration the key challenge in modern SoCs. Don't be left holding the cards with your next chip design. This panel will expose the interrelated and often opposing technical and business issues surrounding IP integration and explore how this fragmented industry can work together.

NASCUG Meeting
Monday, July 24 • 2:00 pm - 6:00 pm **Rm: 200-212**

You are invited to the 5th North American SystemC Users Meeting (NASCUG):

Open to DAC attendees, the focus of the NASCUG meeting is on SystemC real-world design methodologies and user experiences. Topics include techniques for integrating SystemC into the design flow and SystemC tool flows and methodologies. (reception starts at 5:00 pm)

CEDA Distinguished Speaker Reception
Monday, July 24 • 5:30 pm - 7:30 pm **Rm: 124**

CEDA Distinguished Speaker Series, beer/wine/cheese, followed by the TCAD Donald O. Pederson Best Paper Award winner entitled, *Embedded Deterministic Test* by **J. Rajski, J. Tyszer, M. Kassab, N. Mukherjee**

Si2 Members Meeting
Monday, July 24 • 6:00 pm - 7:30 pm **Rm: 111**

The annual Silicon Integration Initiative (Si2) Members Meeting will provide an overview and status report on Si2 projects, such as the OpenAccess Coalition, the Open Modeling Coalition, the Design-to-Manufacturing Coalition, the Design Technology Council, the Liberty TAB, and the LEF/DEF Governing Board. The newly-elected Si2 Board of Directors will be introduced, and industry trends are explored. Companies considering joining Si2 are welcome to attend. Refreshments and snacks will be served before and after the meeting. Please contact Bill Bayer (wbayer@si2.org) if you would like to attend.

The SPIRIT Consortium General Meeting
Monday, July 24 • 6:00 pm - 8:00 pm **Rm: San Francisco Marriott Hotel**

At DAC 2006, The SPIRIT Consortium will provide a major opportunity to hear about The Consortium's specifications and see them applied in practice by multiple users and vendors. Please join us to hear presentations on the released specifications, The Consortium roadmap and proposed IEEE 1685 standard, and see in-use demonstrations of the specifications. Enjoy a brief repast and cocktail hour on behalf of The SPIRIT Consortium! You may register your interest to attend this general meeting by emailing info@spiritconsortium.org.

Synopsys/Sun University Reception
Monday, July 24 • 6:30 pm - 8:30 pm **Rm: 228/230**

University professors and students are invited to join Synopsys and Sun Microsystems for an evening reception including drinks and hors d'oeuvres. Prize drawings will be held throughout the evening and the following keynote presentations will be featured.

The Future is BDA, Dr. Richard Newton, Dean of Engineering, Univ. of California, Berkeley

Design For Testability: The Path to Deep Submicron, Tom W. Williams, Synopsys Fellow

Not sure what BDA is? Join us to find out.

Additional Meetings

Industry Standard IP Protection System for EDA Tool Flows

Tuesday, July 25 • 7:30 am - 9:15 am **Rm: 302**

IP Vendors require security; Chip Designers require interoperability across many tools. Can one methodology satisfy both? This panel will discuss a methodology and its underlying technology that achieves these goals. Panelists from IC vendors, EDA companies, and IP providers will discuss their unique requirements and concerns and will highlight the flexibility and security necessary for an industry standard methodology to emerge. Key panel topics:

- The underlying technology
- IP provider control for the level to which their IP is visible to EDA tools and users
- Advantages of using a non-proprietary encryption mechanism
- EDA vendor requirements

SPICE and FastSPICE: The Next 25 Years
Synopsys Analog Mixed Signal Breakfast Event

Tuesday, July 25 • 7:30 am - 10:00 am **Rm: Marriott: Golden Gate Hall Salon B1**

Synopsys invites you to attend Synopsys' Analog Mixed Signal breakfast program on the future of SPICE and FastSPICE. HSPICE is celebrating it's 25 year anniversary. Come and hear what the industry experts predict the next 25 years have in store for SPICE and FastSPICE challenges. For more information and to register visit: http://www.synopsys.com/ams_breakfast

Brion Technology Lunch Seminar

Tuesday, July 25 • 11:30 am - 2:00 pm **Rm: 111**

Two levers that are improving the resolution and manufacturability of ultra sub wavelength patterns: one is immersion, the other is improving patterning by computational lithography. Computational lithography is used to apply and verify pattern proximity corrections and sub-resolution assist features to full-chip layouts - processes such as SRAF placement, model-based RET/OPC and model-based RET/OPC verification. Re-mapping the problem into an image-based approach allows the application of repetitive grid-based calculations to be hard coded in dedicated computing boards. The combination of the image-based approach and high speed dedicated computing hardware is revolutionizing all aspects of model-based RET/OPC.

SIGDA Ph. D. Forum/Member Meeting

Tuesday, July 25 • 6:30 pm - 8:00 pm **Rm: 310**

SIGDA invites you to attend our annual PhD Forum and Member Meeting. SIGDA members are invited, as we are all members of the EDA Community. We will begin with a presentation of SIGDA's programs and this year's SIGDA Technical Leadership Awards, but the main focus of the meeting will be the Ph.D. Forum. Aimed at strengthening ties between academia and industry, students will present posters and discuss their Ph.D. dissertation research with interested attendees. The Ph.D. Forum gives students feedback on their research, and gives the EDA community a preview of work in process. Also, light refreshments will be served at 7:30 pm. For more information, see http://www.sigda.org/daforum.

Additional Meetings

Escape from Analog Alcatraz through OpenAccess Synopsys Interoperability Breakfast Event

Wednesday, July 26 • 7:30 am - 9:30 am **Rm: 302**

Chi-Foon Chan, President/COO of Synopsys, invites you to attend Synopsys' interoperability breakfast. Speakers including Philippe Magarshack, Front-End Technology and Manufacturing Group VP and GM of Central CAD and Design Solutions at STMicroelectronics, and Jim Hogan, Industry Veteran, discuss the benefits and challenges of enabling interoperability for analog and custom design through OpenAccess. Find out who wins the annual Tenzing Norgay Interoperability Achievement Award. For more information and to register, visit www.synopsys.com/interop/breakfast

Lessons from the Trenches Real-World ESL Project Experiences - Are the Advantages Worth the Cost and Effort?

Wednesday, July 26 • 12:00 pm - 2:00 pm **Rm: 228 & 230**

A panel of users and tools vendors will discuss real world examples of how electronic system level design tools and methodologies are being used today to improve quality, reduce risk and improve time-to-market. Issues to be addressed:
• The usability of the current generation of ELS tools • The amount of training/support required to achieve productivity with ESL point tools • What it takes to put together and support a cost effective • ESL flow • What are the quantifiable benefits of the ESL flow • What has worked/what has not • Next steps in ESL for each panel member's company
For more information or to register contact r.monge@vastsystems.com

ACM TODAES Editorial Board Meeting

Wednesday, July 26 • 12:00 pm - 2:00 pm **Rm: 112**

Annual Editorial Board meeting of the ACM Transactions on Design Automation of Electronic Systems (ACM TODAES).

Fourth Annual Hacks and Flacks Roundtable Discussion at DAC

Wednesday, July 26 • 3:00 pm - 4:30 pm **Rm: 302**

Hours, days and weeks are spent strategizing and agonizing over public relations and marketing plans. Once plans are finalized, a large amount of money is invested on implementation. Time, effort and company dollars are spent with the goal of reaching "key" customers and gaining the attention of various audiences. BUT…do we? Does our message reach the audience who ultimately makes or breaks the sales decisions? Where do your customers get their information? What makes a positive impression on customers for EDA and IP products? What direct effect does public relations have on sales and other corporate departments? Please join us for a lively discussion among EDA customers such as Texas Instruments, STMicroelectronics and Atheros Communications along with public relation and marketing professionals to discuss these questions and find out what they read and what media they believe most influences their purchase and investment decisions.

CANDE Meeting

Wednesday, July 26 • 6:00 pm - 7:30 pm **Rm: 112**

CANDE is a joint Technical Committee on Design Automation for the IEEE Circuits and Systems Society (CASS) and the Council on Electronic Design Automation (CEDA). It is the sponsoring committee from CASS and CEDA for both ICCAD and DAC. CANDE brings design automation professionals together to build relationships, and to sponsor a workshop and initiatives that improve the CAD/EDA industry. Please visit the CANDE website: (http://www.cande.net/) for more information.

Birds-of-a-Feather (BOF) Meetings

Wednesday, July 26 • 6:30 pm - 8:00 pm

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather". All BOF meetings are held at The Moscone Center, Wednesday, July 26, 6:30 pm - 8:00 pm. DAC will facilitate common interest group meetings to discuss DA related topics. To arrange a BOF meeting sign up at the Information Desk located in the lower North Lobby. A room will only be assigned if ten or more people sign up. An LCD projector and screen will be provided. Check DACnet and the Birds-of-a-Feather board at the Information Desk.

The 43rd Design Automation Conference • July 24 - 28, 2006 • San Francisco, CA

44th Call For Papers

DAC is the premier conference devoted to Design Automation (DA) and the application of DA tools in designing electronic systems. Four types of submissions are invited: regular papers, special topic sessions, panels, and tutorials. Submissions must be made electronically at www.dac.com. **Regular Papers are due NO later than 5:00 pm MST, November 20, 2006.**

DAC 2007 is seeking papers that deal with design tools, design methods, design techniques, and embedded design in a number of categories described below.

Design Tools papers describe contributions to the research and development of design tools and their supporting algorithms.

Design Methods and case studies papers describe innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art design projects.

Design Papers describe the use of design tools and methods from the perspective of a specific design project. They include a brief description of the design and discussion of: methodology, flow, innovative use of tools, the limits of current tools, and what new tool capabilities are required for future designs.

Embedded Systems are characterized by mixed hardware and software components with limited resources. Increases in software content introduce new system design issues. Embedded design papers describe tools, methods, and case studies for applications with specific embedded system content.

The theme topic for DAC 2007 is automotive electronics, and papers that specifically refer to the theme will be highlighted at the conference.

Requirements for Submission

Regular paper submissions MUST (1) be in PDF format only, (2) contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission, (3) be no more than 6 pages (including the abstract, figures, tables, and references), double columned, 9pt or 10pt font, and (4) MUST NOT include name(s) or affiliation(s) of the author(s) anywhere on the manuscript or abstract, and any references to the author(s)'s own previous work or affiliations in the bibliographic citations must be in the third person. Format templates are available on the DAC web site for your convenience, but are not required. Submissions not adhering to these rules, or those previously published or simultaneously under review by another conference, will be rejected. DAC will work cooperatively with other conferences and symposia in the field to check for double submissions. Additional submission guidelines are available on the DAC website (after September 1, 2006). All regular papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage. Authors of accepted papers must sign a copyright release form for their paper. Notice of acceptance will be sent via email by March 9, 2007.

Special session submissions must include descriptions of suggested papers and speakers, and the importance of the special session to the DAC audience. DAC reserves the right to restructure all special sessions. **Special session submissions are due NO later than 5:00 pm MST, November 1, 2006**

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panel and tutorial proposals.**Panel and tutorial suggestions are due NO later than 5:00 pm MST, November 1, 2006**

Students are invited to submit descriptions of original electronic designs, either circuit level or system level. **Student Design Contest paper submissions** must (1) be in PDF format only, (2) contain the title of the project, (3) contain an abstract of approximately 60 words, (4) a complete description of the project, and (5) be no more than 6 pages (including the abstract, maximum of 10 figures/tables and references), double columned, 9pt or 10pt font. The submission should clarify the originality, distinguishing features, and measured performance of the design. Three categories of designs - operational, system and conceptual - are eligible for awards. For operational designs, proof-of-implementation is required, while for conceptual designs, complete simulation and test plan is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2005. Submitted designs should not have received awards in other contests. Selected designs will be presented at the conference (and at ISSCC in February 2007). Additional contest rules are available on the DAC web site. **Student Design Contest submissions are due NO later than 5:00 pm MST, December 6, 2006**

ALL SUBMISSIONS MUST BE MADE ELECTRONICALLY AT THE DAC WEB SITE: WWW.DAC.COM

44th Call For Papers

Submitters are required to specify a category from the 18 listed below.

1. System-Level Design and Co-Design
1.1 System specification, modeling, simulation, and performance analysis
1.2 Scheduling, HW-SW partitioning
1.3 IP and platform-based design, IP protection
1.4 System-on-Chip (SoC) and Multi-processor SoC (MPSoC)
1.5 Application-specific processor design tools

2. System-Level Communication and Networks on Chip
2.1 Modeling and performance analysis
2.2 Communications-based design
2.3 Architectural synthesis, mapping, routing, scheduling
2.4 Optimization for energy, fault-tolerance, reliability
2.5 Interfacing and software issues
2.6 NoC Design methodologies and CAD flows, case studies and prototyping

3. Embedded HW Design and Applications
3.1 Case studies of embedded system design
3.2 Flows and methods for specific applications and design domains

4. Embedded SW Tools and Design
4.1 Retargetable compilation
4.2 Memory/cache optimization
4.3 Real-time single- and multi-processor scheduling, linking, loading
4.4 Real-time operating system

5. Power Analysis and Low-Power Design
5.1 System level power design and thermal management
5.2 Embedded low-power approaches: partitioning, scheduling, and resource management
5.3 High-level power estimation and optimization
5.4 Gate-level power analysis and optimization
5.5 Device, circuit techniques for low-power design

6. Verification
6.1 Functional, transaction-level, RTL, and gate-level modeling and verification of hardware design
6.2 Dynamic simulation, equivalence checking, formal (and semi-formal) verification model and property checking
6.3 Emulation and hardware simulators or accelerator engines
6.4 Modeling languages and related formalisms, verification plan development and implementation
6.5 Assertion-based verification, coverage-analysis, constrained-random testbench generation

7. High-Level Synthesis
7.1 High-level, behavioral, algorithmic, and architectural synthesis, "C" to gates tools and methods
7.2 HW-SW interface synthesis, communication and network synthesis
7.3 Synthesis of digital circuits above the RTL level
7.4 Resource scheduling, allocation, and synthesis

8. Beyond Die-Integration and Package/Hybrid/Board Design
8.1 Chip-package-board codesign
8.2 System-in-Package, 3D design, stacked devices
8.3 Beyond-the-die communication, high-speed I/O, optical communication
8.4 Analysis and optimization (signal integrity, physical layout, simulation) beyond the die

9. Logic Synthesis and Circuit Optimization
9.1 Combinational, sequential, and asynchronous logic synthesis
9.2 Library mapping, cell-based design and optimization
9.3 Transistor and gate sizing and resynthesis
9.4 Interactions between logic design and layout or physical synthesis

10. Circuit Simulation and Interconnect Analysis
10.1 Electrical-level circuit simulation
10.2 Model-order reduction methods for linear systems
10.3 Interconnect and substrate modeling and extraction
10.4 High-frequency and electromagnetic simulation of circuits
10.5 Thermal and electrothermal simulation

11. Timing Analysis and Design for Manufacturability
11.1 Design for yield, defect tolerance, cost issues, and impacts of DFM
11.2 Process technology development, characterization, and modeling
11.3 Deterministic static timing analysis and verification
11.4 Statistical performance analysis and optimization
11.5 Design for resilience under manufacturing variations

12. Physical Design and Manufacturability
12.1 Physical floorplanning, partitioning, placement
12.2 Buffer insertion, routing, interconnect planning
12.3 Physical verification and design rule checking
12.4 Automated synthesis of clock networks
12.5 Reticle enhancement, lithography-related design optimizations

13. Signal Integrity and Design Reliability
13.1 Signal integrity, capacitive and inductive crosstalk
13.2 Reliability modeling and analysis
13.3 Novel clocking and power delivery schemes
13.4 Power grid robustness analysis and optimization
13.5 Soft-errors and single-event upsets (SEUs)

14. Analog/Mixed-Signal and RF
14.1 Analog, mixed-signal, and RF design methodologies
14.2 Automated synthesis and macromodeling
14.3 Analog, mixed-signal and RF simulation and optimization

15. FPGA Design Tools and Applications
15.1 Rapid prototyping
15.2 Logical synthesis and physical design techniques for FPGAs
15.3 Configurable and reconfigurable computing

16. Testing
16.1 Test quality and reliability, nanometer technology test, current-based test
16.2 Digital fault modeling, automatic test pattern generation
16.3 Digital design-for-test, test data compression, built-in self test
16.4 Memory test and repair, FPGA testing
16.5 Fault tolerance and on-line testing
16.6 Analog/mixed-signal/RF testing
16.7 Board- and system-level test
16.8 Silicon debug, post-silicon design validation

17. New, Emerging, or Specialized Design Technologies, including but not restricted to
17.1 MEMS, sensors, actuators, imaging devices
17.2 Nano-technologies, nano-wires, nano-tubes
17.3 Quantum computing
17.4 Biologically based or biologically inspired systems
17.5 New transistor structures and devices, new or radical process technologies

18. Special Theme Topic: Automotive Electronics
18.1 Safety critical systems design: engine control, brake systems, automated highways, security systems, low tire pressure monitors, traction control, and auto distance cruise control
18.2 Bus selection and verification challenges for LIN, CAN and FlexRay
18.3 Automotive convenience factors: control systems, entertainment, communication, navigation, climate control, rain sensing, active noise cancellation, and vehicle stability
18.4 Analog mixed-signal design challenges
18.5 Automotive as an EDA driver: will automotive define ESL for EDA?
18.6 Issues with FPGA, ASIC and ASSP based design

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