43rd DESIGN AUTOMATION CONFERENCE

Strike Technology "Gold" at DAC in San Francisco

In 1849, thousands rushed to San Francisco in hopes of striking gold in California's foothills. Today, you are invited to join more than 10,000 electronic design professionals striking gold of another kind – the latest technologies and ideas. Plan today to join the rush.

ADVANCE PROGRAM

The Moscone Center
San Francisco, California
July 24-28, 2006

www.dac.com

Sponsored by:

In Technical Cooperation with:

Designs on the Future

Dear Colleague:

The 43rd Design Automation Conference comes back to San Francisco! It is an excellent venue with its proximity to many high tech companies, its beautiful location on the Bay, and a wide variety of activities and sights to enjoy. Thousands of executives, managers, designers, academics, journalists and others will converge here during DAC, which is the largest and most prestigious event focused on the design of electronic circuits and systems.

As chair, people often ask me what is new and exciting for this year. I never tire of this question as the excitement will be at a high and I enjoy talking about all the new activities, sessions, and topics on the agenda. This year's theme is Multimedia, Entertainment, and Games (MEGa) and it will be found throughout the program including in the keynotes, in several pavilion sessions, and in a full day of technical sessions on Wednesday. Topics will range from issues faced in the design of the iPod, to technology requirements for 3D graphics in feature films, to power management for next-generation media applications. Issues related to this theme have touched all of our lives and I'm delighted we are addressing this exciting area at DAC this year.

DAC's technical program, which received a record 865 regular paper submissions, will include all the favorite topics plus two new ones. Beyond-the-Die will cover issues such as chip-package co-design, system-in-package (SiP), and new integration techniques such as 3D and stacked designs. Emerging Technologies has technical contributions in the areas of nanotubes, nanowires, DNA self-assembled nanostructures, and biochips. This year we have added a seventh full-day tutorial to our tutorial schedule. Overall, the program will contain more than 200 technical presentations in 11 tracks, eight technical program panels, 18 pavilion panels, and seven full-day tutorials – all led by widely respected industry experts.

We will again offer the Management Day on Tuesday, July 25, to offer mid-and senior-level design managers a forum for sharing information on key technology trends and different decision-making processes. The exhibit floor will be very crowded and lively as we have over 240 exhibitors, many of those first-time exhibitors to DAC. We will be holding hands-on tutorials throughout the week, all in the subject area of low power design.

This year's event promises to be a huge success and a great learning experience. There will likely be a full house in The Moscone Center as we draw in more local deep-tech denizens who couldn't travel to conference locations that were further afield, so book your reservation early.

I think those attending will find that the advancements, research and insight that the global design community brings to this year's event is truly stellar, with something to interest everyone.

Whatever your path in EDA, DAC is your source for the best in networking, learning and insight.

For more detailed conference information, please visit us on-line at www.dac.com.

We would be delighted if you design DAC into your July plans. And we think you'll be delighted by the experience you'll have at this year's DAC.

Best regards,
Ellen Sentovich
General Chair, 43rd DAC

The 43rd Design Automation Conference Week in Review

Sunday, July 23	Monday, July 24	Tuesday, July 25	Wednesday, July 26	Thursday, July 27	Friday, July 28
• **UML for SoC Design Workshop**	• **FREE Monday Exhibits** • **Full-Day Tutorials** • **Hands-on Tutorials** • **Workshops** • **Exhibit Floor Happy Hour** ***(5:00 pm - 6:00 pm)***	• **General Session** • **Keynote Address** • **Technical Sessions** • **Management Day** • **Hands-on Tutorial** • **Exhibits**	• **Technical Sessions** • **MEGa Theme** • **Hands-on Tutorials** • **Exhibits** • **DAC Party** *(AT&T Ballpark)*	• **Keynote Address** • **Best Paper Awards** • **Technical Sessions** • **Hands-on Tutorials** • **Exhibits**	• **Full-Day Tutorials**

Special Functions and Social Events

Be sure to attend these DAC functions:

- ✶ Exhibit Floor Happy Hour on Monday, 5:00 pm – 6:00 pm
- ✶ DAC Wednesday Night Party at the AT&T Ballpark, 7:30 pm – 10:00 pm. Enjoy great food and libation.
- ✶ The DAC Pavilion in Booth 2228 on the Exhibit Floor – there's always something going on!
- ✶ Management Day sessions on Tuesday - see the program for details
- ✶ Keynote Speakers on Tuesday and Thursday
- ✶ MEGa (Multimedia, Entertainment, and Games) sessions throughout the technical program

DAC Technical Session Highlights...

This year's technical program was selected from the record number of 865 regular paper submissions, 78 panel submissions and 18 tutorial proposals DAC received. The result will be a full and varied program of timely technical and business-related sessions of interest to design engineers, management, developers, and researchers.

The DAC technical program is made up of 14 tutorials, 4 workshops, 18 DAC Pavilion presentations and 62 technical sessions divided into 11 tracks: Business; System-Level and Embedded Systems Design; MEGa; Low Power and Thermal; Analog and Circuit; Interconnect, Reliability and DFM; Verification and Test; Synthesis and FPGA; Physical Design; Beyond the Die; and New and Emerging Technologies.

Major front end themes include, the use of processors in more and more SoC designs, and a focus on **on-chip interconnect and communications-centric design**, including network-on-chip, the importance of optimizing software for real-time considerations and taking power and memory into account for **embedded software**, and transaction level modeling (TLM) at the **system level**, which also flows into detailed implementation and **verification**. In the verification area, there is a focus on processor-centric verification and an emphasis on the idea of verification planning, moving from formal specifications through well-defined verification processes to achieve satisfactory coverage and quality. Finally, aspects of formal verification are an active area of research with continued progress in design adoption: a session on bounded model checking and equivalence verification, and another on simulation-assisted formal verification will bring researchers and practitioners up to date with the latest work.

Design for manufacturability (DFM) continues to attract impressive work with sessions addressing the latest developments in statistical timing and power analysis methods, design-technology interactions, practical issues in DFM, and yield analysis and improvement. In the area of **low power design**, the DAC program has several sessions that discuss issues ranging from low power, thermally-aware architectures to circuit-level low power design and analysis. Research results will be presented on **signal integrity, physical design, and reliability** to solve recent problems brought up by technology scaling with sessions on topics such as power grid design, routing and buffer insertion, and soft error mitigation.

Besides these topics, numerous others – such as **analog circuit design and CAD, logic and high-level synthesis, and FPGA/reconfigurable circuit issues** – find prominence in the schedule.

New at DAC this year are the **MEGa (Multimedia, Entertainment, & Games)** themed sessions. These sessions focus on multimedia, entertainment, and games, and offer attendees an opportunity to participate in a series of technical sessions, DAC Pavilion events, and special activities on the Exhibit Floor. These sessions will highlight CAD challenges for multimedia designs, a look at next generation **MEGa designs**, and power constraints of consumer devices. Presentations are by representatives from leading companies such as STMicroelectronics, IBM, nVidia, Pixelworks, Qualcomm, and Intel. Highlights will include discussions of the issues faced by iPod and the Cell processor, and the technology requirements for 3-D graphics in feature films.

Seven Full-Day Tutorials are planned, including two on Monday, July 24, and five on Friday, July 28. Topics presented range from ESL, SystemVerilog, DFM, variability, chip and package co-design, and techniques for design error diagnosis, silicon debug and defect diagnosis, and tools for hybrid embedded sytems.

Seven vendor-presented **Hands-on Tutorials** are scheduled throughout the conference, covering a variety of approaches to low power design methods and tools.

For the third year in a row, DAC will offer the popular **Management Day** on Tuesday, July 25, featuring a series of business and technology sessions designed to offer mid- and senior-level managers a forum for sharing information on key decision-making processes as well as current technology trends. It will include a panel discussion on the fabless model, a session on the choice of flows and implementation technologies, and a second session on the design of graphics, entertainment, and wireless products. In addition, registration for Management Day includes the EDA Business Forum Luncheon and Management Day cocktail party to give attendees the opportunity to network with their peers in the industry.

A full roster of panels and presentations is once again planned for the **DAC Pavilion** on the Exhibit Floor, open to all attendees. Gary Smith, chief analyst with Gartner Dataquest, will continue the tradition of opening the Pavilion program on Monday, July 24, with his presentation on EDA trends and "What's Hot at DAC." The Pavilion sessions will also include business-focused discussions, an "Ask the CTO" panel, the annual presentation of the Women in EDA Achievement Award, and this year's DAC/ISSCC Student Design Contest Winners.

To register online, or to print a faxable form, visit the DAC website www.dac.com. The advance conference registration discount deadline is June 26.

43rd Design Automation Conference®

UML for SoC Design Workshop, Sunday, July 23, 9:00 am - 6:00 pm, Room 302

Monday, July 24 — Free Monday Exhibit Hours 9:00 am - 6:00 pm

	Rm: 305	Rm: 304	Rm: 309	Rm: 303	Rm: 302	Rm: 301
9:00	**Tutorial 1** ESL Design Methodology Using SystemC (Breakfast 8:00 am - 9:00 am)	**Tutorial 2** Practical Aspects of Coping with Variability: An Electrical View (Breakfast 8:00 am - 9:00 am)	**Hands-on Tutorial** Analysis and Optimization of Low Power Designs *Apache Design Solutions*			
10:00					Workshop for Women in Design Automation 9:00 am – 12:45 pm	Introduction to Chips and EDA for a Non-Technical Audience 10:00 am - 12:00 pm
12:00	**Lunch** (Rm: 307)	**Lunch** (Rm: 307)			Lunch: 12:45 pm – 1:45 pm	
1:00				Second Integrated Design System Workshop: How Can We Solve the Challenges of Design System Integration 12:00 pm - 5:00 pm		
2:00	**Tutorial 1 (cont.)** ESL Design Methodology Using SystemC	**Tutorial 2 (cont.)** Practical Aspects of Coping with Variability: An Electrical View	**Hands-on Tutorial** Using Virtual System Prototypes to Optimize Architectures for Low Power and Other Key Attributes *VaST, StarCore, Greenhills*			
5:00						

Booth #2228

DAC Pavilion

- Dataquest at DAC with Gary Smith — 9:30 am - 10:30 am
- What Will it Take to Break the $4B Revenue Cap? — 11:00 am - 12:00 pm
- Ask the CTO — 1:00 pm - 2:00 pm
- Inside the iPod — 3:00 pm - 4:00 pm
- Mass Book Signing — 4:15 pm - 5:15 pm

IEEE CEDA Reception and Distinguished Speaker Lecture in Rm: 124 from 5:30 pm - 7:30 pm

Tuesday, July 25 — Exhibit Hours 9:00 am - 6:00 pm

8:30 to 10:15 — General Session and Keynote Speaker Gateway Ballroom

Structuring Process and Design for Future Mobile Communication Devices

Hans Stork - Senior Vice President and Chief Technology Officer, Texas Instruments Inc.

BREAK 10:15 am - 10:30 am

	Rm: 306/308	Rm: 307	Rm: 305	Rm: 304	Rm: 303
	Session 1	Session 2	Session 3	Session 4	Session 5
10:30 to 12:00	**PANEL:** How Will the Fabless Model Survive?	**SPECIAL SESSION:** Why Doesn't My System Work?	Hierarchical Synthesis for Mixed-Signal Designs	Processor and Communication Centric SoC Design	Practical Applications for DFM

LUNCH 12:00 pm - 2:00 pm

	Rm: 306/308	Rm: 307	Rm: 305	Rm: 304	Rm: 303	Rm: 301
	Session 6	Session 7	Session 8	Session 9	Session 10	Session 100
2:00 to 4:00	**PANEL:** The IC Nanometer Race: What Will it Take to Win?	**SPECIAL SESSION:** Bridging the System to RTL Verification Gap	Leakage, Power Analysis and Optimization	MPSoC Design Methodologies and Applications	Statistical Timing Analysis	**MANAGEMENT:** Decision-Making for Complex SoCs in Consumer Electronic Products

BREAK 4:00 pm - 4:30 pm

	Session 11	Session 12	Session 13	Session 14	Session 15	Session 150
4:30 to 6:30	**PANEL:** Entering the Hot Zone - Can You Handle the Heat and Be Cool?	**SPECIAL SESSION:** Reliability Challenges for 65nm and Beyond	Power Grid Analysis and Design	Advances in Formal Solvers	Gate Modeling and Model Order Reduction	**MANAGEMENT:** Trade-offs and Choices for Emerging SoCs in High-End Applications

Booth #2228

DAC Pavilion

- The Do's and Don'ts of Verification — 10:15 am - 11:00 am
- Design Team Collaboration: Tools Challenge or Organization Responsibility — 11:30 am - 12:15 pm
- Exporting in the Hallway — 1:00 pm - 1:45 pm
- Shattering the Glass Ceiling: A Decade of Growth for Women — 2:00 pm - 2:45 pm
- The Fabless Model: Is DFM Our Salvation or Demise? — 4:00 pm - 4:45 pm

SIGDA Ph.D. Forum in Rm: 310 from 6:30 pm - 8:00 pm

- indicates special interest to designers Presenters will be available in Rm: 310 for additional 20-minute question-and-answer periods after the session.

Session Tracks: Business | System Level & Embedded | MEGa | Low Power and Thermal | Analog and Circuit | Interconnect, Reliability and DFM | Verification and Test | Synthesis and FPGA | Physical Design | Beyond the Die | New and Emerging Technologies

Wednesday, July 26 — Exhibit Hours 9:00 am - 6:00 pm

	Rm: 306/308	Rm: 307	Rm: 305	Rm: 304	Rm: 303	Rm: 301
	Session 16	Session 17	Session 18	Session 19	Session 20	Session 21
8:30 to 10:00	**SPECIAL SESSION:** MPSoC Design Tools	**SPECIAL SESSION:** The Best of ISSCC: Multimedia	Buffer Insertion	Testing and Validation for Timing Defects	Advanced Topics in Processor and System Verification	Software for Real-Time Applications

BREAK 10:00 am - 10:30 am

	Session 22	Session 23	Session 24	Session 25	Session 26	Session 27
10:30 to 12:00	**PANEL:** Building a Standard ESL Design and Verification Methodology: Is it Just a Dream?	**INVITED SESSION:** CAD Challenges for Leading-Edge Multimedia Designs	Routing	The Test Bin	**PANEL:** Variation-Aware Analysis: Savior of the Nanometer Era?	Low Power and Ultra-Low Voltage Design

LUNCH 12:00 pm - 2:00 pm

	Session 28	Session 29	Session 30	Session 31	Session 32	Session 33
2:00 to 4:00	High-Level Exploration and Optimization	**PANEL:** Design Challenges for Next-Generation Multimedia, Game, and Entertainment Platforms	CAD for FPGAs	Secure Systems	Logic Synthesis I	Low Power, Thermal Aware Architectures

BREAK 4:00 pm - 4:30 pm

	Session 34	Session 35	Session 36	Session 37	Session 38	Session 39
4:30 to 6:30	Low Power System Level Design	Power-Constrained Design for Multimedia	Electrical and Thermal Issues in FPGAs	**SPECIAL SESSION:** Beyond Low Power Design: Environmental Energy Harvesting	Communication Driven Synthesis	Parallelism and Memory Optimizations

Booth #2228

DAC Pavilion

- Student Design Contest Award Presentations — 10:00 am - 10:45 am
- The Xbox 360 Uncloaked: Doing What it Takes to get Chips into High-Volume Consumer Electronics — 11:15 am - 12:00 pm
- AMD/DreamWorks - Fueling Technology Innovation — 1:00 pm - 2:00 pm
- ESL: Software Engineers are from Pluto and Hardware Engineers are from Mercury: Can ESL bridge the gap? — 2:15 pm - 3:15 pm
- The Accidental Pirate — 4:00 pm - 4:45 pm

Wednesday Night Party • 7:30 pm - 10:00 pm • AT&T Ballpark

- indicates special interest to designers Presenters will be available in Rm: 310 for additional 20-minute question-and-answer periods after the session.

Session Tracks: Business | System Level & Embedded | MEGa | Low Power and Thermal | Analog and Circuit | Interconnect, Reliability and DFM | Verification and Test | Synthesis and FPGA | Physical Design | Beyond the Die | New and Emerging Technologies

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Thursday, July 27 — Exhibit Hours 9:00 am - 1:00 pm

	Rm: 306/308	Rm: 307	Rm: 305	Rm: 304	Rm: 303	Rm: 301
	Session 40	Session 41	Session 42	Session 43	Session 44	Session 45
8:30 to 10:00	**PANEL:** Tomorrow's Analog: Just Dead or Just Different?	Nanotubes and Nanowires	Simulation Assisted Formal Verification	Yield Analysis and Improvement	Approaches to Soft Error Mitigation	Design/Technology Interaction
	BREAK 10:00 am - 10:30 am					
	Session 46	Session 47	Session 48	Session 49	Session 50	Session 51
10:30 to 12:00	**PANEL:** Building a Verification Test Plan: Trading Brute Force for Finesse	**SPECIAL SESSION:** More Moore's Law and More than Moore's Law	Formal Specification, Verification Planning, and Test Generation	Analysis and Optimization Issues in NoC Design	**SPECIAL SESSION:** Key Technologies for Beyond the Die	Analog Design and Design Assistance
	12:45 pm - 1:45 pm • Gateway Ballroom • Keynote – *The Challenges of Convergence* *Alessandro Cremonesi* - Strategy and System Technology Group Vice-President & Advanced System Technology General Manager, STMicroelectronics					**Best Paper Award Presentations**
	Session 52	Session 53	Session 54	Session 55	Session 56	Session 57
2:00 to 4:00	High-Performance Simulation of Transaction Level and Dataflow Models	Nano- and Bio-Chip Design	Logic and Sequential Synthesis	Low Power Circuit Design	Beyond-the-Die Circuit and System Integration	New Ideas in Analog/RF Modeling and Simulation
	BREAK 4:00 pm - 4:30 pm					
	Session 58	Session 59	Session 60	Session 61	Session 62	
4:30 to 6:00	Advanced Methods for Interconnect Extraction, Clocks and Reliability	**PANEL:** DFM: Where's the Proof of Value?	Bounded Model Checking and Equivalence Verification	Test Response Compaction and ATPG	Placement	

Booth #2228
DAC Pavilion

Developing Consumer SoCs - IP and Automation or Sticks and Duct Tape
10:00 am - 10:45 am

Wireless USB - The Next Ubiquitous Connectivity Standard?
11:00 am - 11:45 am

Troubleshooting the Multi-Processor SoC Design Flow
12:00 pm - 12:45 pm

- indicates special interest to designers Presenters will be available in Rm: 310 for additional 20-minute question-and-answer periods after the session.

Session Tracks: Business · System Level & Embedded · MEGa · Low Power and Thermal · Analog and Circuit · Interconnect, Reliability and DFM · Verification and Test · Synthesis and FPGA · Physical Design · Beyond the Die · New and Emerging Technologies

Hands-on Tutorials & Full-Day Tutorials

	Monday, July 24		Tuesday, July 25	Wednesday, July 26	Thursday, July 27	Friday, July 28
		Full-Day Tutorials:				*Full-Day Tutorials:*
9:00 to 12:00	Analysis and Optimization of Low Power Designs *Apache Design Solutions, Inc.*	1) ESL Design Methodology Using SystemC 2) Practical Aspects of Coping with Variability: An Electrical View	———	Low Power by Using a Clockless Design Style *Handshake Solutions*	Low Power Management Design Using Multi-Voltage Design and Verification Tools *ArchPro Design Automation, Inc.*	3) Real DFM Solutions, Tools Methodologies and Successes 4) Surviving and Thriving in the World of Chip and Package Co-Design 5) SystemVerilog: Language Tutorial and Industrial Verification Experience
			BREAK 12:00 pm - 2:00 pm			
2:00 to 5:00	Using Virtual System Prototypes to Optimize Architectures for Low Power and Other Key Attributes *VaST Systems Tech., StarCore LLC, Greenhills Software*		Low Power Design Using Predictive Development - Atrenta Solution in Action on a Next-Generation 3G Cell Phone Chip *Atrenta, Inc., Freescale*	Reduce Leakage Power and Increase Battery Life by Implementing an Ideal Vt Selection Strategy *Prolific, Inc., ARM*	Low Power Design - Designer's Perspective *Virage Logic Corp., Cadence Design Systems, Inc., Sandbridge Technologies*	6) Tools for Hybrid Embedded Systems: Modeling, Verification, and Design 7) From Basic to Advanced Techniques for Silicon Debug and Diagnosis

Keynote, Tuesday, July 25 • 8:30 am - 10:15 am • Gateway Ballroom

Structuring Process and Design for Future Mobile Communication Devices

Hans Stork

Senior Vice President and Chief Technology Officer, Texas Instruments Inc.

The density and speed of sub-50nm CMOS technology enables the design of multi-functional SoCs for highly integrated, mobile communication devices. At the same time, process variations, power issues, and complexity of scope are challenging even the most advanced simulation capabilities. The growing design complexity is addressed by rapidly improving modeling of systematic manufacturing variations and design sensitivities. Physical design is becoming more structured to allow for process optimized design rules and efficient automation. While challenges remain in the scaling and optimization of analog and I/O functions, highly integrated, mobile communication devices are a major driving force for continued economies of scaling.

Keynote, Thursday, July 27 • 12:45 pm - 1:45 pm • Gateway Ballroom

The Challenges of Convergence

Alessandro Cremonesi

Strategy and System Technology Group Vice-President & Advanced System Technology General Manager, STMicroelectronics

In this talk, the trends of the major application fields in the era of convergence are analyzed. The emphasis is on the challenges the semiconductor industry will have to face to address these new trends and opportunities.

Applications are becoming increasingly complex and the need to guarantee the coexistence of a wider range of applications on a single chip makes system-level integration a real challenge. Most of the applications will run on platforms designed for portable products, pushing the industry to emphasize power budgets for new designs, both at silicon and at system level. From the platform architecture perspective, multiprocessing is already a reality, and the industry will have to find new paradigms to handle the increased complexity at the system, embedded software, and at the silicon implementation levels.

The talk concludes with future perspectives from the viewpoint of ST's advanced research organization.

Management Day – Tuesday, July 25

DAC's Management Day is where the technology and the business of IC and system design intersect. This full day of sessions is designed for managers and executives of semiconductor, communications and consumer electronics companies. Participants meet, interact with, and learn from peers who are facing the issues of how to make the right business and technology decisions in the dynamic world of electronic design. The Management Day $75 registration fee includes the 11th Annual EDA Business Forum luncheon, and the wrap-up cocktail party. Sessions include:

General Session Keynote Address - *Structuring Process and Design for Future Mobile Communication Devices*
Hans Stork, Senior Vice President and Chief Technology Officer, Texas Instruments Inc.

Session 1: PANEL: *How Will the Fabless Model Survive?*

Management Day Session 100: *Decision-Making for Complex SoCs in Consumer Electronic Products*

Session Chair: Ron Wilson, EDN

Qualcomm Lesson Learned at the 65nm Node - Charlie Matar, Riko Radojcic, Qualcomm CDMA Technologies

Low Power Challenges in Wireless ICs - Rene Delgado, Freescale

Consumer Electronics Development Tradeoff's in the High-Tech Startup - Dwan Fitzgerald, JamTech

Architecture Planning Criteria for a System-in-a-Package Portable Multimedia Platform - Mario Manninger, AMS

Management Day Session 150: *Tradeoffs and Choices for Emerging SoCs in High-End Applications*

Session Chair: Nic Mokhoff, EE Times

Assessing Process Nodes and IP for SoC Development - Ken Wagner, PMC Sierra

Open-IP: How Your Selection of IP Drives Your ASIC Success - Rajesh Shah, Open Silicon

Yield, Manufacturability and Test: The Criteria to Judge the Right Design Investment - Rajesh Galivanche, Intel Corp.

MEGa Sessions: Multimedia, Entertainment, and Games

For 2006, the 43rd DAC is presenting MEGa Sessions: the design challenges and design technology requirements for creating advanced multimedia, entertainment, and game (MEGa) products. The MEGa theme is woven into both keynote addresses and is a full-track of sessions on July 26th. The presentations include a special session highlighting the best papers from ISSCC in the multimedia area, with presentations from Renasas/DoCoMo, MediaTek, National Chiao-Tung University, and Samsung, and continues with two complementary events: an invited session on CAD challenges for leading-edge multimedia designs, followed by a panel on design challenges for next generation multimedia, entertainment, and game platforms. These two sessions include experts from STMicroelectronics, IBM, nVidia, PixelWorks, Qualcomm, and Intel. The sessions conclude with four papers on power-constrained design for multimedia.

Complementing the MEGa sessions will be Pavilion Panels, taking place throughout the week on the exhibit floor. These include presentations on Inside the iPod, technology requirements for 3-D graphics in feature films, and a discussion on the Xbox 360 and getting chips into high-volume products.

All full-conference attendees are invited to attend the MEGa technical sessions, and all registrants are invited to attend the DAC Pavilion sessions in Booth 2228 on the exhibit floor.

DAC Pavilion on the Exhibit Floor Booth #2228

DAC has an exciting line-up of panels and presentations in the DAC Pavilion on the exhibit floor. The DAC Pavilion sessions are open to all attendees and feature provocative technical, business, and strategy discussions.

DAC PAVILION	DAY	TIME
Dataquest at DAC with Gary Smith	Mon., July 24	9:30 am - 10:30 am
What Will it Take to Break the $4B Revenue Cap?	Mon., July 24	11:00 am - 12:00 pm
Ask the CTO	Mon., July 24	1:00 pm - 2:00 pm
Inside the iPod	Mon., July 24	3:00 pm - 4:00 pm
Mass Book Signing	Mon., July 24	4:15 pm - 5:15 pm
The Do's and Don'ts of Verification	Tues., July 25	10:15 am - 11:00 am
Design Team Collaboration: Tools Challenge or Organization Responsibility	Tues., July 25	11:30 am - 12:15 pm
Exporting in the Hallway	Tues., July 25	1:00 pm - 1:45 pm
Shattering the Glass Ceiling: A Decade of Growth for Women	Tues., July 25	2:00 pm - 2:45 pm
The Fabless Model: Is DFM Our Salvation or Demise?	Tues., July 25	4:00 pm - 4:45 pm

DAC PAVILION	DAY	TIME
Student Design Contest Award Presentations	Wed., July 26	10:00 am - 10:45 am
The Xbox 360 Uncloaked: Doing What it Takes to get Chips into High-Volume Consumer Electronics	Wed., July 26	11:15 am - 12:00 pm
AMD/DreamWorks - Fueling Technology Innovation	Wed., July 26	1:00 pm - 2:00 pm
ESL: Software Engineers are from Pluto and Hardware Engineers are from Mercury: Can ESL Bridge the Gap	Wed., July 26	2:15 pm - 3:15 pm
The Accidental Pirate	Wed., July 26	4:00 pm - 4:45 pm
Developing Consumer SoCs - IP and Automation or Sticks and Duct Tape?	Thur., July 27	10:00 am - 10:45 am
Wireless USB - The Next Ubiquitous Connectivity Standard?	Thur., July 27	11:00 am - 11:45 am
Troubleshooting the Multi-Processor SoC Design Flow	Thur., July 27	12:00 pm - 12:45 pm

43rd DAC Workshops

UML for SoC Design
Sunday, July 23, 9:00 am - 6:00 pm $100 (member), $150 (non-member)

Introduction to Chips and EDA
Monday, July 24, 10:00 am - 12:00 pm $10

Second Integrated Design System Workshop
Monday, July 24, 12:00 pm - 5:00 pm $50 (member), $75 (non-member)

Workshop for Women in Design Automation - ***Working the 80/20 Rule for Success - Focusing in on What Matters***
Monday, July 24, 9:00 am - 12:45 pm $50 (member), $75 (non-member)

Exhibition

The 43rd DAC Exhibition is located in the North (Booths 3000-4367) and in the South (Booths 101-2323) Halls of The Moscone Center

The DAC Exhibit floor is bursting with over 240 vendors offering products for all phases of the electronic design process including EDA tools, IP cores, embedded system and system-level tools, silicon vendors, and a host of new design-for-manufacturing companies. The DAC show floor features its unique exhibit booth and private suite combination, which gives you the freedom to deeply explore the products on the show floor and find a solution that is right for your design. Visit the DAC exhibition and find out how you can improve performance and shorten the time-to-market on your next product.

Attend Free Monday, July 24 , 2006 Register today on-line. For more information call 800-321-4573 or email register@dac.com.

Exhibit Hours

Monday-Wednesday, July 24-26	**9:00 am - 6:00 pm**
Thursday, July 27	**9:00 am - 1:00 pm**

Exhibiting Companies (as of May 8, 2006)

Accelicon Technologies, Inc.
ACE Associated Compiler Experts bv
Advanced Circuit Engineers, LLC
Advantest Technology Solutions Corp.
Agilent Technologies
Aldec, Inc.
Algotronix Ltd.
Altos Design Automation
Analog Bits Inc.
Anasift Technology, Inc.
Anchor Semiconductor, Inc.
Ansoft Corp.
Apache Design Solutions, Inc.
Applied Simulation Technology
Applied Wave Research, Inc.
Appro International, Inc.
Aprio Technologies, Inc.
ArchPro Design Automation Inc.
ARM
Arteris
Artwork Conversion Software, Inc.
asicNorth, Inc.
ASSET InterTech, Inc.
Athena Design Systems
Atrenta Inc.
austriamicrosystems USA, Inc.
Averant, Inc.
Avery Design Systems, Inc.
Axiom Design Automation
Azuro, Inc.
Barth Electronics, Inc.
Beach Solutions
Berkeley Design Automation, Inc.
Blaze DFM, Inc.
Blue Pearl Software
Bluespec, Inc.
Brion Technologies
BullDAST s.r.l.
Cadence Design Systems, Inc.
Calypto Design Systems, Inc.
Cambridge Consultants Ltd.
Carbon Design Systems, Inc.
CAST, Inc.
CebaTech, Inc.
Celoxica
Certess Inc.
Certicom Corp.
ChipEDA
Chip Estimate Corporation
ChipVision Design Systems AG
Clear Shape Technologies, Inc.
ClioSoft, Inc.
CMP
CoFluent Design
Cologne Chip AG
CommandCAD, Inc.
Concept Engineering GmbH
Coupling Wave Solutions
CoWare, Inc.
CRC Press - Taylor & Francis Group LLC
CriticalBlue
DAC Pavilion
DAFCA, Inc.
Dataram
DATE '07
DeFacTo Technologies
Denali Software, Inc.
Design and Reuse
Dini Group La Jolla, Inc. (The)
Dolphin Integration
Doulos
Dynalith Systems Co., Ltd.
EDA Cafe-IB Systems
EDA Tech Forum Journal
EDXACT
eInfochips Inc.
Elsevier
EMA Design Automation, Inc.
Emerging Memory Technologies Inc.
Entasys Design, Inc.
Europractice
EVE
Extension Media / Chip Design Magazine
Extreme DA
Fenix Design Automation B.V.
Fintronic USA, Inc.
FishTail Design Automation
Flomerics, Inc.
Forte Design Systems
Fortelink Inc.
FTL Systems, Inc.
Gaisler Research AB
GDA Technologies, Inc.
Genesys Testware, Inc.
Gidel Ltd.
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