CALL FOR PAPERS

43rd DESIGN AUTOMATION CONFERENCE®

FOR INFORMATION CALL: 1-303-530-4333

Moscone Center, San Francisco, CA · July 24-28, 2006

DAC is the premier conference devoted to Design Automation (DA) and the application of DA tools in designing electronic systems. Four types of submissions are invited: regular papers, special topic sessions, panels, and tutorials. Submissions must be made electronically at www.dac.com. Panel and Tutorial suggestions and Special Session submissions are due **NO later than 5:00 pm MST, November 2, 2005**; Regular Papers are due **NO later than 5:00 pm MST, December 19, 2005.**

TOPICS OF INTEREST

DAC 2006 is seeking papers that deal with design tools, design methods and case studies, and embedded design in a number of categories described below.

Design Tools papers describe contributions to the research and development of design tools and their supporting algorithms.

Design Methods and case studies papers describe innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art design projects.

Embedded Systems are characterized by mixed hardware and software components with limited resources. Increases in software content introduce new system design issues. Embedded design papers describe tools, methods, and case studies for applications with specific embedded system content.

Design papers describe the use of design tools and methods from the perspective of a specific design project. They include a brief description of the design and discussion of: methodology, flow, innovative use of tools, the limits of current tools, and what new tool capabilities are required for future designs.

Submitters no longer need to specify a tools, methods, or embedded systems track, but only specify a category from the 18 listed below.

Categories:

1. Circuit Simulation and Timing Analysis
- Electrical-level circuit and timing simulation
- Static timing analysis and timing verification
- Electrothermal simulation methods

2. Design-for-Manufacturability
- Design for yield, cost issues, and impacts of DFM
- Process technology development, extraction, measurement, and modeling
- Statistical performance analysis and optimization
- Reticle enhancement, lithography-related design optimizations

3. Power Analysis and Low-Power Design
- Analysis and estimation of power
- Embedded low-power approaches: partitioning, scheduling, and resource management
- Device, circuit, and system techniques for low-power design
- Impacts on thermal management of low-power design techniques

4. Testing
- Digital, system, memory, analog/mixed-signal, and RF test
- ATPG, fault modeling, DFT and BIST, test debugging
- Scan-based testing, delay testing, on-line testing
- Cost issues and impacts of testability

5. Verification
- Functional, transaction-level, RTL and gate-level modeling and verification of hardware design
- Dynamic simulation, equivalence checking, formal (and semi-formal) verification model and property checking
- Emulation and hardware simulators or accelerator engines
- Modeling languages and related formalisms, verification plan development and implementation
- Assertion-based verification, coverage-analysis, constrained-random testbench generation

6. IC Physical Design
- Physical floorplanning, partitioning, placement
- Buffer insertion, routing, interconnect planning
- Module generation, cell sizing, and library optimization
- Physical verification

7. Logic Synthesis
- Combinational, sequential, and asynchronous logic synthesis, both technology-independent and dependent
- Library mapping, cell-based design and optimization
- Transistor sizing
- Interactions between logic design and layout or physical synthesis

8. High-Level Synthesis
- High-level, behavioral, algorithmic, and architectural synthesis, "C" to gates tools and methods
- HW-SW interface synthesis, communication and network synthesis
- Synthesis of digital circuits above the RTL level
- Resource scheduling, allocation, and synthesis

9. Interconnect
- Interconnect modeling and extraction for current and advanced mainstream IC processes
- Model-order reduction methods for linear systems
- Substrate modeling with interconnect parasitic extraction
- High-frequency and electromagnetic simulation of circuits

10. Signal Integrity and Design Reliability
- Signal integrity, thermal analysis, and reliability modeling and analysis
- Timing, clocking, and power distribution, especially novel techniques
- Power grid robustness analysis and optimization
- Capacitive and inductive crosstalk noise
- Soft-errors and single-event upsets (SEUs)

11. Analog/Mixed-Signal and RF
- Analog, mixed-signal, and RF design
- Automated synthesis and macromodeling
- Simulation and optimization

12. FPGA Design Tools and Applications
- Rapid prototyping
- Logical synthesis and physical design techniques for FPGAs
- Configurable and reconfigurable computing

13. Embedded HW Design and Applications
- Case studies of embedded system design
- Flows and methods for specific applications and design domains

14. Embedded SW Tools and Design
- Retargetable compilation
- Memory/cache optimization
- Real-time single- and multi-processor scheduling, linking, loading
- Real-time operating systems

15. System-Level Design and Co-Design
- System specification, modeling, simulation, and performance analysis
- Scheduling, HW-SW partitioning
- IP and platform-based design, IP protection
- Communications-based design
- System-on-Chip (SoC), Network-on-Chip (NoC), Multi-processor SoC (MPSOC)
- Application-specific processor design tools

16. New, Emerging, or Specialized Design Technologies Including, But Not Restricted to,
- MEMS, sensors, actuators, imaging devices
- Nano-technologies, nano-wires, nano-tubes
- Quantum computing
- Biologically based systems
- New transistor structures and devices, new or radical process technologies

17. Beyond Die-Integration and Packaging
- Chip-package-board codesign
- System-in-Package
- 3D design, stacked devices
- Analysis and optimization (signal integrity, physical layout, simulation) beyond the die

18. Special Theme Day—ENTERTAINMENT, GAMES, and MULTIMEDIA
- Design issues pertaining to mobile devices, music, video, broadcast, video on demand, and other multimedia/consumer entertainment devices
- Intensive multimedia processing as part of entertainment computing and specialized entertainment engine design
- Design and implementation of game playing, video, and audio engines
- Cross-platform entertainment and game software design and design implications
- System-level design approaches for games and multimedia entertainment devices

ALL SUBMISSIONS MUST BE MADE ELECTRONICALLY AT THE DAC WEB SITE: WWW.DAC.COM

REGULAR PAPERS DUE BEFORE 5 pm MST, Dec. 19, 2005

Regular paper submissions must (1) be in PDF format only, (2) contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission, (3) be no more than 6 pages (including the abstract, figures, tables, and references), double columned, 9pt or 10pt font, and (4) **MUST NOT** include name(s) or affiliation(s) of the author(s) anywhere on the manuscript, abstract, or bibliographic citations. Format templates are available on the DAC web site for your convenience, but are not required. Submissions not adhering to these rules, or those previously published or simultaneously submitted to another conference, will be rejected. Additional submission guidelines are available on the DAC website (after Sept. 1, 2005). All regular papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage. Authors of accepted papers must sign a copyright release form for their paper. Notice of acceptance will be sent via email by April 17, 2006.

SPECIAL SESSIONS DUE BEFORE 5 pm MST, Nov. 2, 2005

Special session submissions must include descriptions of suggested papers and speakers, and the importance of the special session to the DAC audience. DAC reserves the right to restructure all special sessions.

PANELS and TUTORIALS DUE BEFORE 5 pm MST, Nov. 2, 2005

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panels and tutorials.

STUDENT DESIGN CONTEST DUE BEFORE 5 pm MST, Dec. 8, 2005

Students are invited to submit descriptions of original electronic designs, either circuit level or system level. Student Design Contest paper submissions must (1) be in PDF format only, (2) contain the title of the project, (3) contain an abstract of approximately 60 words, (4) a complete description of the project, and (5) be no more than 6 pages (including the abstract, maximum of 10 figures/tables and references), double columned, 9pt or 10pt font. The submission should clarify the originality, distinguishing features, and measured performance of the design. Two categories of designs - operational and conceptual - are eligible for awards. For operational designs, proof-of-implementation is required, while for conceptual designs, complete simulation is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2004. Submitted designs should not have received awards in other contests. Selected designs will be presented at the conference (and at ISSCC in February 2006). Additional submission guidelines are available on the DAC web site.

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