43rd DAC Best Paper Awards

Technical Program Co-Chair: Grant E.Martin - *Tenscilica, Inc., Santa Clara, CA*
Technical Program Co-Chair: Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

Front-End Design Award

Session 14.2 ***SAT Sweeping Using Local Observability Don't-Cares***
Qi Zhu, Nathan B. Kitchen - *Univ. of California, Berkeley, CA*
Andreas Kuehlmann - *Cadence Berkeley Labs, Berkeley, CA*
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

Back-End Design Award

Session 13.1 ***Power Grid Physics and Implications for CAD***
Eli Chiprout - *Intel Corp., Hillsboro, OR*
Sanjay Pant - *Univ. of Michigan, Ann Arbor, MI*

Best Paper Candidates:

Session 3.1 ***A CPPLL Hierarchical Optimization Methodology Considering Jitter, Power and Locking Time***
Jun Zou, Daniel Mueller, Helmut Graeb, Ulf Schlichtmann

Session 8.1 ***Charge Recycling in MTCMOS Circuits: Concept and Analysis***
Ehsan Pakbaznia, Farzan Fallah, Massoud Pedram

Session 9.1 ***A Multiprocessor System-on-Chip for Real-Time Biomedical Monitoring and Analysis: Architectural Design Space Exploration***
Iyad Alkhatib, Francesco Polett, Davide Bertozzi, Luca Benini

Session 13.2 ***Fast Analysis of Structured Power Grid by Triangularization Based Structure Preserving Model Order Reduction***
Hao Yu, Yiyu Shi, Lei He

Session 19.2 ***Timing-Based Delay Test for Screening Small Delay Defects***
Nisar Ahmed, Mohammad Tehranipoor, Vinay Jayaram

Session 24.1 ***BoxRouter: A New Global Router Based on Box Expansion and Progressive ILP***
Minsik Cho, David Z. Pan

Session 28.2 ***Register Binding for Clock Period Minimization***
Shih Hsu Huang, Chun Hua Cheng, Wei Chieh Yu, YowTyng Nieh

Session 30.1 ***Architecture-Aware FPGA Placement using Metric Embedding***
Padmini Gopalakrishnan, Xin Li, Lawrence T. Pileggi

Session 31.1 ***VIRTUS: A New Processor Virtualization Architecture forSecurity-Oriented Next-generation Mobile Terminals***
Hiroaki Inoue, Akihisa Ikeno, Masaki Kondo, Junji Sakai, Masato Edahiro

Session 39.1 ***A Constraint Network Based Solution to Code Parallelization***
Ozcan Ozturk, Guilin Chen, Mahmut Kandemir