Awards

Marie R. Pistilli Women in EDA Achievement Award

• **Ellen J. Yoffa** - *Director of Next Generation Web, IBM T.J. Watson Research Center, Yorktown Heights, NY*

For her significant contributions in helping women advance in the field of EDA technology.

The P.O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering

The objective of the P.O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under-represented groups (women, African American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship and SIGDA continues to administer the program for DAC. DAC normally funds two or more $4000 scholarships, renewable up to five years, to graduating high school seniors.

The 2006 winners are:

Katlyn DeLuca - attending University of Massachusetts, Lowell, MA

Eletha Flores - attending Massachusetts Institute of Technology, Cambridge, MA

For more information about the P.O. Pistilli scholarship, contact Dr. Cherrice Traver, ECE Dept., Union College, Schenectady, NY 12308. email: traverc@union.edu

DAC/ISSCC Student Design Contest Winners

Operational Chip Design Category: 1st Place (Best Overall)

A 10.6mW/0.8pJ Power-Scalable 1 GS/s 4b ADC in 0.18um CMOS with 5.8GHz ERBW

Pierluigi Nuzzo, Fernando De Bernardinis, Pierangelo Terreni - *University of Pisa*
Bert Gyselinckx, Liesbet Van der Perre, Geert Van der Plas - *IMEC*

Design Automation Conference Graduate Scholarships

Each year the Design Automation Conference sponsors several $24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in "design and test automation of electronic and computer systems". Each scholarship is awarded directly to a university for the Faculty Investigator to expend in direct support of one or more DA graduate students.

The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are: the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Prof. Jennifer L. Dworak - *Division of Engineering–Electrical Sciences and Computer Engineering, Brown University, Providence, RI*

Student: **Elif Alpaslan**

A Statistical Coverage Metric and Stimulus Generation Approach for Design Verification Based upon Structural Analysis of the Design and Stimulus

Prof. Daniel Kroening - *Computer Systems Institute, Swiss Institute of Technology, Zurich, Switzerland*

Student: **Vijay D'silva**

Automatic Detection of Multi-Cycle Paths in Large Circuits

Information on next year's DAC scholarship award program will be available on the DAC web site: http://www.dac.com.

Awards

The ACM Transactions on Design Automation of Electronic Systems (TODAES) 2006 Best Paper Award

Zero Cost Indexing for Improved Processor Cache Performance • Volume 11, Issue 1, January 2006, Pages 3-25

Tony Givargis - *University of California, Irvine, CA*

The Association for Computing Machinery/Special Interest Group on Design Automation (ACM/SIGDA) Distinguished Service Award

• **Robert A. Walker** - *Kent State University, Kent, OH*

For dedicated service as SIGDA Chair (2001 - 2005), and over a decade of service to SIGDA, DAC, and the EDA profession

2005 Phil Kaufman Award for Distinguished Contributions to EDA

• **Phil Moorby** - *Chief Scientist, Synopsys, Inc.*

Phil Moorby is the recipient of the prestigious EDA Consortium 2005 Phil Kaufman Award for industry contributions as the inventor of the Verilog hardware design language (HDL) which has become, and today remains, one of the world's most popular electronic design languages.

IEEE Circuits and Systems Society 2006 Education Award

• **Wayne Wolf** - *Princeton University, Princeton, NJ*

For outstanding education and leadership in VLSI systems and embedded computing

IEEE Circuits and Systems Society 2006 Industrial Pioneer Award

• **John A Darringer** - *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*

For the development of practical techniques and algorithms for automated logic synthesis, for their realization as usable tools, and for their successful application to high performance computing products

IEEE Circuits and Systems Society 2006 Donald O. Pederson Award

Embedded Deterministic Test • IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 23, no. 5, pp. 776-792, May 2004

Janusz Rajski – *Mentor Graphics Corp., Wilsonville, OR*
Jerzy Tyszer – *Poznan University of Technology, Poznan, Poland*
Mark Kassab – *Mentor Graphics Corp., Wilsonville, OR*
Nilanjan Mukherjee – *Mentor Graphics Corp., Wilsonville, OR*

IEEE Circuits and Systems Society 2006 CSVT Transactions Best Paper Award

Complexity Scalable Motion Compensated Wavelet Video Encoding • IEEE Transactions on Circuits and Systems for Video Technology, vol. 15, no. 8, pp. 982-993, August 2005

Deepak Srinivas Turaga – *Philips Research USA, Briarcliff Manor, NY*
Mihaela van der Schaar-Mitrea – *Philips Research USA, Briarcliff Manor, NY*
Beatrice Pesquet-Popescu – *Telecom Paris, Paris Cedex 13, France*

IEEE Circuits and Systems Society 2006 VLSI Transactions Best Paper Award

A Process-Tolerant Cache Architecture for Improved Yield in Nanoscale Technologies • IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, no. 1, pp. 27-38, January 2005

Amit Agarwal – *Intel Corp., Hillsboro, OR*
Bipul C. Paul – *Purdue University, West Lafayette, IN*
Hamid Mahmoodi – *San Francisco State University, San Francisco, CA*
Animesh Datta – *Purdue University, West Lafayette, IN*
Kaushik Roy – *Purdue University, West Lafayette, IN*

Awards

2006 IEEE Fellows

• **Charles Alpert** - *IBM Corp., Austin, TX*
For contributions to physical design automation of very large scale integrated (VLSI) circuits

• **Wolfgang Kunz** - *University of Kaiserlautern, Kaiserlautern, Germany*
For contributions to hardware verification, very large scale integrated (VLSI) circuit testing and logic synthesis

• **Resve Saleh** - *University of British Columbia, Vancouver, BC, Canada*
For contributions to mixed-signal integrated circuit simulation and design verification

• **Chuan-Jin Richard Shi** - *University of Washington, Seattle, WA*
For contributions to computer-aided design of mixed-signal integrated circuits

• **Martin Wong** - *University of Illinois at Urbana-Champaign, Urbana, IL*
For contributions to algorithmic aspects of computer-aided design (CAD) of very large scale integrated (VLSI) circuits and systems

Best Paper Winners

Front-End Design Winner

14.2 SAT Sweeping with Local Observability Don't-Cares
Qi Zhu, Nathan B. Kitchen - *Univ. of California, Berkeley, CA*
Andreas Kuehlmann - *Cadence Berkeley Labs, Berkeley, CA*
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

Back-End Design Winner

13.1 Power Grid Physics and Implications for CAD
Eli Chiprout - *Intel Corp., Hillsboro, OR*
Sanjay Pant - *Univ. of Michigan, Ann Arbor, MI*

Best Paper Candidates

Twelve papers were nominated by the Technical Program Committee as a DAC Best Paper Candidate; six in front-end design and six in back-end design. Final decisions will be made after the papers are presented at the conference. The awards for the best papers, one in front-end design and one in back-end design, will be presented at 12:45 on Thursday, July 27 in the Gateway Ballroom, just before the Keynote Address.

Session 3.1 A CPPLL Hierarchical Optimization Methodology Considering Jitter, Power and Locking Time

Session 8.1 Charge Recycling in MTCMOS Circuits: Concept and Analysis

Session 9.1 A Multiprocessor System-on-Chip for Real-Time Biomedical Monitoringand Analysis: Architectural Design Space Exploration

Session 13.1 Power Grid Physics and Implications for CAD

Session 13.2 Fast Analysis of Structured Power Grid by Triangularization BasedStructure Preserving Model Order Reduction

Session 14.2 SAT Sweeping Using Local Observability Don't-Cares

Session 19.2 Timing-Based Delay Test for Screening Small Delay Defects

Session 24.1 BoxRouter: A New Global Router Based on Box Expansion and Progressive ILP

Session 28.2 Register Binding for Clock Period Minimization

Session 30.1 Architecture-Aware FPGA Placement using Metric Embedding

Session 31.1 VIRTUS: A New Processor Virtualization Architecture forSecurity-Oriented Next-generation Mobile Terminals

Session 39.1 A Constraint Network Based Solution to Code Parallelization

Student Design Contest

DAC/ISSCC Student Design Contest

The Student Design Contest promotes excellence in the design of electronic systems by providing a competition for graduate and undergraduate students at universities and colleges. It is co-organized by ISSCC and DAC. This year we received over 50 submissions in three categories: Conceptual, Operational Chip, and Operational Systems. Operational designs are those which have been implemented and tested. Conceptual designs have not yet been fabricated and tested but must have been thoroughly simulated. Students compete for cash prizes donated by industrial supporters, as well as the DAC conference. winners have been invited to show their work at the University Booth on the show floor. Awards will be given at the DAC Pavilion on Wednesday, July 26, 2006 from 10:00 am - 10:45 am. The ceremony will include brief overview presentations from each winning project team.

DAC/ISSCC 2006 Student Design Contest Winners

Operational Chip Design Category:

1st Place **A 10.6mW/0.8pJ Power-Scalable 1 GS/s 4b ADC in 0.18um CMOS with 5.8GHz ERBW** **(Best Overall)**

Pierluigi Nuzzo, Fernando De Bernardinis, Pierangelo Terreni - *University of Pisa*
Bert Gyselinckx, Liesbet Van der Perre, Geert Van der Plas - *IMEC*

(tie) **2nd Place** **Increasing the Time Dynamic Range of Pulse Measurement Techniques in Digital CMOS**

Mona Safi-Harb, Gordon W. Roberts - *McGill University*

(tie) **2nd Place** **A DSP Enabled Microsystem for Cochlear Implants with Hybrid LC Clocking**

Eric D. Marsman, Robert M. Senger - *University of Michigan*
Richard B. Brown-*University of Utah*

3rd Place **A 160K Gates/4.5KB SRAM H.264 Video Decoder for HDTV Applications**

Chien-Chang Lin, Jia-Wei Chen, Hsiu-Cheng Chang, Chao-Ching Wang, Yi-Huan Ou-Yang, Ming-Chih Tsai, Yao-Chang Yang, Jiun-In Guo, Jinn-Shyan Wang - *National Chung ChengUniversity*

Conceptual Category:

1st Place **ASIC Implementation of LDPC Decoder Accelerating Message-Passing Schedule**

Kazunori Shimizu, Tatsuyuki Ishikawa, Nozomu Togawa, Takeshi Ikenaga, Satoshi Goto - *Waseda University*

Operational System Design Category:

1st Place **Demonstration of Uncoordinated Multiple Access in Optical Communications**

Herwin Chan, Andres I. Vila Cadaso, Juthika Basak, Miguel Griot, Wen-Yen Weng, Richard Wesel, B. Jalali, Eli Yablonovitch- *University of California, Los Angeles*
Ingrid Verbauwhede - *University of California, Los Angeles and K.U. Leuven, Belgium*

2nd Place **Illumimote: A High Performance Light Sensor Module for Wireless Sensor Networks**

Heemin Park, Jonathan Friedman, Mani B. Srivastava, Pablo Gutierrez, Vidyut Samanta, Jeff Burke - *University of California, Los Angeles*

3rd Place **An Ultra Low Power Wireless Micro-Sensor Node**

Denis Daly, Daniel Finchelstein, Nathan Ickes, Naveen Verma, Anantha Chandrakasan - *Massachusetts Institute of Technology*

Honorable Mention **Phase Delay Based Collision Avoidance RADAR for Smart Automobiles**

Babu L. Saincha - *Indian Institute of Information Technology*

Award Contributors: