Awards

Marie R. Pistilli Women in EDA Achievement Award

- **Kathryn Kranen** - *President & CEO, Jasper Design Automation, Inc., Mountain View, CA*

For her significant contributions in helping women advance in the field of EDA technology.

The P.O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering

The objective of the P.O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering and Computer Science from under-represented groups (women, African American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship and SIGDA continues to administer the program for DAC. DAC normally funds two or more $4000 scholarships, renewable up to five years, to graduating high school seniors.

The 2005 winners are:

Elizabeth Hong-An Boi Ha - attending Georgia Institute of Tech., Atlanta, GA

Helen You - attending Massachusetts Institute of Tech., Cambridge, MA

For more information about the P.O. Pistilli scholarship, contact Dr. Cherrice Traver, ECE Dept., Union College, Schenectady, NY 12308. email: traverc@union.edu

Design Automation Conference Graduate Scholarships

Each year the Design Automation Conference sponsors several $24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in "design and test automation of electronic and computer systems". Each scholarship is awarded directly to a university for the Faculty Investigator to expend in direct support of one or more DA graduate students.

The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are: the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

The SPICE Modernization Project

Prof. Elias Kougianos - *Dept.of Engineering Technology, Univ. of North Texas, Denton, TX*

Student: Rahul Allawadhi

Spiral Inductor Synthesis for Mixed-Signal Systems

Prof. Yehia Massoud - *Dept.of Electrical and Computer Engineering and Computer Engineering,Rice Univ., Houston TX*

Student: Arthur Nieuwouldt

Information on next year's DAC scholarship award program will be available on the DAC web site: http://www.dac.com.

Awards

ACM Transaction on Design Automation of Electronic Systems (TODAES) 2005 Best Paper Award

Technology Mapping and Architecture Evaluation for k/m-macrocell-based FPGAs **• Volume 10, No. 1, January 2005, Pages:3 - 23.**

Jason Cong - Univ. of California, Los Angeles, CA
Hui Huang - Sun Microsystems, Santa Clara, CA
Xin Yuan -IBM Corp., Essex Junction VT

The Association for Computing Machinery/Special Interest Group on Design Automation (ACM/SIGDA) presents its Distinguished Service Awards

• **Mary Jane Irwin** - *Penn State Univ., University Park, PA*
For dedicated service as Editor in Chief of ACM Journal, TODAES (1998 - 2004), and many years of service to SIGDA, DAC, and the EDA profession.

2004 Phil Kaufman Award for Distinguished Contributions to EDA

• **Joe Costello** - Chairman and CEO of think3 and former Chairman and CEO of Cadence Design Systems, Inc.
For his business contributions that helped grow the EDA industry. Under his leadership (1987-1997), Cadence became the world's leading supplier of EDA software and services, and one of the top ten largest software suppliers in the world.

IEEE Circuits and Systems Society 2005 VLSI Transactions Best Paper Award

• **Radu Marculescu** - *Carnegie Mellon Univ., Pittsburgh, PA*
• **Girish Varatkar** - *Carnegie Mellon Univ.,Pittsburgh, PA*
For the paper entitled, *On-Chip Traffic Modeling and Synthesis for MPEG-2 Video Applications*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol.12, no. 1, pp. 108-119, January 2004.

IEEE Circuits and Systems Society 2005 Darlington Award

• **Payam Heydari** - *Univ. of California, Irvine, CA*
For the paper entitled, *Analysis of the PLL Jitter Due to Power/Ground and Substrate Noise*, IEEE Transactions on Circuits and Systems I, Regular Papers, vol. 51, no. 12, pp. 2404-2416 December 2004.

IEEE Circuits and Systems Society 2005 Industrial Pioneer Award

• **Yervant Zorian** - *Virage Logic Corp., Freemont, CA*
For his contributions to design for test technology through Built-In Self-Test solutions and design tools that dramatically boosted the quality and reliability of digital systems and the efficiency of design and test engineers.

Awards

IEEE Circuits and Systems Society 2005 Outstanding Young Author Award

• **Chris Hyung-Il Kim** - *Purdue Univ., Lafayette,IN*

For the paper entitled, *Ultra Low-Power DLMS Adaptive Filter for Hearing Aid Applications*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol.11, no. 6, pp. 1058-1067, December 2003 (with H. Soeleman and K. Roy).

IEEE Circuits and Systems Society 2005 Donald O. Pederson Award

• **Subhasish Mitra** - *Intel Corp., Folsom, CA*
• **Kee Sup-Kim** - *Intel Corp.,Sacramento, CA*

For the paper entitled, *X-compact: An Efficient Response Compaction Technique*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 23, no. 3, pp. 421-432 March 2004.

2005 IEEE Fellows

• **Fadi Joseph Kurdahi** - *Univ. of California, Irvine,CA*
For contributions to design automation of digital systems and to reconfigurable computing.

• **David J. Comer** - *Brigham Young Univ., Provo UT*
For leadership in engineering education and publication of electronic circuit design textbooks.

• **Kartikeya Mayaram** - *Oregon State Univ.,Corvallis,OR*
For contributions to coupled device and circuit simulation.

• **Chandu Visweswariah** - *IBM Corp., Yorktown Heights, NY*
For contributions to large scale integrated circuits.

• **Reinaldo Alvarenga Bergamaschi** - *IBM Corp., Yorktown Heights,NY*
For contributions to the development of system design tools and methodologies.

• **Domine Leenaerts** - *Phillips Research, Eindhoven, Netherlands*
For contributions to nonlinear circuit theory and design.

DAC/ISSCC Student Design Contest

The purpose of the Student Design Contest is to promote excellence in the design of electronic systems by providing competition between graduate and undergraduate students at universities and colleges. This year we received over 50 submissions in two categories: "Conceptual" and "Operational". Operational designs are those which have been implemented and tested. Conceptual designs have not yet been fabricated and tested but must have been thoroughly simulated. Students compete for cash prizes donated by a number of industrial supporters, as well as the conference. Prize winners have been invited to show their work at the University Booth on the show floor. Awards will be given at the DAC Pavilion, on Wednesday, June 15, 2005 from 10:00 am - 10:45 am.

DAC/ISSCC 2005 Student Design Contest Winners

Operational Category:

1st Place **A 50MS/s (35mW) to 1kS/s (15uW) Power Scaleable 10b Pipelined ADC with Minimal Bias Current Variation**

Imran Ahmed, David Johns - *Univ. of Toronto, Toronto, ON. Canada*

2nd Place **A 1.3 TOPS H.264/AVC Single-Chip Encoder for HDTV Applications**

Tung-Chien Chen, Yu-Wen Huang, Chen-Han Tsai, To-Wei Chen, Ching-Yeh Chen, Liang-Gee Chen - *National Taiwan Univ., Taipei, Taiwan*

3rd Place **A side-Channel Leakage Free Coprocessor IC in 0.18µm CMOS for Embedded AES-based Cryptographic and Biometric Processing**

Kris Tiri, David Hwang, Alireza Hodjat, Bo-Cheng Lai, Shenglin Yang, Patrick Schaumont, Ingrid Verbauwhede - *Univ. of California,Los Angeles,CA*

Conceptual Category:

1st Place **Design and Implementation of a Fractional-N Frequency Synthesizer for Cellular Systems**

Petrus J. Venter, Saurabh Sinha - *Univ. of Pretoria, Pretoria, South Africa*

2nd Place **A 1-V IEEE 802.11a/b/g-Compliant Receiver IF-to-Baseband Chip in 0.35µm CMOS for Low-Cost Wireless SiP**

Pui-In Mak, Rui P. Martins - *Univ. of Macau, Macao SAR,China*
Seng-Pan U - *Chipidea Microelectronics (Macau) Ltd., Macao SAR,China*

3rd Place **Collision Detection System using an FPGA Implemented on the FPX Platform**

Hasan N. Atay, Burchan Bayazit, John W. Lockwood - *Washington Univ., St.Louis,MO*

Award Contributors:

The 42nd Design Automation Conference • June 13 - 17, 2005 • Anaheim, CA

Best Paper Awards

Technical Program Co-Chair: **Andrew B.Kahng** - *Univ. of California at San Diego, La Jolla, CA*
Technical Program Co-Chair: **Grant E.Martin** - *Tenscilica, Inc., Santa Clara, CA*

Front-End Design and Embedded Systems Award

Paper 24.2 *A New Canonical Form for Fast Boolean Matching in Logic Synthesis and Verification*

Afshin Abdollahi, Massoud Pedram- *Univ. of Southern California, Los Angeles, CA*

Back-End Design Award

Paper 19.1 *An Efficient Algorithm for Statistical Minimization of Total Power under Timing Yield Constraints*

Murari Mani- *Univ. of Texas, Austin, TX*
Anirudh Devgan- *IBM Corp., Austin, TX*
Michael Orshansky- *Univ. of Texas, Austin, TX*

Best Paper Candidates:

8.1 **Locality-Conscious Workload Assignment for Array-Based Computations in MPSOC Architectures**
Feihui Li, Mahmut Kandemir

9.1 **Response Compression with Unlimited Number of Unknowns Using a New LFSR Architecture**
Erik H. Volkerink

10.1 **A Green Function-Based Parasitic Extraction Method for Inhomogeneous Substrate Layers**
Chenggang Xu, Kartikeya Mayaram, Ranjit Gharpurey, Terri Fiez

12.1 **Partitioning-Based Approach to Fast On-Chip Decap Budgeting and Minimization**
Hang Li, Sheldon Tan, Zhenyu Qi

13.1 **Temperature-Aware Resource Allocation and Binding in High-Level Synthesis**
Gokhan Memik, Rajarshi Mukherjee, Seda Ogrenci Memik

15.1 **Approximate VCCs: A New Characterization of Multimedia Workloads for System-level MpSoC Design**
Samarjit Chakraborty, Wei Tsang Ooi, Yanhong Liu

20.1 **Fine-grained Application Source Code Profiling for ASIP Design Gerd Ascheid, Heinrich Meyr, Kingshuk Karuri, Mohammad Al**
Faruque, Rainer Leupers, Stefan Kraemer

23.2 **Advanced Timing Analysis Based on Post-OPC Extraction of Critical Dimensions**
Dennis Sylvester, Jie Yang, Luigi Capodieci

25.2 **Simulation of the Effects of Timing Jitter in Track-and-Hold and Sample-and-Hold Circuits**
Vinita Vasudevan

25.3 **Scalable Trajectory Methods for On-Demand Analog Macromodel Extraction**
Saurabh K. Tiwary

27.2 **FPGA Technology Mapping: A Study of Optimality**
Andrew C. Ling, Deshanand P. Singh, Stephen D. Brown

28.1 **Word Level Predicate Abstraction and Refinement for Verifying RTL Verilog**
Daniel Kroening, Edmund M. Clarke, Himanshu Jain, Natasha Sharygina

34.3 **Floorplan-aware Automated Synthesis of Bus-based Communication Architectures**
Elaheh Bozorgzadeh, Mohamed Ben-Romdhane, Nikil Dutt, Sudeep Pasricha

35.4 **Multilevel Full-Chip Routing for the X-Based Architecture**
Chen-Feng Chang, Sao-Jie Chen, Tsung-Yi Ho, Yao-Wen Chang