Important Information At-a-Glance

Exhibit Hours:

Monday, June 7 .....9:00 AM to 6:00 PM
Tuesday, June 8 .....9:00 AM to 6:00 PM
Wednesday, June 9 .....9:00 AM to 6:00 PM
Thursday, June 10 .....9:00 AM to 1:00 PM

Registration Hours

The registration desk will be located in Lobby D of the San Diego Convention Center and will be open at the following times:

Sunday, June 6 .....8:30 AM to 5:00 PM
Monday, June 7 .....7:00 AM to 6:00 PM
Tuesday, June 8 .....7:00 AM to 6:00 PM
Wednesday, June 9 .....7:00 AM to 6:00 PM
Thursday, June 10 .....7:00 AM to 6:00 PM

Tutorial Registration.....Friday, June 11, 7:00 AM to 6:00 PM
on the second level outside meeting Room 6.

Virtual DAC (www.dac.com)

Virtual DAC offers two powerful on-line tools for attendees to make the most of their time at DAC. The *DAC Floor* is designed to allow attendees to plan which exhibitors they want to visit. The *DAC Planner* is designed for attendees to plan which technical sessions and other important DAC events they want to attend. Together, the two services allow attendees to organize their time at DAC, and can be downloaded to a palm.

DACnet-2004

DACnet stations are located in Lobby E and in the Sails Pavilion on the second level of the San Diego Convention Center.

Co-Located Conferences	The 41st Design Automation Conference Week in Review					
	Sunday, June 6	Monday, June 7	Tuesday, June 8	Wednesday, June 9	Thursday, June 10	Friday, June 11
• IWLS June 2-4 *Temecula Creek Inn, Temecula, CA*	• Workshop	• Free Monday • Full-Day Tutorial • Hands-on Tutorials • Exhibits • Workshops	• Opening Session • Keynote Address • Technical Sessions • Business Day at DAC • Hands-on Tutorials • Exhibits	• Technical Sessions • Hands-on Tutorials • Exhibits • DAC Party	• Keynote Address • Technical Sessions • Hands-on Tutorials • Exhibits • Best Paper Awards	• Full-Day Tutorials

Program Highlights

Technical Program - details on pgs. 14 - 35

This year DAC is celebrating its 41st year with a technical program that includes over 163 papers, panels, tutorials, and keynote presentations covering a wide range of design issues. The program covers sessions in seven topic areas: Business, System Level Design and Verification, Power, Logic Design and Test, Embedded Systems, Nanometer Analysis and Simulation, and Physical Circuit Design.

In each of these areas the sessions will cover aspects of both design methodology and design tools. New this year DAC is also offering the Business Day at DAC on Tuesday, June 8th featuring an entire day of sessions woven into the technical program that provide a deep examination of issues at the intersection of technology and business.

OPENING SESSION & KEYNOTE
Patrick P. Gelsinger
CTO & Sr. Vice President, Intel Corp.
Tuesday, June 8 - 8:30 AM
Ballroom 20ABC

THURSDAY KEYNOTE
Walden C. Rhines
Chairman, EDA Consortium
CEO & Chairman, Mentor Graphics Corp.
Thursday, June 10 - 12:45 PM
Ballroom 20ABC

Hands-on Tutorials - details on pgs. 43 - 46

Hands-on Tutorials are three-hour tutorials presented by exhibitors to demonstrate their solutions to issues in two areas: "Power Minimization" and "Structured ASICs".

Business Day at DAC - details on pg. 6

DAC has dedicated a full day of keynotes, panels and special presentations by experts on business topics that affect technology decisions and directions.

Opening Session Keynote Address
Session 2: CEO Panel: EDA: This is Serious Business
Session 7: Panel: When IC Yield Missed the Target, Who is at Fault?
Session 12: Panel What Happened to ASIC? Go (Recon)figure?
Session 100: Competitive Strategies for the Electronics Industry
Session 150: Business Models in IP, Software Licensing and Services

Tutorials - details on pgs. 36 - 38

Monday, June 7 • 9:00 AM - 5:00 PM

1) Getting Your "Cool ASIC" Up to Speed: Practical Techniques and Tools to Achieve Custom-Like Performance in a Power-Aware Design Flow

Friday, June 11 • 9:00 AM - 5:00 PM

2) Automated Macromodelling Techniques for Design of Complex Analog, Mixed-Signal Integrated Systems
3) Buffering Interconnect: from Basics To Breakthroughs
4) Linux for Real-Time and Embedded Systems
5) Silicon Debug: What Do You Do When Your ASIC Does Not Work as Fast as Expected?
6) SystemVerilog for Verification: The Unification of Design, Testbench and Assertions in a Single Language

Exhibit Highlights

Exhibit Floor

Monday - Wednesday, June 7-9, 9:00am - 6:00pm
Thursday, June 10, 9:00am - 1:00pm
Halls A-G of the San Diego Convention Center

Booth/Suite Format

The Design Automation Conference (DAC) convenes for the 41st time in San Diego, CA with a completely new look. For the first time, DAC is merging the exhibit booths and the demo suites into a single exhibit area. This means more accessible suites for exhibitors and an improved DAC experience for the attendees. With over 220 exhibitors, including over 45 first-time participants, the exhibits will be a dynamic showplace for this year's lineup of EDA, silicon, semi IP, and embedded systems tools.

Children under the age of 14 will NOT be allowed in the exhibit hall.

Exhibit-Only Registration

- Free Monday Exhibit-Only Passes - Attend the exhibition free of charge Monday, June 7.
- $60 Exhibit-Only registration will allow you to attend exhibits Monday through Thursday.

DAC Pavilion

DAC has an exciting lineup of panels and presentations in the DAC Pavilion, booth 3733 on the exhibit floor. The DAC Pavilion sessions are open to all attendees at no charge and feature fourteen provocative technical, business and strategy discussions. See pages 7-9 for details.

New Exhibitors at DAC

DAC has always been the best place to see the industry's newest companies, and this year is no exception. With over 45 new exhibitors, DAC is the place to be to find out what the hot startups are up to. Among the companies participating in DAC for the first time are:

ADVEDA
Analog Bits Inc.
Anchor Semiconductor, Inc.
Appro International
Aprio Technologies, Inc.
Avertec Inc.
Azuro, Inc.
Berkeley Design Automation, Inc.
Blue Pearl Software, Inc.
Bluespec, Inc.
BULLDAST S.R.L.
CapExt Corp.
Carbon Design Systems, Inc.
CATS Co., Ltd.
CiraNova, Inc.
Convergence Promotions
CRC Press - A Member of Taylor & Francis Pub.
CriticalBlue
Dynamic Details Inc.
eTop Design Technology, Inc.
FishTail Design Automation
GeTeDes Technologies SAS
GigaScale IC, Inc.
Handshake Solutions
Hier Design Inc.
i2 Content & Data Services
IC Manage
Inovys Corp.
Lorentz Solution Inc.
LTRIM Technologies
Meiosys, Inc.
Nannor Technologies, Inc.
PLDApplications (PLDA)
Praesagus, Inc.
Quintics
Semantic Designs, Inc.
Sierra Design Automation, Inc.
Silicon & Software Systems
Silicon Dimensions
Simantix Systems Inc.
Socle Technology Corp.
SoftJin Infotech Pvt. Ltd.
Speeding Edge
SpiraTech Ltd.
Stelar Tools Inc.
Synfora, Inc.
Verari Systems, Inc.
Verific Design Automation
ViASIC Inc.

Tuesday Keynote - Gigascale Integration for Teraops Performance–Challenges, Opportunities and New Frontiers

Patrick P. Gelsinger
Chief Technology Officer and Senior Vice President,
Intel Corp.
Tuesday, June 8, 2004, 8:30 AM - 10:00 AM
Room: Ballroom 20ABC

Abstract: VLSI system performance increased by five orders of magnitude in the last three decades, made possible by continued technology scaling, improving transistor performance to increase frequency, increasing integration capacity to realize complex architectures, and reducing energy consumed per logic operation to keep power dissipation within limit. The technology treadmill will continue, providing integration capacity of billions of transistors, enabling unprecedented teraops levels of performance; however, with some adverse effects posing barriers.

Transistor subthreshold as well as gate leakage will impact supply voltage scaling, resulting in excessive power consumption. Therefore, transistor structure will have to change from today's basic bulk transistor to a complex structure of high-k dielectric, single or multiple gates per transistor, and polysilicon or a metal as a gate material. The interconnect performance will continue to get worse. Variations due to process, temperature, and supply voltage will have even more prominent effects, and tighter process control will limit design flexibility once taken for granted. Therefore, performance at any cost will not be an option; future system architectures will have to maximize performance in a given power envelope, and evolve innovative architectures to cope with increasing interconnect parasitics. Variations and tighter process control will have a major impact on the design methodology, making a bold move from today's deterministic design to statistical and probabilistic design.

Future design automation tools must comprehend these paradigm shifts, be ready with design technology that comprehends new transistor structures, adopt statistical design methodology to overcome variations, comprehend tighter process controls, and still provide unprecedented productivity boost with gigascale integration.

Biography: Pat Gelsinger is Senior Vice President and Chief Technology Officer of Intel Corp. Gelsinger joined Intel in 1979, and has more than 20 years of experience in general management and product development positions. Gelsinger leads Intel's Corporate Technology Group, which encompasses many Intel research activities, including leading Intel Labs and Intel Research, and driving industry alignment with these technologies and initiatives. As CTO, he coordinates Intel's longer-term research efforts and helps ensure consistency from Intel's emerging computing, networking and communications products and technologies.

Before his appointment as the company's first CTO, Gelsinger was the Chief Technology Officer of the Intel Architecture Group where he led the design and development of next-generation hardware and software technologies for all Intel Architecture platforms for business and consumer market segments.

Gelsinger has held several senior technical and management positions in the company. He led the Desktop Products Group, where he was responsible for Intel's desktop processors, chipsets and motherboards for consumer and commercial OEM customers. Gelsinger was instrumental in defining and delivering the Intel® ProShare® video conferencing and Internet communications product line. He was general manager of the division responsible for the Pentium® Pro, IntelDX2™ and Intel486™ microprocessor families and a key contributor on the original i386™ and i286 chip design teams. Gelsinger holds six patents and six applications in the areas of VLSI design, computer architecture and communications. He has more than 20 publications in these technical fields.

Gelsinger received an associate's degree from Lincoln Technical Institute in 1979, a bachelor's degree from Santa Clara University in 1983, Magna Cum Laude, and a master's degree from Stanford University in 1985. All degrees are in electrical engineering.

Thursday Keynote - EDA Industry Growth - Are There Enough New Problems to Solve?

Walden C. Rhines
Chairman EDA Consortium,
CEO and Chairman, Mentor Graphics Corp.
Thursday, June 10, 2004, 12:45 PM - 1:45 PM
Room: Ballroom 20ABC

Abstract: Electronic design automation became an industry when diversification of the electronics and semiconductor industries led to economies of scale for the design software industry.

Although the EDA industry gives the appearance of relatively steady growth over its history, in actuality it is driven by rapid growth segments and saturation of successive waves of new design paradigms, e.g. printed circuit board layout, ASIC top-down design, physical design facilitated by silicon foundries, etc.

As each of these design paradigms matured, they became slow growth segments of EDA. Future growth of the EDA industry can come only from solving new design problems. Fortunately, there is an abundance of these. Dr. Rhines will address the problems most likely to be the drivers of future industry growth, as well as some less likely possibilities.

Biography: Walden C. Rhines, 57, is Chairman and Chief Executive Officer of Mentor Graphics Corp., a leader in worldwide electronic design automation with revenue of over $675 million in 2003.

Prior to joining Mentor, Rhines was Executive Vice President in charge of Texas Instruments' Semiconductor Group with responsibility for over $5 billion of revenue and over 30,000 people.

Rhines joined Texas Instruments, Inc. (TI) in 1972 and held a variety of technical and business management positions, primarily in the Semiconductor Group, but also in the Consumer Products Division, Central Research Laboratories and Data Systems Group. From 1985 to 1987, Rhines was President of the Data Systems Group. During his career at TI, Rhines was responsible for development of products including TI's first speech synthesis devices (used in "Speak & Spell") and the TMS 320 family of digital signal processors. He managed TI's microprocessor and application specific integrated circuit (ASIC) businesses from less than $10 million in annual revenue to nearly $2 billion.

He served as chairman of the Semiconductor Technical Advisory Committee of the Department of Commerce, as an executive committee member of the board of directors of the Corporation for Open Systems, as a board member of the Computer and Business Equipment Manufacturers' Association (CBEMA), and as a board member of Sematech. He is board chairman of the Electronic Design Automation Consortium, a board member of the Semiconductor Research Corporation and Lewis and Clark College, and he serves as Chairman of the Engineering Technology Industry Council of the State of Oregon.

Dr. Rhines holds a bachelor of science degree in metallurgical engineering from the University of Michigan, a master of science and Ph.D. in materials science and engineering from Stanford University, a master of business administration from Southern Methodist University and an Honorary Doctor of Technology degree from Nottingham Trent University.

DAC Business Day - Tuesday, June 8

DAC is the premier forum for both technology and business. To further encourage exchange and education on business and technology issues, DAC has dedicated a full day to keynotes, panels and special presentations by experts on business topics that affect technology decisions and directions. Business Day at DAC is open to all DAC Full-Conference and Tuesday-Only registrants and is targeted at executives and managers who are responsible for technology decisions. No additional registration is required.

Business Day Sessions include:

Opening Session Keynote Address - Ballroom 20ABC
8:30 AM - 10:00 AM

Patrick P. Gelsinger, CTO & Senior Vice President, Intel Corp., *Gigascale Integration for Teraops Performance- Challenges, Opportunities, and New Frontiers*

Session 1 CEO Panel - Rm: 6A - 10:30 AM - 12:00 PM

EDA: This is Serious Business - A candid discussion with the CEOs of the three largest EDA companies
Moderated by A. Richard Newton, Dean of Engineering at UC Berkeley.

Session 7 Panel - Rm: 6B - 2:00 PM - 4:00 PM

When IC Yield Missed the Target, Who is at Fault?

Session 12 Panel - Rm: 6B - 4:30 PM - 6:00 PM

What Happened to ASIC? Go (Recon)figure?

Special Business Day Session 100 - 2:00 PM - 4:00 PM

Competitive Strategies for the Electronics Industry

Special Business Day Session 150 - 4:30 PM - 6:00 PM

Business Models in IP, Software Licensing and Services

Business Day Session 100 - Rm: 6F - 2:00 PM - 4:00 PM
Competitive Strategies for the Electronics Industry

Chair: Alan Naumann, CoWare, Inc.
Organizer: Ellen M. Sentovich, Cadence Design Systems, Inc.

Competing in today's economy requires close examination of current business practices and careful strategies for moving into the future. This session will examine three key areas for establishing competitive edge: globalization, patents and intellectual property management, and strategic marketing. Each talk will cover a broad spectrum of approaches, applicable to design, EDA, and IP-based companies. Conclusions will be drawn about which methods will be most successful for moving into the next era of electronics. The final portion of the session is devoted to discussion, debate, and Q&A.

Speakers: Jaswinder Ahuja - Cadence Design Systems, Inc., Noida, India
Paul Lippe - Silicon Image, Sunnyvale, CA
Bernie Rosenthal - Tensilica, Inc., Santa Clara, CA

Business Day Session 150 - Rm: 6F - 4:30 PM - 6:00 PM
Business Models in IP, Software Licensing, and Services

Chair: Lucio Lanza, Lanza Tech. Ventures
Organizer: Ellen M. Sentovich, Cadence Design Systems, Inc.

A variety of business models in design and design automation are being employed today that have a dramatic effect on the success of individual companies and of multiple industries within the domain of electronics. The three talks in this session will study models for managing IP, software licensing, design and EDA services. A variety of approaches, constraints, and case studies will be presented in each case, with conclusions about how to make these models most successful for all parties involved. The final portion of the session is devoted to discussion, debate, and Q&A.

Speakers: Raul Camposano - Synopsys, Inc., Mountain View, CA
Jim Douglas - ReShape, Inc., Mountain View, CA
Aurangzeb Khan - Cadence Design Systems, Inc., San Jose, CA

DAC Pavilion

DAC brings its technical program to the exhibit floor through live panel discussions and presentations in the DAC Pavilion. DAC attendees and exhibitors are invited to visit the DAC Pavilion in Booth 3733 to participate in these engaging technical presentations. Sessions are scheduled daily from Monday, June 7 - Thursday, June 10.

Monday, 9:15 AM - 10:00 AM

EDA Business Forecast

Moderator: Dennis Brophy - *Model Technology, Inc., a Mentor Graphics Co.*
Panelist: Gary Smith - *Gartner Dataquest*
Highlights from the annual Gartner Dataquest EDA and semiconductor industry forecast for those who were not able to attend their Sunday evening presentation.

Monday, 10:15 AM - 11:00 AM

Wall Street Review of EDA: 2004 Update

Moderator: Jessica Kourakos - *Synopsys, Inc.*
Panelists: Richard Valera - *EDA & Semiconductor Analyst - Needham & Company, Inc.*
John Barr - *Buckingham Capital Management, Inc.*
After at least three years of economic stall for systems and semiconductor companies, there are cautiously optimistic whispers of a recovery in 2004. The continued pressure on the EDA industry and its customers helped drive an ongoing trend toward consolidation. Will an economic recovery slow down consolidation and foster an increase in IPOs? Do EDA players need to look to additional markets for growth?

Monday, 11:15 AM - 12:00 PM

EDA Mergers and Acquisitions: Glory or Death?

Moderator: John Barr - *Buckingham Capital Advisors*
Panelists: Venk Shukla - *Magma Design Automation, Inc.*
John Sanguinetti - *Forte Design Systems*
Jim Hogan - *Telos Venture Partners*
A collection of long-time EDA participants and observers who can speak to the topic of mergers and acquisitions from a variety of perspectives: technologist, entrepreneur, and financier.

Monday, 2:00 PM - 2:45 PM

Export Controls In the Age of Globalization

Moderator: Walden C. Rhines - Chairman EDA Consortium/ CEO & Chairman, *Mentor Graphics Corp.*
Panelists: Larry Disenhof - Cadence Design Systems, Inc.
Erik Oliver - Synopsys, Inc.
WAN access to design data or design tools across international boundaries is an export, and corporate officers can be severely fined or jailed for violations of international export regulations. Learn about the recently simplified international EDA export regulation. Find out from EDA export experts how international export regulations affect you and your company, and how piracy issues affect export controls.

Monday, 3:00 PM - 3:45 PM

The Semiconductor IP Business In 2004

Moderator: John Chilton - *Synopsys, Inc.*
Panelists: Mike Kaskowitz - *Mentor Graphics Corp./VSIA*
Jerry Ardizzone - *ARM*
Michael Depeyrot - *Dolphin Integration*
Tim Daniels - *LSI Logic Corp.*

There are a growing number of companies that provide high-quality semiconductor IP, but sometimes customers can't tell how good the IP really is until you "move in". Customers have been clamoring for some method to measure the "quality" of the IP they are considering for use in their designs. Will there ever be a "Good Housekeeping" seal of approval for IP quality or will customers have to continue to rely on their noses to figure out if they are in the penthouse or the outhouse?

Monday, 4:00 PM - 4:45 PM

User Forums or Useless Forums?

Moderator: Naveed Sherwani - *Open Silicon*
Panelists: John Cooley - *ESNUG*
Pallab Chatterjee - *SiliconMap, LLC*
Marco Casale-Rossi - *STMicroelectronics*
Kaushik Banerjee - *Marvell Semiconductor*
Moazzem Hossein - *Fastrack Design, Inc.*
John McGehee - *Voom, Inc.*
Steve Schultz - *Silicon Integration Initiative, Si2, Inc.*

There is a lot of value in designers coming together and sharing their experiences with each other. Oracle, Sun, Apple and many other companies hold their users' group meetings and provide value to new and seasoned users. However, when such user groups are used as marketing media, do the users get the value they hope for? Who should manage, coordinate these user groups?

Tuesday, 2:00 PM - 2:45 PM

Ask the CTOs: Everything You Ever Wanted to Know But Were Afraid to Ask

Moderator: Andrew B. Kahng - *Univ. of California, San Diego*
Panelists: Mike Muller - *ARM*
Raul Camposano - *Synopsys, Inc.*
Ted Vucurevich - *Cadence Design Systems, Inc.*

CTOs from top EDA and IP companies will discuss customers' leading-edge design issues, such as 90 nm, IP verification, the future of ASICs and embedded FPGAs, low power issues, verification solutions, and other challenges as identified in the International Technology Roadmap for Semiconductors (ITRS).

Tuesday, 3:00 PM - 3:45 PM

EDA Software Quality

Moderator: Yehuda Shiran - *Intel Corp.*
Panelists: Erric Solomon - *Synopsys, Inc.*
Mark Noneman - *Cadence Design Systems, Inc.*

When a designer gets a tool that is bug ridden, dead on arrival, or generates different results than a previous version, this usually results in lower productivity for the designer. At best, designers need to switch gears while waiting for the fix, incurring idle and switching costs. The worst case is when there is no work around and the design work is shut down until a fix is shipped. Our panelists will address this critical issue.

Tuesday, 4:00 PM - 4:45 PM

Does EDA Need a Roadmap for OS Support?

Moderator: Rich Goldman - *Synopsys, Inc.*
Panelists: Peter Denyer - *Sun Microsystems, Inc.*
Todd Barr - *Red Hat*
Mark Toth - *Cadence Design Systems, Inc.*

With so many OS choices and versions, how do you know your choices will be supported by the products you need? Get an update on the platforms outlook through 2009. Learn about the EDA Baseline OS Guideline and Roadmap being developed by the EDA Consortium.

Wednesday, 10:15 AM - 11:00 AM

Standards at the International Level

Moderator: Dennis Brophy - *Model Technology, Inc., a Mentor Graphics Co.*

Panelists: Laurent Maillet-Contoz - *STMicroelectronics*
Jim Heaton - *Design Automation Group*
Satoshi Kojima - *JEITA STD - TSC*
Edward Rashba - *IEEE Standards Assoc.*

Standards have gone global to support a global market. How do regional or nationalistic issues impact the development and adoption of standards in a global market? What standards activities for EDA or the larger electronics industry are taking place in international or regional settings?

Wednesday, 11:15 AM - 12:00 PM

IP Quality: State-of-the-Art Technical Approaches and Their Business Impacts

Moderator: Jim Tully - *Gartner Dataquest*

Panelists: Mike Keating - *Synopsys, Inc.*
Kurt Wolf - *TSMC*
Norbert Diesing - *PMC-Sierra, Inc.*

IP users demand nearly impossibly high quality, but suppliers constantly need to ask if they are willing to pay for that quality. This educational and interactive panel will survey state-of-the-art approaches to increasing IP quality.

Wednesday, 3:00 PM - 3:45 PM

Student Design Contest Award Presentations

Moderators: Alan Mantooth - *Univ. of Arkansas*
Bryan Ackland - *Bunyip Consulting*

Presentation of winners of the Student Design Contest, sponsored by the Design Automation Conference and the International Solid State Circuits Conference (ISSCC).

Thursday, 10:15 AM - 11:00 AM

ASIC, COT, or FPGA: Which Should Your Next Chip Be?

Moderator: Howard Baldwin - *Reed Electronics Group, Inc.*

Panelists: Ronnie Vasishta - *LSI Logic Corp.*
Robert Blake - *Altera Corp.*
Kamalesh Ruparel - *Cisco Systems, Inc.*

It used to be simple when deciding how to implement your next chip. If it was fairly simple and low-volume, you used FPGAs. If it was large or high-volume, you used an ASIC. If you wanted more design or cost control you could use a COT methodology. Now, the converging economic realities of engineering cost, manufacturing cost, and yield make that decision more complicated. FPGAs offer solutions that can rival low- and mid-range ASICs while design costs at advanced technology nodes have driven ASIC prices sky-high and out of the reach of many potential customers. COT customers find that the ROI is only worthwhile in a shrinking percentage of their designs. Is there a standard checklist on how to build your next chip?

Monday, June 7, 2004

	Room 6C	Room 11A & 11B	Room 6D	Room 3	Room 1A
9:00	**Tutorial 1** Getting Your "Cool ASIC" Up to Speed (Continental Breakfast 8:00 AM - 9:00 AM)	**Hands-on Tutorial** System-Level Power Management • *CoWare, Inc., Chip Design Systems AG, & PowerEscape,* Inc. **Room 11B**			
10:00					Introduction to Chips and EDA for a Non-Technical Audience 10:00 AM - 12:00 PM
12:00	Lunch				
1:00	**Tutorial 1 (cont.)** Getting Your "Cool ASIC" Up to Speed	**Hands-on Tutorial** Low-Power Design Methodologies and Tools • BullDAST srl, Accent Inc., & STMicroelectronics **Room 11A**	The Last Interoperability Workshop 12:00 PM - 5:00 PM	Lunch 1:00 PM Workshop for Women in Design Automation: Career and Life Drivers - "Passion vs. Ambition" 2:00 PM - 5:00 PM	
2:00					
5:00					

Booth #3733

DAC Pavilion

- EDA Business Forecast 9:15 - 10:00
- Wall Street Review of EDA-2004 Update 10:15 - 11:00
- EDA Mergers & Acquisitions Glory or Death? 11:15 - 12:00
- Export Controls in the Age of Globilization 2:00 - 2:45
- The Semiconductor IP Business in 2004 3:00 - 3:45
- User Forums or Useless Forums? 4:00 - 4:45

Exhibit Hours 9:00 AM - 6:00 PM

Tutorial 1 - Getting Your "Cool ASIC" Up to Speed: Practical Techniques and Tools to Achieve Custom Like Performance in a Power Aware Design Flow - see pg 36

Hands-on Tutorial - System-Level Power Management • CoWare, Inc., Chip Design Systems AG, & PowerEscape, Inc. • see pg 43

Hands-on Tutorial - Low-Power Design Methodologies and Tools • BullDAST s.r.l., Accent Inc., & STMicroelectronics • see pg 44

The Last Interoperability Workshop • see pg 39

Workshop for Women in Design Automation - Career and Life Drivers - "Passion vs. Ambition" see pg 40

Introduction to Chips and EDA for a Non-Technical Audience • see pg 41

Opening Session

Opening Remarks: Sharad Malik - *General Chair, 41st DAC* Ballroom 20ABC

Awards Presented By: Robert Walker, *ACM/SIGDA Representative*; Al Dunlop, *2004 IEEE/CASS Awards Presenter*

Awards/Scholarships

- Marie R. Pistilli Women in EDA Achievement Award
- P.O. Pistilli Undergraduate Scholarships (ACSEE)
- DAC Graduate Scholarships
- ACM/TODAES Best Paper Award
- ACM/SIGDA Distinguished Service Award
- Phil Kaufman Award
- IEEE/CASS Mac Van Valkenburg Award
- IEEE/CASS Meritorious Service Award
- IEEE/CASS Chapter-of-the-Year Award
- 2004 IEEE Fellows
- IEEE/CASS Donald O. Pederson Award
- IEEE/CASS Guillemin-Cauer Award

Keynote Address:

Gigascale Integration for Teraops Performance–Challenges, Opportunities and New Frontiers

Patrick P. Gelsinger - *Chief Technology Officer & Senior Vice President, Intel Corp.*

41 SAN DIEGO DAC JUNE 7 - 11, 2004

Tuesday June 8

8:30 to 10:00

All speakers are denoted in **bold**

§ – denotes short paper

ß – denotes best paper candidates

41 SAN DIEGO DAC
JUNE 7 - 11, 2004

Tuesday June 8 10:30 to 12:00

All speakers are denoted in **bold**

S – denotes short paper

ß – denotes best paper candidates

session topic area given on page 12

Business Sessions shaded blue

Session 1 — Methods/Tools — Rm: 6A

PANEL: CEO PANEL: EDA: THIS IS SERIOUS BUSINESS

CHAIR: A. Richard Newton - *Univ. of California, Berkeley, CA*
ORGANIZERS: Bob Dahlberg, Kurt Keutzer

Over the last 20 years, electronic design has grown to annual revenues of $3B per year and dominates the Technical and Systems Sector of the Software Industry. Cadence Design Systems, Inc. and Synopsys, Inc. are among the top 15 independent software vendors when ranked by market capitalization. In short, the EDA industry has come of age, but the future of the industry is far from certain. Where will the future growth of the industry come from? Are EDA revenues forever tied to the cyclical semiconductor industry? Will there ever be another "next great EDA company" or has the industry settled into a stable tri-opoloy?

Panelists:
Ray Bingham - *Cadence Design Systems, Inc., San Jose, CA*
Aart De Geus - *Synopsys, Inc., Mountain View, CA*
Walden C. Rhines - *Mentor Graphics Corp., Wilsonville, OR*

After the opening statements by the CEOs, Professor A. Richard Newton, Univ. of California at Berkeley, will moderate a series of questions posed by a panel of six questioneers.

Questioners:
Gary Banta - *Stretch, Inc.*
Richard Goering - *EETimes*
Jennifer Jordan - *Wells Fargo Bank, NA*
Mark Papermaster - *IBM Corp.*
Sunil Shenoy - *Intel Corp., Inc.*
Gary Smith - *Gartner Dataquest*

Session 2 — Methods/Tools — Rm: 6B

SPECIAL SESSION: HOT LEAKAGE

CHAIR: Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*
ORGANIZER: Lei He

Leakage has a growing importance due to technology scaling, and for better control thermal dependency must be considered to better control leakage. This session surveys state-of-the-art leakage reduction at device, circuit and system levels, and poses challenges and opportunities for further CAD development.

2.1 Circuit and Device Optimizations with Electrothermal Coupling in Scaled Technologies

Arman Vassighi - *Intel Corp., Kitchner, ON, Canada*
Ali Keshavarzi - *Intel Corp., Hillsboro, OR*
Siva Narendra - *Intel Corp., Hillsboro, OR*
Gerhard Schrom - *Intel Corp., Chandler, AZ*
S. Lee - *Intel Corp., Hillsboro, OR*
Greg Chysler - *Intel Corp., Chandler, AZ*
Y. Ye, Vivek De - *Intel Corp., Hillsboro, OR*

2.2 Leakage Estimation and Leakage Control for Nano-Scale CMOS Circuits

Kaushik Roy - *Purdue Univ., West Lafayette, IN*
Saibal Mukhopadhyay - *Univ. of Waterloo, Waterloo, ON, Canada*

2.3 System Level Leakage Reduction Considering the Interdependency between Temperature and Leakage

Lei He, Weiping Liao - *Univ. of California, Los Angeles, CA*
Mircea R. Stan - *Univ. of Virginia, Charlottesville, VA*

Session 3 — Methods/Tools — Rm: 6C

CLOCK ROUTING AND BUFFERING

CHAIR: John Lillis - *Univ. of Illinois, Chicago, IL*
ORGANIZERS: Dirk Stroobandt, Raymond Nijssen

This session presents three papers on clock routing and buffering that address critical design challenges in today's deep sub-micron regime. The first paper shows how to add cross-links to current clock tree routing constructions to reduce variability. The next paper presents a fast buffering technique that can handle a variety of physical environment constraints. The last paper in the session presents a method for choosing repeaters that minimize power while maintaining excellent delay characteristics, which is becoming an increasingly prevalent problem.

§3.1 Reducing Clock Skew Variability via Cross Links

Anand Rajaram, Jiang Hu, Rabi Mahapatra - *Texas A&M Univ., College Station, TX*

3.2 Fast and Flexible Buffer Trees That Navigate the Physical Layout Environment

Charles J. Alpert - *IBM Corp., Austin, TX*
Milos Hrkic - *Univ. of Illinois, Chicago, IL*
Jiang Hu - *Texas A&M Univ., College Station, TX,*
Stephen T. Quay - *IBM Corp., Austin, TX*

3.3 Practical Repeater Insertion For Low Power: What Repeater Library Do We Need?

Xun Liu, Yuantao Peng - *North Carolina State Univ., Raleigh, NC*
Marios C. Papaefthymiou - *Univ. of Michigan, Ann Arbor, MI*

Session 4 — Methods — Rm: 6D

TOOLS AND STRATEGIES FOR DYNAMIC VERIFICATION

CHAIR: Jacob Abraham - *Univ. of Texas, Austin, TX*
ORGANIZERS: Adnan Aziz, Yaron Kashi

Successful dynamic verification is built upon several closely linked concepts. This session addresses a number of these concepts: recent advances in test generation targeting processors, tools for measuring and analyzing functional coverage, and a regression strategy optimized for coverage.

§4.1 Industrial Experience with Test Generation Languages for Processor Verification

Michael Behm- *IBM Corp., Austin, TX*
Yossi Lichtenstein- *IBM Corp., Haifa, Israel*
John Ludden- *IBM Corp., Burlington, VT*
Michal Rimon, Michael Vinov - *IBM Corp., Haifa, Israel*

4.2s Defining Coverage Views to Improve Functional Coverage Analysis

Sigal Asaf, Eitan Marcus, Avi Ziv - *IBM Corp., Haifa, Israel*

4.3s Systematic Functional Coverage Metric Synthesis from Hierarchical Temporal Event Relation Graph

Young-Su Kwon, Young-Il Kim, Chong-Min Kyung - *KAIST, Daejeon, Republic of Korea*

4.4 Probabilistic Regression Suites for Functional Verification

Shai Fine, Shmuel Ur, Avi Ziv- *IBM Corp., Haifa, Israel*

Session 5 — Methods — Rm: 4

TIMING-DRIVEN SYSTEM SYNTHESIS

CHAIR: Prashant Sawkar - *Intel Corp., Hillsboro, OR*
ORGANIZERS: Gila Kamhi, Krzysztof Kuchcinski

This session includes papers discussing different approaches to timing-driven modular design. Results are provided on scalable system level design with tight connections to physical level timing requirements. The first two papers promote scalable and hierarchical design methodology through modular scheduling and formal synthesis of timing optimized scheduling algorithms. The last two papers discuss timing problems at the system-level in connection with physical design. Their approaches address the problem of handling system level long wire delays encountered at later design stages.

§5.1 Modular Scheduling of Dynamic Atomic Actions

Daniel L. Rosenband, Arvind - *Massachusetts Institute of Tech., Cambridge, MA*

5.2 Automatic Correct Scheduling of Control Flow Intensive Behavioral Descriptions in Formal Synthesis

Kai Kapp, Viktor Sabelfeld - *Univ. of Karlsruhe, Karlsruhe, Germany*

5.3s A Timing-Driven Module-Based Chip Design Flow

Fan Mo, Robert K. Brayton - *Univ. of California, Berkeley, CA*

5.4s Timing Closure through a Globally Synchronous Timing Partitioned Design Methodology

Anders Edman, Christer Svensson - *Linkoping Univ., Linkoping, Sweden*

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S – denotes short paper

B – denotes best paper candidates

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Session 6 — Methods/Tools — Rm: 6A

SPECIAL SESSION: RELIABLE SYSTEM-ON-A-CHIP DESIGN IN THE NANOMETER ERA

CHAIR: Chandu Visweswariah - *IBM Corp., Yorktown Heights, NY*
ORGANIZERS: Naresh Shanbhag, Giovanni De Micheli

Reliability of systems-on-chips (SOCs) is recognized to be the major problem of this decade. In addition to performance and power dissipation, SOCs also have to satisfy constraints on mean time to failure. The dramatic increase in complexity further compounds the problem. This special session will focus on the reliability problem in SOCs at the semiconductor process technology, algorithms, computation, communication, systems and software levels. These presentations will be coordinated to provide a comprehensive view of this important problem.

6.1 Design and Reliability Challenges in Nanometer Technologies
Shekhar Borkar, Tanay Karnik, Vivek De - *Intel Corp., Hillsboro, OR*

6.2s A Communication-Theoretic Design Paradigm for Reliable SoCs
Naresh Shanbhag - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

6.3s Reliable Communication in SoCs
Giovanni De Micheli - *Stanford Univ., Stanford, CA*

6.4s Designing Robust Microarchitectures
Todd Austin - *Univ. of Michigan, Ann Arbor, MI*

6.5s Hierarchical Application-Aware Error Detection and Recovery
Ravishankar K. Iyer - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

Session 7 — Methods/Tools — Rm: 6B

PANEL: WHEN IC YIELD MISSED THE TARGET, WHO IS AT FAULT?

CHAIR: Lucio Lanza - *Lanza techVentures, Palo Alto, CA*
ORGANIZER: Andrzej Strojwas

Silicon yield was once dominated by contaminants and particulates, making yield a process issue. But with today's electronics supply chain, multiple suspects may be indicted on manufacturability issues. Who is responsible for preventive actions in manufacturability and yield? The panelists, representing a foundry, a fabless company, an IP provider, two EDA vendors, and an IC design team, will discuss the problems and solutions for achieving manufacturability and yield goals.

Panelists:
Michael Campbell - *QUALCOMM, Inc., San Diego, CA*
Vassilios C. Gerousis - *Infineon Tech., Munich, Germany*
John Kibarian - *PDF Solutions, Inc., San Jose, CA*
Jim Hogan - *Telos Venture Partners, Palo Alto, CA*
Marc Levitt - *Cadence Design Systems, Inc., San Jose, CA*
Walter Ng - *Chartered Semiconductor Manufacturing, Inc., Milpitas, CA*
Dipu Pramanik - *Synopsys, Inc., Mountain View, CA*
Mark Templeton - *Artisan Components, Inc., Sunnyvale, CA*

Session 8 — Tools — Rm: 6C

POWER MODELING AND OPTIMIZATION FOR EMBEDDED SYSTEMS

CHAIR: Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*
ORGANIZERS: Luca Benini, Trevor Mudge

Embedded system designers critically need high-level models for software and hardware. This session includes contributions on advanced modeling and optimization approaches for critical system-level components, namely: on-chip interconnect, memory system, high speed IO links and software.

8.1 Memory Access Scheduling and Binding Considering Energy Minimization in Multi-Bank Memory Systems
Chun-Gi Lyuh - *ETRI, Daejeon, Republic of Korea*
Taewhan Kim - *Seoul National Univ., Seoul, Republic of Korea*

8.2 Profile-Based Optimal Intra-Task Voltage Scheduling for Hard Real-Time Applications
Jaewon Seo - *KAIST, Daejeon, Republic of Korea*
Taewhan Kim - *Seoul National Univ., Seoul, Republic of Korea*
Ki-Seok Chung - *Hanyang Univ., Seoul, Republic of Korea*

8.3 Requirement-Based Design Methods for Adaptive Communications Links
Juan Antonio Carballo, Kevin Nowka, Seung-Moon Yoo, Ivan Vo- *IBM Corp., Austin, TX*
Robert Norman, Clay Cranford - *IBM Corp., Raleigh, NC*

8.4s Automated Energy/Performance Macromodeling of Embedded Software
Anish Muttreja - *Princeton Univ., Princeton, NJ*
Anand Raghunathan, Srivaths Ravi - *NEC Labs., Princeton, NJ*
Niraj K. Jha - *Princeton Univ., Princeton, NJ*

8.5s Coding for System-on-Chip Networks: A Unified Framework
Srinivasa R. Sridhara, Naresh R. Shanbhag - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

Session 9 — Methods/Tools — Rm: 6D

PERFORMANCE EVALUATION AND RUN TIME SUPPORT

CHAIR: Joerg Henkel - *Univ. of Karlsruhe, Karlsruhe, Germany*

ORGANIZERS: Radu Marculescu, Rainer Leupers

Evaluating system performance is a critical issue in system design. Of particular interest is performance evaluation at higher levels of abstraction. The papers in this session cover techniques ranging from WCET to run-time support for various architectures and platforms. The first two papers deal with early performance estimation. The next two propose new optimization techniques for dynamic scheduling. Finally, the last paper presents an area estimation technique for reconfigurable devices.

§9.1 Abstraction of Assembler Programs for Symbolic Worst Case Execution Time Analysis
Tobias Schuele, Klaus Schneider - *Univ. of Kaiserslautern, Kaiserslautern, Germany*

9.2 Extending the Transaction Level Modeling Approach for Fast Communication Architecture Exploration
Sudeep Pasricha, Nikil Dutt - *Univ. of California, Irvine, CA*
Mohamed Ben-Romdhane - *Conexant Systems, Inc., Newport Beach, CA*

9.3 Specific Scheduling Support to Minimize the Reconfiguration Overhead of Dynamically Reconfigurable Hardware
Javier Resano - *Univ. Complutense de Madrid, Madrid, Spain*
Diederik Verkest - *IMEC, Leuven, Belgium*
Daniel Mozos - *Univ. Complutense de Madrid, Madrid, Spain*
Francky Catthoor, Serge Vernalde - *IMEC, Leuven, Belgium*

9.4s LODS: Locality-Oriented Dynamic Scheduling for On-Chip Multiprocessors
Mahmut Kandemir - *Penn State Univ., University Park, PA*

9.5s An Area Estimation Methodology for FPGA Based Designs at SystemC Level
Carlo Brandolese, Fabio Salice, William Fornaciari - *Politecnico di Milano, Milano, Italy*

Session 10 — Methods/Tools — Rm: 4

ADVANCES IN ANALOG CIRCUIT AND LAYOUT SYNTHESIS

CHAIR: Koen Lampaert - *Mindspeed Technologies, Inc., Newport Beach, CA*

ORGANIZERS: Georges G. Gielen, Koen Lampaert

This session deals with important advances in analog circuit and layout synthesis. The first paper presents a method for designing operational amplifiers using reversed geometric programming. The next paper describes an analog layout-centric reuse strategy. The third paper proposes techniques for fast estimation of parasitics during layout synthesis. Synthesis of reconfigurable analog circuits is described next. The session ends with a presentation on an electrical and physical synthesis flow for radio frequency integrated circuits.

§10.1 Automated Design of Operational Transconductance Amplifiers Using Reversed Geometric Programming
Johan P. Vanderhaegen, Robert W. Brodersen - *Univ. of California, Berkeley, CA*

10.2 Correct-by-Construction Layout-Centric Retargeting of Large Analog Designs
Sambuddha Bhattacharya, Nuttorn Jangkrajarng, Roy Hartono, Richard Shi - *Univ. of Washington, Seattle, WA*

10.3 Fast and Accurate Parasitic Capacitance Models for Layout-Aware Synthesis of Analog Circuits
Anuradha Agarwal, Hemanth Sampath, Veena Yelamanchili, Ranga Vemuri - *Univ. of Cincinnati, Cincinnati, OH*

10.4s ORACLE: Optimization with Recourse of Analog Circuits Including Layout Extraction
Yang Xu, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*
Stephen P. Boyd - *Stanford Univ., Stanford, CA*

10.5s A Synthesis Flow Toward Fast Parasitic Closure for Radio-Frequency Integrated Circuits
Gang Zhang - *Carnegie Mellon Univ., Pittsburgh, PA*
Aykut Dengi, Ronald A. Rohrer - *Neolinear, Inc., Pittsburgh, PA,*
Rob A. Rutenbar, L. Richard Carley - *Carnegie Mellon Univ., Pittsburgh, PA*

Session 100 — Rm: 6F

BUSINESS DAY: COMPETITIVE STRATEGIES FOR THE ELECTRONICS INDUSTRY

CHAIR: Alan Naumann - *CoWare, Inc., San Jose, CA*

ORGANIZER: Ellen M. Sentovich

Competing in today's economy requires close examination of current business practices and careful strategies for moving into the future. This session will examine three key areas for establishing competitive edge: globalization, patents, intellectual property management, and strategic marketing. Each talk will cover a broad spectrum of approaches, applicable to design, EDA, and IP-based companies. Conclusions will be drawn about what methods will be most successful moving into the next era of electronics. The final portion of the session is devoted to discussion, debate, and Q&A.

100.1 Competing in the Age of Globalization
Jaswinder Ahuja - *Cadence Design Systems, Inc., Noida, India*

100.2 Better, Faster, Cheaper Approaches to Patents: Managing Intellectual Property Strategically and Cost-Effectively
Paul Lippe - *Silicon Image, Sunnyvale, CA*

100.3 Competitive Marketing in an Evolving Electronics World
Bernie Roserthal - *Tensilica Inc., Santa Clara, CA*

100.4 Discussion/ Q&A

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Session 11 Methods/Tools Rm: 6A

POWER GRID DESIGN AND ANALYSIS TECHNIQUES

CHAIR: Eli Chiprout - *Intel Corp., Chandler, AZ*
ORGANIZERS: Abhijit Dharchoudhury, Lei He

This session deals with power grid and clock design and analysis. The first paper considers buffer sizing for low power with clock skew constraints. The second paper discusses optimal placement of power pads and pins. The third paper proposes a stochastic approach to P/G analysis and the fourth paper describes a practical application of macro-modeling to P/G analysis. The last paper presents a layout decompaction technique to correct EM failures.

11.1 Buffer Sizing for Clock Power Minimization Subject to General Skew Constraints
Kai Wang, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

11.2 Optimal Placement of Power Supply Pads and Pins
Min Zhao - *Freescale Semiconductor, Inc., Austin, TX*
Yuhong Fu, Vladimir Zolotov, Savithri Sundareswaran - *Motorola, Inc., Austin, TX*
Rajendran Panda - *Motorola, Inc., Austin, TX*

11.3 A Stochastic Approach to Power Grid Analysis
Sanjay Pant, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Vladimir Zolotov, Savithri Sundareswaran, Rajendran Panda - *Motorola, Inc., Austin, TX*

11.4s Efficient Power/Ground Network Analysis for Power Integrity-Driven Design Methodology
Shu-Wei Wu - *Elan Microelectronics Corp., Hsinchu, Taiwan*
Yao Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

11.5s Reliability-Driven Layout Decompaction for Electromigration Failure Avoidance in Complex Mixed-Signal IC-Designs
Goeran Jerke - *Robert Bosch GmbH, Reutlingen, Germany*
Jens Lienig - *Dresden Univ. of Tech., Dresden, Germany*
Juergen Scheible - *Robert Bosch GmbH, Reutlingen, Germany*

Session 12 Methods/Tools Rm: 6B

PANEL: WHAT HAPPENED TO ASIC? GO (RECON)FIGURE?

CHAIR: Kurt Keutzer - *Univ. of California, Berkeley, CA*
ORGANIZERS: Nitin Deo, Behrozz Zahiri

Increasing design cost and risk is causing more and more designers to build configurable platforms that will amortize design and manufacturing costs across many generations. Several reconfiguration schemes exist and none of them seems to be a clear winner. Most notably there are three forms of technology: structured ASIC, configurable software programmable, reconfigurable FPGA-like platform. New solutions are emerging and may induce drastic changes in the current industry organization. The panel will examine factors in the success of the various options, and look to what the future might bring.

Panelists:
Phillip LoPresti - *NEC Electronics America, Inc., Santa Clara, CA*
Ray Simar - *Texas Instruments, Inc., Stafford, TX*
Chris Rowen - *Tensilica, Inc., Santa Clara, CA*
Bhusan Gupta - *STMicroelectronics, Berkeley, CA*
Chris Reynolds - *IBM Corp., Essex Junction, VT*
Ivo Bolsens - *Xilinx, Inc., San Jose, CA*
Jason Cong - *Magma Design Automation, Inc., Los Angeles, CA*

Session 13 Methods/Tools Rm: 6C

METHODS FOR A PRIORI FEASIBLE LAYOUT GENERATION

CHAIR: K. S. (Hardy) Leung - *Magma Design Automation, Inc., Santa Clara, CA*
ORGANIZERS: Charles J. Alpert, Dirk Stroobandt, Raymond Nijssen

This session combines methods that demonstrate the effectiveness of a priori-correct layout generation. The first paper addresses this by modeling the effects of modern lithography so as to avoid routing patterns complicating optical proximity correction. The following three papers focus on a topic of great interest: regular fabrics for improved manufacturing yield and cost. These papers successfully narrow the flexibility gap between regular and structured ASICs. The final paper discusses improved layout predictability through more accurate pre-layout standard cell characterization.

13.1 Optical Proximity Correction (OPC)-Friendly Maze Routing
Li-Da Huang - *Univ. of Texas, Austin, TX*
Martin D.F. Wong - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

13.2 Design Automation for Mask Programmable Fabrics
Narendra V. Shenoy - *Synopsys, Inc., Bangalore, India*
Jamil Kawa, Raul Camposano - *Synopsys, Inc., Mountain View, CA*

13.3 On Designing Via-Configurable Cell Blocks for Regular Fabrics
Yajun Ran, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

13.4s Routing Architecture Exploration for Regular Fabrics
Veerbhan Kheterpal - *Carnegie Mellon Univ., Pittsburgh, PA*

13.5s Accurate Pre-Layout Estimation of Standard Cell Characteristics
Hiroaki Yoshida, Kaushik De, Vamsi Boppana - *Zenasis Technologies, Inc., Campbell, CA*

Session 14 — Tools — Rm: 6D

ABSTRACTION TECHNIQUES FOR FUNCTIONAL VERIFICATION

CHAIR: Vigyan Singhal - *Jasper Design Automation, Inc., Mountain View, CA*

ORGANIZERS: Karem A. Sakallah, Rajeev Ranjan

Abstraction techniques are essential for improving the capacity and performance of formal functional verification tools. The first paper combines bit-level SAT and word-level ILP solvers to verify both the control and datapath of RTL designs. The second paper performs automatic uninterpreted function abstraction of Verilog models to establish functional equivalence between an RTL design and its specification. The third paper enhances state-of-the-art abstraction refinement techniques by using two novel metrics. The last two papers describe case studies which demonstrate how real world designs can be effectively verified using formal methods.

14.1 An Efficient Finite-Domain Constraint Solver for Circuits

Ganapathy Parthasarathy, Madhu K. Iyer, Kwang T. Cheng, Li C. Wang - *Univ. of California, Santa Barbara, CA*

14.2 Automatic Abstraction and Verification of Verilog Models

Zaher S. Andraus, Karem A. Sakallah - *Univ. of Michigan, Ann Arbor, MI*

14.3 Abstraction Refinement by Controllability and Cooperativeness Analysis

Freddy Y. C. Mang - *Synopsys, Inc., Mountain View, CA*
Pei-Hsin Ho - *Synopsys, Inc., Portland, OR*

14.4s Verifying a Gigabit Ethernet Switch Using SMV

Yuan Lu, Mike Jorda - *Broadcom Corp., San Jose, CA*

14.5s A General Decomposition Strategy for Verifying Register Renaming

Hazem I. Shehata, Mark D. Aagaard - *Univ. of Waterloo, Waterloo, ON, Canada*

Session 15 — Methods/Tools — Rm: 4

MEMORY AND NETWORK OPTIMIZATION IN EMBEDDED DESIGNS

CHAIR: Faraydon Karim - *STMicroelectronics, La Jolla, CA*

ORGANIZERS: Adam Donlin, Grant E. Martin

Generic methods for designing memory and communications architectures for embedded applications are completely insufficient for modern design. This session presents advanced results in new approaches to optimizing memory and network architectures. The first two papers cover run-time scratchpad structures and code compression. The next one links the themes of memory subsystem and on-chip networks together for multi-processor SoC. The final two short papers cover particular aspects of SoC design: moving OS functions for SoC to hardware and designing new hybrid routing algorithms to optimize on-chip communication.

§15.1 An Integrated Hardware Software Approach for Run-Time Scratchpad-Management

Francesco Poletti - *Univ. Di Bologna, Bologna, Italy*
Paul Marchal - *IMEC, Leuven, Belgium*
David Atienza - *DACYA/UCM, Madrid, Spain*
Luca Benini - *Univ. Di Bologna, Bologna, Italy*
Francky Catthoor - *IMEC, Leuven, Belgium*
Jose Mendias - *DACYA/UCM, Madrid, Spain*

15.2 Multi-Profile Based Code Compression

Eduardo B. Wanderleynetto, Rodolfo J. Azevedo, Paulo C. Centoducatte, Guido S. Araujo - *IC-UNICAMP, Campinas, Brazil*

15.3 An Efficient Scalable and Flexible Data Transfer Architecture for Multiprocessor SoC with Massive Distributed Memory

Sang Il Han - *Seoul National Univ., Seoul, Republc of Korea*
Amer Baghdadi - *ENST Bretagne, Brest, France*
Bonaciu B. Marius Petru- *TIMA Lab., Grenoble, France*
Soo Ik Chae - *Seoul National Univ., Seoul, Republic of Korea*
Ahmed Amine Jerraya - *TIMA Lab., Grenoble, France*

15.4s Operating-System Controlled Network on Chip

Vincent Nollet, Theodore M. Marescaux, Diederik Verkest, Jean-Yves Mignolet, Serge Vernalde - *IMEC, Leuven, Belgium*

15.5s DyAD – Smart Routing for Networks-on-Chip

Jingcao Hu, Radu Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

Session 150 — Rm: 6F

BUSINESS DAY: BUSINESS MODELS IN IP, SOFTWARE LICENSING, AND SERVICES

CHAIR: Lucio Lanza - *Lanza techVentures, Palo Alto, CA*

ORGANIZER: Ellen M. Sentovich

A variety of business models in design and design automation are being employed today that have a dramatic effect on the success of individual companies and of multiple industries within the domain of electronics. The three talks in this session will study models for managing IP, software licensing, design and EDA services. A variety of approaches, constraints, and case studies will be presented in each case, with conclusions about how to make these models most successful for all parties involved. The final portion of the session is devoted to discussion, debate, and Q&A.

150.1 Who Needs What, and Where They Find It

Raul Camposano - *Synopsys, Inc., Mountain View, CA*

150.2 Licensing Options: Finding the Win-Win

Jim Douglas - *ReShape, Inc., Mountain View, CA*

150.3 Integrated Design/Supply Chain Models to Accelerate Product Development

Aurangzeb Khan - *Cadence Design Systems, Inc., San Jose, CA*

150.4 Discussion/Q&A

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Session 16 — Methods/Tools — Rm: 6A

SPECIAL SESSION: THE FUTURE OF TIMING CLOSURE

CHAIR: Phiroze Parakh - *Sierra Design Automation, Inc., Santa Clara, CA*
ORGANIZER: Charles J. Alpert

Timing closure is far from solved, and approaches are diverging. Leading-edge methodologies cope with variability, leakage, and wiring predictability, while new "platform tools" aim for chip-level optimization, and academic research offers the promise of "single-pass" closure at long last.

16.1 Timing Closure for Low-FO4 Microprocessor Design
Daivd S. Kung - *IBM Corp., Yorktown Heights, NY*

16.2 Forest vs. Trees: Where's the Slack?
Paul Rodman - *ReShape, Inc., Mountain View, CA*

16.3 Efficient Timing Closure Without Timing Driven Placement and Routing
Miodrag Vujkovic, David Wadkins - *Univ. of Washington, Seattle, WA*
William Swartz - *InternetCAD.com, Inc., Dallas, TX*
Carl Sechen - *Univ. of Washington, Seattle, WA*

Session 17 — Methods/Tools — Rm: 6B

PANEL: VERIFICATION, WHAT WORKS AND WHAT DOESN'T

CHAIR: Robert Damiano - *Synopsys, Inc., Hillsboro, OR*
ORGANIZER: Francine Bacchini

Today's leading chip and system companies are faced with ever increasing design verification challenges; industry studies reveal that as much as 50% of the total schedule is being spent in verification. Large companies, with almost infinite resources, have shown that throwing CPU cycles and people at the simulation problem still doesn't guarant ee a level of coverage desired by the design team.

So, what is the answer? Are assertions, faster simulators, and testbench languages the "holy grail", or are they just micro-optimizations of a methodology that is fundamentally flawed? Is there hope for a verification methodology that completely covers a design with a predictable verification schedule?

The panelists will describe their experiences of what works and what doesn't, providing insights into their methodologies and philosophies.

Panelists:
Bob Bentley - *Intel Corp., Hillsboro, OR*
Makoto Ishii - *Sony Corp., Osaki Shinagawa-Ku, Japan*
Einat Yogev - *Cisco Systems, Inc., San Jose, CA*
Kurt Baty - *WSFDB Consulting, Austin, TX*
Kevin Normoyle - *Azul Systems, Inc., Mountain View, CA*

Session 18 — Tools — Rm: 6C

DESIGN SPACE EXPLORATION AND SCHEDULING FOR EMBEDDED SOFTWARE

CHAIR: Mahmut Kandemir - *Penn State Univ., University Park, PA*
ORGANIZERS: Heinrich Meyr, Lothar Thiele, Mahmut Kandemir

Future embedded systems have to deal with increasing heterogeneity on the one hand and influence from physical implementation on the other hand to achieve the required performance in an energy efficient way. In this session we address the exploration from both caches and the system level viewpoint. In addition, power constraints under the current constraints of leakage are discussed.

18.1 Leakage Aware Dynamic Voltage Scaling for Real-Time Embedded Systems

Ravindra Jejurikar - *Univ. of California, Irvine, CA*
Cristiano Pereira, Rajesh Gupta - *Univ. of California, San Diego, La Jolla, CA*

18.2 Retargetable Profiling for Rapid, Early System Level Design Space Exploration

Lukai Cai, Andreas Gerstlauer, Daniel Gajski - *Univ. of California, Irvine, CA*

18.3 High Level Cache Simulation for Heterogeneous Multiprocessors

Joshua J. Pieper - *Carnegie Mellon Univ., Pittsburgh, PA*
Alain Mellan - *STMicroelectronics, San Diego, CA*
Joann M. Paul, Donald E. Thomas - *Carnegie Mellon Univ., Pittsburgh, PA*
Faraydon Karim - *STMicroelectronics, San Diego, CA*

Session 19 — Methods — Rm: 6D

ADVANCES IN ACCELERATED SIMULATION

CHAIR: Wolfgang Roesner - *IBM Corp., Austin, TX*
ORGANIZERS: Avi Ziv, Yaron Kashi

This session discusses techniques for achieving high performance simulations for SoCs and other complex designs. The approaches vary from circuit aware architectural level simulation to efficient co-simulation with hardware acceleration.

19.1 Communication-Efficient Hardware Acceleration for Fast Functional Simulation

Young-Il Kim, Wooseung Yang, Young-Su Kwon, Chong-Min Kyung - *KAIST, Daejeon, Republic of Korea*

19.2 A Fast Hardware/Software Co-Verification Method for System-on-a-Chip by Using a C/C++ Simulator and FPGA Emulator with Shared Register Communication

Yuichi Nakamura, Kouhei Hosokawa, Ichiro Kuroda - *NEC Corp., Kawasaki-City, Japan*
Ko Yoshikawa - *NEC Corp., Fuchu-City, Japan*
Takeshi Yoshimura - *Waseda Univ., Kitakyusyu-City, Japan*

19.3 Circuit-Aware Architectural Simulation

Seokwoo Lee, Shidhartha Das, Valeria Bertacco, Todd Austin, David Blaauw, Trevor Mudge - *Univ. of Michigan, Ann Arbor, MI*

Session 20 — Tools — Rm: 4

DESIGN FOR MANUFACTURABILITY

CHAIR: Ruiqi Tian - *Motorola, Inc., Austin, TX*
ORGANIZERS: Charlie Chung-Ping Chen, Martin D.F. Wong

This session addresses design for manufacturability issues. The first paper presents a methodology to derive manufacturability-driven design rules so that RET effects can be anticipated during the design phase. The second paper presents an AltPSM-driven routing strategy that produces layouts, which are phase correct. The third paper presents a timing methodology that takes systematic variations into account. Finally, the last paper presents a technique to reduce leakage and its variability.

20.1 Toward a Methodology for Manufacturability Driven Design Rule Exploration

Luigi Capodieci - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Puneet Gupta, Andrew B. Kahng - *Univ. of California, at San Diego, La Jolla, CA,*
Dennis Sylvester, Jie Yang, - *Univ. of Michigan, Ann Arbor, MI*

20.2s Phase Correct Routing for Alternating Phase Shift Masks

Kevin Mccullen - *IBM Corp., Essex Junction, VT*

20.3 Toward a Systematic-Variation Aware Timing Methodology

Puneet Gupta - *Univ. of California, San Diego, La Jolla, CA*
Fook-Luen Heng - *IBM Corp., Yorktown Heights, NY*

20.4s Selective Gate-Length Biasing for Cost-Effective Runtime Leakage Control

Puneet Gupta, Andrew B. Kahng, Puneet Sharma - *Univ. of California, San Diego, La Jolla, CA*
Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*

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All speakers are denoted in **bold**

S – denotes short paper

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Session 21 — Tools — Rm: 6A

STATISTICAL TIMING ANALYSIS

CHAIR: Anirudh Devgan - *IBM Corp., Austin, TX*
ORGANIZERS: Charlie Chung-Ping Chen, Sani R. Nassif

This session presents several new approaches to statistical static timing analysis. The first paper describes an incremental statistical timing approach based on a block-based traversal of the timing graph. The second paper proposes a way to compute the bounds on the distribution of circuit delay for timing graphs with arbitrary delay correlations. The third paper proposes an alternative approach to block-based statistical timing computation.

ß21.1 First-Order Incremental Block-Based Statistical Timing Analysis

Chandu Visweswariah - *IBM Corp., Yorktown Heights, NY*
Kaushik Ravindran - *Univ. of California, Berkeley, CA*
Kerim Kalafala - *IBM Corp., Hopewell Junction, NY*
Steven G. Walker - *IBM Corp., Yorktown Heights, NY*
Sambasivan Narayan - *IBM Corp., Essex Junction, VT*

21.2 Fast Statistical Timing Analysis Handling Arbitrary Delay Correlations

Michael Orshansky, Arnab Bandyopadhyay - *Univ. of Texas, Austin, TX*

21.3 STAC: Statistical Timing Analysis with Correlation

Jiayong Le, Xin Li, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

Session 22 — Methods/Tools — Rm: 6B

PANEL: SYSTEM-LEVEL DESIGN: SIX SUCCESS STORIES IN SEARCH OF AN INDUSTRY

CHAIR: Grant E. Martin - *Tensilica, Inc., Santa Clara, CA*
ORGANIZERS: Francine Bacchini, Rita Glover

System-level design is being touted as the "holy grail" that the electronics industry has long sought, but most offers have been disappointing because they seldom deliver results. Many designers are fed up with the "Blah, Blah" on system-level design as they are waiting for design facts.

Why? It seems that major breakthroughs are happening thanks to the adoption of a standard direction for modeling design at higher than RTL level. These models are called TLM and new languages are being adopted (SystemC, SystemVerilog). The emergence of new standards may reshape completely the way the design industry is organized.

This panel will bring six speakers relating their success stories about design, starting at the system-level. The format is that of an educational panel aimed at informing DAC attendees of the challenges (difficulties and pitfalls) and opportunities (sizable benefits and lessons learned from these experiences).

Panelists:

Pierre Paulin - *STMicroelectronics, Ottawa, ON, Canada*
Arie Bernstein - *Intel Corp., Haifa, Israel*
Reinaldo A. Bergamaschi - *IBM Corp., Yorktown Heights, NY*
Ramesh Chandra - *QUALCOMM, Inc., San Diego, CA*
Raj Pawate - *Texas Instruments, Bangalore, India*
Mohamed Ben-Romdhane - *Conexant, Newport Beach, CA*

Session 23 — Tools — Rm: 6C

NEW IDEAS IN PLACEMENT

CHAIR: Patrick H. Madden - *University of Kitakyushu, Kitakyushu, NY*

ORGANIZERS: Carl Sechen, Igor L. Markov

This session covers a broad range of topics, including a novel geometric placement algorithm, a high-impact improvement of recursive bisection, and layout of quantum cellular automata (QCA).

§23.1 Large-Scale Placement by Grid-Warping

Zhong Xiu, James D. Ma - *Carnegie Mellon Univ., Pittsburgh, PA*
Suzanne M. Fowler - *Intel Corp., Chandler, AZ*
Rob A. Rutenbar - *Carnegie Mellon Univ., Pittsburgh, PA*

23.2 Placement Feedback: A Concept and Method for Better Min-Cut Placements

Andrew B. Kahng, Sherief Reda - *Univ. of California, San Diego, La Jolla, CA*

23.3 Quantum-Dot Cellular Automata (QCA) Circuit Partitioning: Problem Modeling and Solutions

Dominic A. Antonelli, Danny Z. Chen, Timothy J. Dysart, Xiaobo S. Hu - *Univ. of Notre Dame, Notre Dame, IN*
Andrew B. Kahng - *Univ. of California, San Diego, La Jolla, CA*
Peter M. Kogge, Richard C. Murphy, Michael T. Niemier - *Univ. of Notre Dame, Notre Dame, IN*

Session 24 — Tools — Rm: 6D

MODEL ORDER REDUCTION AND VARIATIONAL TECHNIQUES FOR PARASITIC ANALYSIS

CHAIR: Luca Daniel - *Massachusetts Institute of Tech, Cambridge, MA*

ORGANIZERS: Byron L. Krauter, Vikram Jandhyala

This session presents new advances in model order reduction and variational techniques for parasitic analysis. The first paper presents an efficient project-and-balance scheme for passivity preserving model order reduction. The next paper presents a linear fractional transform based model for interconnect parametric uncertainty. The third paper extends closed-form moment-based delay and slew metrics to consider back-end process variation. The final paper presents a model order reduction scheme that exploits input information in massively coupled parasitic networks to produce compact models.

§24.1 Passivity-Preserving Model Reduction via a Computationally Efficient Project-and-Balance Scheme

Ngai Wong - *Univ. of Hong Kong, Hong Kong, Hong Kong*
Venkataramanan Balakrishnan, Cheng-Kok Koh - *Purdue Univ., West Lafayette, IN*

24.2 A Linear Fractional Transform (LFT) Based Model for Interconnect Parametric Uncertainty

Janet Wang, Omar A. Hafiz - *Univ. of Arizona, Tucson, AZ*
Jun Li - *eTop Design Technology, Inc., Sunnyvale, CA*

24.3s Variational Delay Metrics for Interconnect Timing Analysis

Kanak Agarwal, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Frank Liu, Sani Nassif - *IBM Corp., Austin, TX*
Sarma Vrudhula - *Univ. of Arizona, Tucson, AZ*

24.4s Exploiting Input Information in a Model Reduction Algorithm for Massively Coupled Parasitic Networks

Miguel Silveira - *INESC, Lisbon, Portugal*
Joel R. Phillips - *Cadence Berkeley Labs., San Jose, CA*

Session 25 — Tools — Rm: 4

COMPILATION TECHNIQUES FOR EMBEDDED APPLICATIONS

CHAIR: Heinrich Meyr - *RWTH Aachen/CoWare, Inc., Aachen, DEU*

ORGANIZER: Mahmut Kandemir

The increasing software content in embedded systems makes it imperative to consider code optimizations. These techniques are of key importance to the design of heterogeneous application specific SoCs. The papers in this session range from compilation for customized memory architectures to instruction set design.

25.1 Automatic Translation of Software Binaries onto FPGAs

Gaurav Mittal, David C. Zaretsky, Xiaoyong Tang, Prithviraj Banerjee - *Northwestern Univ., Evanston, IL*

25.2 Area-Efficient Instruction Set Synthesis for Reconfigurable System-on-Chip Designs

Philip Brisk, Adam Kaplan, Majid Sarrafzadeh - *Univ. of California, Los Angeles, CA*

§25.3 Data Compression for Improving SPM Behavior

Ozcan Ozturk, Mahmut Kandemir - *Penn State Univ., University Park, PA*
Ilteris Demirkiran - *Syracuse Univ., Syracuse, NY,*
Guangyu Chen, Mary Jane Irwin - *Penn State Univ., University Park, PA*

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Session 26 — Methods/Tools — Rm: 6A

SPECIAL SESSION: PLATFORM-BASED SYSTEM DESIGN

CHAIR: Sujit Dey - *Univ. of California, San Diego, La Jolla, CA*
ORGANIZER: Sujit Dey

Rising design complexity and NRE/manufacturing costs of ASICs pushes the industry toward reuse. Platforms are emerging as an alternative to System-on-Chips rather than reuse of components, use of platforms potentially eliminates need for backend design. This special session will analyze and evaluate the characteristics and strengths/weaknesses of different types of platforms and their applicability to different segments of the semiconductor industry. Key issues regarding their adoption, including EDA and Software Support will also be addressed.

26.1s Platform Based Design: Does it Answer the Entire SoC Challenge?
Gary Smith - *Gartner Dataquest, San Jose, CA*

26.2 Nomadic Platform Approach for Wireless Mobile Multimedia
Mark Hopkins - *STMicroelectronics, San Diego, CA*

26.3 Benefits and Challenges for Platform-Based Design
Alberto L. Sangiovanni-Vincentelli, Luca Carloni - *Univ. of California, Berkeley, CA*
Fernando De Bernadinis - *Univ. of Pisa, Pisa, Italy*
Marco Sgroi - *Docomo Euro Labs., Munich, Germany*

26.4 Trends in the Use of Re-Configurable Platforms
Max Baron - *In-Stat/MDR, San Jose , CA*

26.5s Discussion: Q&A

Session 27 — Methods/Tools — Rm: 6B

INNOVATIONS IN LOGIC SYNTHESIS

CHAIR: Rajeev Murgai - *Fujitsu Labs., Sunnyvale, CA*
ORGANIZERS: Marek Perkowski, Soha Hassoun

Logic synthesis continues to play a critical role in Design Automation. The first paper presents a novel recursive approach to finding a minimal function that represents a Boolean relationship. The second paper describes a fast technique for computing approximate CODCs for large circuits based on computing the CODCs of smaller sub-networks. The third paper discusses BDD-based functional decomposition into a cascade of LUTs with intermediate outputs. The fourth paper proposes a novel algorithm to compute symmetries in incompletely specified functions. The final paper introduces new circuit restructuring techniques based on implicit enumeration of all possible restructuring patterns.

ß27.1 A Recursive Paradigm to Solve Boolean Relations
David Bañeres, Jordi Cortadella - *Univ. Politecnica Catalunya, Barcelona, Spain*
Mike Kishinevsky - *Intel Corp., Hillsboro, OR*

27.2 A Robust Algorithm for Approximate Compatible Observability Don't Care (CODC) Computation
Nikhil Saluja, Sunil Khatri - *Univ. of Colorado, Boulder, CO*

27.3 A Method to Decompose Multiple-Output Logic Functions
Tsutomu Sasao, Munehiro Matsuura - *Kyushu Institute of Tech., Iizuka, Japan*

27.4s Symmetry Detection for Incompletely Specified Functions
Kuo-Hua Wang, Jia-Huang Chen - *Fu Jen Catholic Univ., Taipei, Taiwan*

27.5s Implicit Enumeration of Structural Changes in Circuit Optimization
Victor N. Kravets, Prabhakar Kudva - *IBM Corp., Yorktown Heights, NY*

Session 28 — Tools — Rm: 6C

YIELD ESTIMATION AND OPTIMIZATION

CHAIR: John Cohn - *IBM Corp., Essex Junction, VT*
ORGANIZERS: Michael Orshansky, Sudhakar Bobba

Process variability has come to the forefront of the concerns of the design and EDA communities. The recent work on statistical static timing is an example of the response of the EDA community to this important area. This session is an indicator of the next wave of research in this area, one that will begin to apply these algorithms to estimate and optimize the timing yield of a design.

§28.1 Parametric Yield Estimation Considering Leakage Variability
Rajeev R. Rao - *Univ. of Michigan, Ann Arbor, MI*
Anirudh Devgan - *IBM Corp., Austin, TX*
David Blaauw, Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*

28.2 A Methodology to Improve Timing Yield in the Presence of Process Variations
Sreeja Raj, Sarma Vrudhula, Janet M. Wang - *Univ. of Arizona, Tucson, AZ*

28.3 Novel Sizing Algorithm for Yield Improvement under Process Variation in Nanometer Technology
Seung Hoon Choi - *Intel Corp., Hillsboro, OR*
Bipul C. Paul, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

28.4 Statistical Timing Analysis Based on a Timing Yield Model
Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*
Noel Menezes - *Intel Corp., Hillsboro, OR*

Session 29 — Methods/Tools — Rm: 6D

HIGH-LEVEL TECHNIQUES FOR SIGNAL PROCESSING

CHAIR: Stephen A. Edwards - *Columbia Univ., New York, NY*
ORGANIZERS: Reinaldo A. Bergamaschi, Stephen A. Edwards

The papers in this session deal with high-level synthesis problems that appear in signal processing applications. The first paper applies transaction-level modeling to DSP applications. The next three papers deal with choosing word lengths in hardware implementations of DSP applications. The last paper synthesizes error-correcting codes that greatly reduce wiring costs.

29.1 System Design for DSP Applications in Transaction Level Modeling Paradigm
Abhijit K. Deb - *Royal Institute of Tech., Kista, Sweden*
Axel Jantsch - *Royal Institute of Tech., Stockholm, Sweden*
Johnny Oberg - *Royal Institute of Tech., Kista, Sweden*

29.2 An Analytical Approach for Dynamic Range Estimation
Bin Wu, Jianwen Zhu, Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*

29.3 Automated Fixed-Point Data-Type Optimization Tool for Signal Processing and Communication Systems
Changchun Shi, Robert W. Brodersen - *Univ. of California, Berkeley, CA*

29.4s An Algorithm for Converting Floating-Point Computations to Fixed-Point in MATLAB Based FPGA Design
Sanghamitra Roy, Prith Banerjee - *Northwestern Univ., Evanston, IL*

29.5s Synthesizing Interconnect-Efficient Low Density Parity Check Codes
Marghoob Mohiyuddin, Amit Prakash, Adnan Aziz - *Univ. of Texas, Austin, TX*
Wayne Wolf - *Princeton Univ., Princeton, NJ*

Session 30 — Tools — Rm: 4

ADVANCED TEST SOLUTIONS

CHAIR: Paolo Prinetto - *Politecnico di Torino, Torino, Italy*
ORGANIZERS: TM Mak, Yervant Zorian

Novel and efficient solutions to test for very deep submicron chips are presented in this session. These solutions address a number of optimization factors, including: reducing power, identifying critical paths, diagnosing FPGA faults and optimizing silicon debug.

30.1 On Path-Based Learning and Its Applications in Delay Test and Diagnosis
Li C. Wang - *Univ. of California, Santa Barbara, CA*
TM Mak - *Intel Corp., Santa Clara, CA*
Kwang-Ting Cheng - *Univ. of California, Santa Barbara, CA,*
Magdy S. Abadir - *Motorola, Inc., Austin, TX*

§30.2 Efficient On-Line Testing of FPGAs with Provable Diagnosabilities
Vinay Verma - *Xilinx, Inc., San Jose, CA*
Shantanu Dutt, Vishal Suthar - *Univ. of Illinois, Chicago, IL*

30.3 On Test Generation for Transition Faults with Minimized Peak Power Dissipation
Wei Li, Sudhakar M. Reddy - *Univ. of Iowa, Iowa City, IA*
Irith Pomeranz - *Purdue Univ., West Lafayette, IN*

30.4s A New State Assignment Technique for Testing and Low Power
Sungju Park, Sangwook Cho - *Hanyang Univ., Ansan, Republic of Korea*
Seiyang Yang - *Pusan Univ., Pusan, Republic of Korea,*
Maciej Ciesielski - *Univ. of Massachusetts, Amherst, MA*

30.5s Automatic Generation of Breakpoint Hardware for Silicon Debug
Bart Vermeulen - *Philips Research Labs., Eindhoven, The Netherlands*
Mohammad Z. Urfianto - *Royal Institute of Tech., Kista, Sweden*
Sandeep K. Goel - *Philips Research Labs., Eindhoven, The Netherlands*

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Session 31 — Tools — Rm: 6A

ADVANCES IN BOOLEAN ANALYSIS TECHNIQUES

CHAIR: Aarti Gupta - *NEC Corp., Princeton, NJ*
ORGANIZERS: Pei-Hsin Ho, Tony Ma

Recent years have witnessed significant advances in the scalability and applicability of Boolean reasoning methods in a variety of EDA problems. Papers in this session represent significant extensions to the state-of-the-art technology in this area. The first paper proposes a SAT-based method for diagnosing infeasibility. The second paper uses re-parametrization to improve symbolic simulation. The third paper presents efficient symmetry detection methods. The last two papers describe methods for enhancing bounded model checking and combinational equivalence checking.

ß31.1 AMUSE: A Minimally-Unsatisfiable Subformula Extractor
Yoonna Oh, **Maher N. Mneimneh**, Zaher S. Andraus, Karem A. Sakallah, Igor L. Markov - *Univ. of Michigan, Ann Arbor, MI*

31.2 A SAT-Based Algorithm for Reparameterization in Symbolic Simulation
Pankaj P. Chauhan, Edmund M. Clarke, Daniel Kroening - *Carnegie Mellon Univ., Pittsburgh, PA*

31.3 Exploiting Structure in Symmetry Generation for CNF
Paul T. Darga, Mark H. Liffiton, Karem A. Sakallah, Igor L. Markov - *Univ. of Michigan, Ann Arbor, MI*

31.4s Refining the SAT Decision Ordering for Bounded Model Checking
Chao Wang, HoonSang Jin, Gary D. Hachtel, Fabio Somenzi - *Univ. of Colorado, Boulder, CO*

31.5s Efficient Equivalence Checking with Partitions and Hierarchical Cut-Points
Demosthenes Anastasakis, **Lisa R. McIlwain** - *Synopsys, Inc., Hillsboro, OR*
Slawomir Pilarski - *Univ. of Washington, Tacoma, WA*

Session 32 — Methods/Tools — Rm: 6B

PANEL: WERE THE GOOD OLD DAYS ALL THAT GOOD? EDA THEN AND NOW

CHAIR: William H. Joyner, Jr. - *IBM Corp./SRC, Research Triangle Park, NC*
ORGANIZERS: Shishpal Rawat, William H. Joyner, Jr.

A long, long time ago, in a laboratory far, far away, EDA researchers and developers used paper tape instead of Linux, rubylith instead of GDS II, yellow wires instead of ten levels of metal. Sitting around a potbellied stove, in their rocking chairs, practitioners of that era (and this) will offer insight into why some great ideas were immediately put into practice while others stayed on the drawing board or in the ivory tower. They will share remembrances of things past, of simpler days when foundries made steel, when options meant CMOS or bipolar, when real parts were measured instead of benchmarks touted. Their stories of what it was like, what has changed, and whether the "good old days" were then or now will be followed by questions and, possibly, answers.

Panelists:
John Darringer - *IBM Corp., Yorktown Heights, NY*
Hugo De Man - *IMEC, Leuven, Belgium*
Daniel Gajski - *Univ. of California, Irvine, CA*
Carl Harris - *Kluwer Academic Publishers, Norwell, MA*
P.O. Pistilli - *MP Associates, Inc., Boulder, CO*
Jim Solomon - *Independent Technology Advisor, Los Gatos, CA*

Session 33 — Methods/Tools — Rm: 6C

POWER OPTIMIZATION FOR REAL-TIME AND MEDIA-RICH EMBEDDED SYSTEMS

CHAIR: Sujit Dey - *Univ. of California, San Diego, La Jolla, CA*

ORGANIZER: Sujit Dey

Real-time, multimedia applications promise to be strong drivers for mobile, battery-constrained embedded systems. However, these applications are highly computation intensive, and thereby energy demanding. This session offers energy modeling and optimization techniques for several real-time and multimedia systems, including MPEG decoding, video-array based tracking systems, watermarking for image transmission, and fault-tolerant real-time systems.

§33.1 Off-Chip Latency-Driven Dynamic Voltage and Frequency Scaling for an MPEG Decoding

Kihwan Choi, Ramakrishna Soma, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

33.2 Energy-Aware Deterministic Fault Tolerance in Distributed Real-Time Systems

Ying Zhang - *Duke Univ., Durham, NC*
Robert Dick - *Northwestern Univ., Evanston, IL*
Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

33.3 Proxy-Based Task Partitioning of Watermarking Algorithms for Reducing Energy Consumption in Mobile Devices

Arun Kejariwal, Sumit Gupta, Alexandru Nicolau, Nikil Dutt - *Univ. of California, Irvine, CA*
Rajesh Gupta - *Univ. of California, San Diego, La Jolla, CA*

33.4s Power-Aware Adaptive Data Partitioning for Ambeint Multimedia

Xiaoping Hu, Radu Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

33.5s Energy Characterization of Filesystems for Diskless Embedded Systems

Siddharth Choudhuri - *Univ. of California, Irvine, CA*
Rabi Mahapatra - *Texas A&M Univ., College Station, TX*

Session 34 — Tools — Rm: 6D

LATENCY TOLERANCE AND ASYNCHRONOUS DESIGN

CHAIR: Marios Papaefthymiou - *Univ. of Michigan, Ann Arbor, MI*

ORGANIZERS: James C. Hoe, Leon Stok

This session presents five papers in the areas of latency tolerance and asynchronous design. The first paper describes a technique to automatically correct the functionality of wire-pipelined circuits. The second paper describes an approach to minimize the latency management overhead in statically schedulable designs. The third paper proposes approaches to estimate wire length and congestion during logic synthesis. The fourth paper presents optimizations to asynchronous logic synthesis by "de-synchronization". The final paper presents a fast algorithm for hazard detection in combinational circuits.

§34.1 A Method for Correcting the Functionality of a Wire-Pipelined Circuit

Vidyasagar Nookala, Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

34.2 A New Approach to Latency Insensitive Design

Luca Macchiarulo, Mario R. Casu - *Politecnico di Torino, Torino, Italy*

34.3 Pre-Layout Wire Length and Congestion Estimation

Qinghua Liu, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

34.4s The Best of Both Worlds: The Efficient Asynchronous Implementation of Synchronous Specifications

Abhijit Davare - *Univ. of California, Berkeley, CA*
Kelvin Lwin - *Cadence Design Systems, Inc., San Jose, CA*
Alex Kondratyev - *Cadence Berkeley Labs., Berkeley, CA*
Alberto L. Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

34.5s Fast Hazard Detection in Combinational Circuits

Cheoljoo Jeong, Steven M. Nowick - *Columbia Univ., New York, NY*

Session 35 — Methods/Tools — Rm: 4

NEW TECHNOLOGIES IN SYSTEM DESIGN

CHAIR: Petru Eles - *Linkoping Univ., Linkoping, Sweden*

ORGANIZERS: Ahmed A. Jerraya, Gila Kamhi

This session covers a broad set of ideas in system design, ranging from nanotechnologies to bus usage analysis. The first paper presents strategies for successful design given the anticipated high-defect rate of future nanotechnologies. The next three papers tackle the challenges of architectural synthesis from both the design and verification viewpoints. The last paper provides throughput and power dissipation analysis of AMBA AHB bus usage.

35.1 Defect Tolerant Probabilistic Design Paradigm for Nanotechnologies

Margarida Jacome, Chen He - *Univ. of Texas, Austin, TX*
Gustavo deVeciana, Steve Bijansky - *Univ. of Texas, Austin, TX*

35.2 Architecture-Level Synthesis for Automatic Interconnect Pipelining

Jason Cong, Yiping Fan, Zhiru Zhang - *Univ. of California, Los Angeles, CA*

35.3 Automatic Generation of Equivalent Architecture Model from Functional Specification

Samar Abdi, Daniel Gajski - *Univ. of California, Irvine, CA*

35.4s Divide-and-Concatenate: An Architecture Level Optimization Technique for Universal Hash Functions

Bo Yang, Ramesh Karri - *Polytechnic Univ., Brooklyn, NY*
David A. Mcgrew - *Cisco Systems, Inc., San Jose, CA*

35.5s Performance Analysis of Different Arbitration Algorithms of the AMBA AHB Bus

Massimo Conti, Marco Caldari, Simone Orcioni, Claudio Turchetti, Giovanni B. Vece - *Univ. Politecnica delle Marche, Ancona, Italy*

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Session 36 — Methods/Tools — Rm: 6A

SPECIAL SESSION: BIOMEMS

CHAIR: Andrew B. Kahng - *Univ. of California, San Diego, La Jolla, CA*
ORGANIZER: Jacob K. White

The variety of applications for BioMEMS and the potential volumes involved has started to influence CAD development. Because almost all products are created by physical prototyping and have huge times-to-market, there is a substantial opportunity for address new CAD challenges: developing hierarchy, topology synthesis, shape optimization and layout, circuit simulation, and more.

36.1 Design Tools for BioMEMS
Tom Korsmeyer, Jun Zeng, Ken Greiner - *Coventor, Inc., Cambridge, MA*

36.2 Atomistic and Multiscale Techniques for Bio-Nano Devices
Narayan Aluru - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

36.3 CAD Challenges in BioMEMS Design
Jacob White - *Massachusetts Institute of Tech., Cambridge, MA*

Session 37 — Methods/Tools — Rm: 6B

PANEL: WILL MOORE'S LAW RULE IN THE LAND OF ANALOG?

CHAIR: Rob A. Rutenbar - *Carnegie Mellon Univ., Pittsburgh, PA*
ORGANIZER: Rob A. Rutenbar

Once upon a time there was a wise and benevolent ruler whose Law multiplied his subjects' wealth and happiness—about 2X, every couple of years. But the kingdom was divided. Those in the happy hamlet of Digital got fatter (and faster), year after year. Not so the talented artisans in the town of Analog complained constantly about "voltage headroom", "variability", "noise", "matching", "kT/C limits", the rising costs of supporting their neighbors' insatiable addiction to shrinking transistors, and how the grass looked greener just over the border, in Silicon-Germania. So, what's a King to do? Will we see billion-transistor chips with integrated RF made from transistors that are 25 atoms wide? Or will the peasants in the land of Analog really revolt?

Panelists:
Teresa Meng - *Stanford Univ./Atheros, Stanford, CA*
Charlie Sodini - *Massachusetts Institute of Tech., Cambridge, MA*
Jim Wieser - *National Semiconductor Corp., Santa Clara, CA*
Robert Pitts - *Texas Instruments, Inc., Dallas, TX*
Ernesto Perea - *STMicroelectronics, Crolles, France*
Tony Bonaccio - *IBM Corp., Essex Junction, VT*

Session 38 — Tools — Rm: 6C

FLOORPLANNING

CHAIR: Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*
ORGANIZERS: Chung-Kuan Cheng, Frank M. Johannes

The session advocates floorplanning for architecture-level and layout optimization. In the first paper, a microarchitectural floorplanner is presented that considers both the impacts of wire delay and architectural behavior. The second paper increases instructions per cycle using a trajectory piece-wise linear model. A representation to tackle the floorplanning of triangular objects that achieves efficient area utilization is introduced in the third paper.

38.1 Profile-Guided Microarchitectural Floorplanning for Deep Submicron Processor Design

Mongkol Ekpanyapong, Jacob R. Minz - *Georgia Institute of Tech., Atlanta, GA*
Thaisiri Watewai - *Univ. of California, Berkeley, CA,*
Hsien-Hsin S. Lee, Sung Kyu Lim - *Georgia Institute of Tech., Atlanta, GA*

38.2 Floorplanning Optimization with Trajectory Piecewise-Linear Model for Pipelined Interconnects

Changbo Long, Lucanus J. Simonson, Weiping Liao, Lei He - *Univ. of California, Los Angeles, CA*

38.3 A Packing Algorithm for Non-Manhattan Hexagon/Triangle Placement by Using an Adaptive O-Tree Representation

Jing Li, Bo Yang, Tan Yan, Juebang Yu - *Univ. of Electronic Sci. & Tech. of China, Chengdu, China*
Chunghui Li - *Cadence Design Systems, Inc., San Jose, CA*

Session 39 — Tools — Rm: 6D

ISSUES IN TIMING ANALYSIS

CHAIR: David Hathaway - *IBM Corp., Essex Junction, VT*
ORGANIZERS: Kenneth L. Shepard, Sudhakar Bobba

This session considers several issues in the static timing analysis of digital integrated circuits. In the first paper, the effect of power supply variations on timing is analyzed. The second paper offers a statistical gate delay model that considers the effects of multiple input switching. The final paper in this session proposes a new timing analysis algorithm using a two-pass traversal of the timing graph.

39.1 Worst-Case Circuit Delay Taking Into Account Power Supply Variations

Dionysios Kouroussis, Rubil Ahmadi, Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*

39.2 Statistical Gate Delay Model Considering Multiple Input Switching

Aseem B. Agarwal - *Univ. of Michigan, Ann Arbor, MI*
Florentin Dartu - *Intel Corp., Hillsboro, OR*
David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

39.3 Static Timing Analysis using Backward Signal Propagation

Dongwoo Lee - *Univ. of Michigan, Ann Arbor, MI*
Vladimir Zolotov - *Motorola, Inc., Austin, TX*
David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

Session 40 — Methods/Tools — Rm: 4

SPECIAL SESSION: ISSCC HIGHLIGHTS

CHAIR: Grant E. Martin - *Tensilica, Inc., Santa Clara, CA*
ORGANIZER: Grant E. Martin

40.1 Design and Implementation of the POWER5 Microprocessor

Joachim Clabes, Joshua Friedrich - *IBM Corp., Austin, TX*

40.2 A Dual Core 64b UltraSPARC Microprocessor for Dense Server Applications

Toshinari Takayanagi, Joachim Clabes, Jinuk Luke Shin, Bruce Petrick - Sun Microsystems, Inc., *Sunnyvale, CA*
Jeffrey Su - Sun Microsystems, Inc., *Austin, TX*
Ana Sonia Leon - Sun Microsystems, Inc., *Sunnyvale, CA*

40.3 Low-Voltage-Swing Logic Circuits for a Pentium® 4Processor Integer Core

Daniel Deleganes - *Intel Corp., Hillsboro, OR*

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Thursday
June 10
10:30
to
12:00

All speakers are denoted in **bold**

S – denotes short paper

ß – denotes best paper candidates

session topic area given on page 12

Business Sessions shaded blue

Session 41 — Methods/Tools — Rm: 6A

SPECIAL SESSION: MULTIPROCESSOR SOC MPSOC SOLUTIONS/NIGHTMARE

CHAIR: Grant E. Martin - *Tensilica, Inc., Santa Clara, CA*
ORGANIZER: Grant E. Martin

What ? (Topic) - Multi-processor System-on-Chip is the future of SoC and indeed of much of IC Design. A network of heterogeneous processors - RISCs, DSPs, ASIPs, and dedicated function blocks - interconnected by a Network-on-Chip (NoC) fabric seems destined to be a key architecture for MPSoC. However, we are a long, long way from knowing how to effectively design MPSoC and obtaining the right tools, methods and approaches. This Special session will first give an overview of MPSoC and key design problems and then have a couple of talks outlining some potential solutions.

Why ? (Motivation, Importance, Interest) - SoCs are already "MP" if we take the now classical RISC+DSP combination used in many handsets and consumer products. We currently lack effective means and tools to design even this simple combination, so the issues of how to map complex applications to MPSoC with 4, 10 or many 10's of processors is a daunting one. However, leading researchers and companies are beginning to identify solutions to key parts of this puzzle, and this special session will educate designers on what is possible and what will come.

41.1 The Future of Multiprocessor Systems-on-Chips
Wayne Wolf - *Princeton Univ., Princeton, NJ*

41.2 Heterogeneous MPSoC—The Solution to Energy-Efficient Signal Processing
Heinrich Meyr - *Aachen Univ. of Tech., Aachen, Germany*

41.3 Flexible Architectures for Engineering Successful MPSoCs
Steve Leibson - *Tensilica, Inc., Santa Clara, CA*

Session 42 — Methods/Tools — Rm: 6B

PANEL: IS STATISTICAL TIMING STATISTICALLY SIGNIFICANT?

CHAIR: Andrew B. Kahng - *Univ. of California, San Diego, La Jolla, CA*
ORGANIZERS: Rich Goldman, Kurt Keutzer

Process variations that affect critical electrical parameters leading to changes in circuit performance have always posed significant challenges to semiconductor design. In the past, in-die process variation was relatively small, and methods such as corner-based analysis were sufficient. This allowed timing analysis tools to calculate delays and slews in a straightforward way. As statistical variation increases, will corner-casing lead to too much conservatism, or are the advantages of statistical timing analysis overstated?

Panelists:
Chandu Visweswariah - *IBM Corp., Yorktown Heights, NY*
Ahsan Bootehsaz - *Synopsys, Inc., Mountain View, CA*
Ed Chen - *TSMC, Hsin-Chu, Taiwan*
Clive Bittlestone - *Texas Instruments, Inc., Dallas, TX*
Lou Scheffer - *Cadence Design Systems, Inc., San Jose, CA*
Shekhar Y. Borkar - *Intel Corp., Hillsboro, OR*

Session 43 — Methods/Tools — Rm: 6C

TIMING ISSUES IN PLACEMENT

CHAIR: Bill Halpin - *Intel Corp., Santa Clara, CA*

ORGANIZERS: Carl Sechen, Phiroze Parakh

This session presents algorithmic improvements in performance-driven physical synthesis. This includes buffering and logic replication, as well as a new timing-driven placement algorithm.

43.1 Modeling Repeaters Explicitly Within Analytical Placement

Prashant Saxena - *Intel Corp., Hillsboro, OR*
Bill Halpin - *Synplicity, Inc., Sunnyvale, CA*

43.2 Quadratic Placement Using an Improved Timing Model

Bernd Obermeier, Frank M. Johannes - *Technical Univ. of Munich, Munich, Germany*

43.3 An Approach to Placement-Coupled Logic Replication

Milos Hrkic, John Lillis, Giancarlo Beraudo - *Univ. of Illinois, Chicago, IL*

Session 44 — Methods — Rm: 6D

DESIGN METHODOLOGIES FOR ASIPS

CHAIR: Masaharu Imai - *Osaka Univ., Toyonaka, Japan*

ORGANIZERS: Joachim Gerlach, Margarida Jacome

Application Specific Instruction Set Processors (ASIPs) offer a good trade-off between flexibility, performance and energy efficiency. However, their effectiveness relies on the ability to properly customize processors to target classes of embedded applications and create the corresponding development environments, in reasonable time. The first paper enhances a well-known architecture description language so that compilers and instruction set simulators can all be generated from a single, consistent model. The second and third papers explore several aspects of extending a processor's instruction set, including mechanisms for instruction set selection and inclusion of local memory elements.

44.1 A Novel Approach for Flexible and Consistent ADL-Driven ASIP Design

Gunnar Braun - *CoWare, Inc., Aachen, Germany*
Weihua Sheng - *Institute for Integrated Systems, Aachen, Germany*
Achim Nohl - *CoWare, Inc., Aachen, Germany,*
Jianjiang Ceng, Manuel Hohenauer, Hanno Scharwaechter, Rainer Leupers, Heinrich Meyr - *Institute for Integrated Systems, Aachen, Germany*

44.2 Characterizing Embedded Applications for Instruction-Set Extensible Processors

Pan Yu, Tulika Mitra - *National Univ. of Singapore, Singapore, Singapore*

44.3 Introduction of Local Memory Elements in Instruction Set Extensions

Partha Biswas - *Univ. of California, Irvine, CA*
Vinay Choudhary, Kubilay Atasu, Laura Pozzi, Paolo Ienne - *Swiss Federal Institute of Technology, Lausanne, Switzerland*
Nikil Dutt - *Univ. of California, Irvine, CA*

Session 45 — Methods — Rm: 4

FPGA-BASED SYSTEMS

CHAIR: Katherine Compton - *Univ. of Wisconsin, Madison, WI*

ORGANIZERS: Jens Palsberg, Scott Hauck

The heterogeneity of newer FPGAs is driving new classes of systems, and corresponding problems, for the FPGA CAD designer. With multiple resources, traditional algorithms such as partitioning must be reformulated to deal with these constraints. Power minimization is also crucial, forcing changes in architecture and algorithms. These new architectures give rise to new uses, such as mixed-mode simulators.

45.1 FPGA Power Reduction Using Configurable Dual-Vdd

Fei Li, Yan Lin, Lei He - *Univ. of California, Los Angeles, CA*

45.2 Multi-Resource Aware Partitioning Algorithms for FPGAs with Heterogeneous Resources

Navaratnasothie Selvakkumaran - *Univ. of Minnesota, Minneapolis, MN*
Abishek Ranjan, Salil Raje - *Hier Design Inc., Santa Clara, CA*
George Karypis - *Univ. of Minnesota, Minneapolis, MN*

45.3 An SoC Design Methodology Using FPGA and Embedded Microprocessors

Nobuyuki Ohba - *IBM Corp., Sendai, Japan*
Kohji Takano - *IBM Corp., Yamato, Japan*

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Session 46 — Methods/Tools — Rm: 6A

SPECIAL SESSION: SECURITY AS A NEW DIMENSION IN EMBEDDED SYSTEM DESIGN

CHAIR: Srivaths Ravi - *NEC Corp., Princeton, NJ*
ORGANIZER: Srivaths Ravi

The growing number of instances of breaches in information security in the last few years has created a compelling case for efforts towards secure electronic systems. Embedded systems, which will be ubiquitously used to capture, store, manipulate, and access data of a sensitive nature, pose several unique and interesting security challenges. This special session is intended to introduce the challenges involved in designing secure embedded systems to embedded system designers and design tool developers. The session will provide a unified and holistic view of embedded system security: "Security is often mis-construed by designers as the hardware or software implementation of specific cryptographic algorithms and security protocols. Whereas in reality it is an entirely new metric that designers should consider throughout the design process, along with other metrics such as cost, performance, power, etc." Speakers will provide a clear introduction of typical functional security requirements for embedded systems from an end-user perspective. They will identify the implied challenges for embedded system architects, as well as hardware and software designers (e.g., tamper-resistant embedded system design, processing requirements for security, impact of security on battery life for battery-powered systems, etc). Speakers will also provide an overview of solution techniques to address these challenges, drawing from both current practice and emerging research, and identify open research problems that will require innovations in embedded system architecture and design methodologies.

46.1 Security Challenges In Embedded System Design
Anand Raghunathan - *NEC Corp., Princeton, NJ*

46.2 Exploiting Embedded Software
Gary McGraw - *Cigital, Inc., Dulles, VA*

46.3 Processor Architectures for Efficient Secure Information Processing
Ruby Lee - *Princeton Univ., Princeton, NJ*

46.4 Attacks and Countermeasures for Tamper-Resistant Embedded Hardware Devices
Paul Kocher - *Cryptography Research, Inc., San Francisco, CA*

Session 47 — Methods/Tools — Rm: 6B

LEAKAGE POWER OPTIMIZATION

CHAIR: Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*
ORGANIZERS: Enrico Macii, Naehyuck Chang

This session presents different approaches for reducing leakage power consumption in deep submicron CMOS circuits. The papers investigate different trade-offs between gate Tox, Vdd, Vth and sizing. Also, techniques for deriving input vector control and encoding schemes for simultaneous crosstalk and leakage power reduction on buses are described.

47.1 Tradeoffs between Gate Oxide Leakage and Delay for Dual Tox Circuits
Anup Kumar Sultania - *Univ. of Minnesota, Minneapolis, MN*
Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*
Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

47.2 Implicit Pseudo Boolean Enumeration Algorithms for Input Vector Control
Kaviraj S. Chopra, Sarma Vrudhula - *Univ. of Arizona, Tucson, AZ*

47.3 Statistical Optimization of Leakage Power Considering Process Variations Using Dual-Vth and Sizing
Ashish Srivastava, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

47.4s Leakage – and Crosstalk-Aware Bus Encoding for Total Power Reduction
Harmander S. Deogun, Rajeev R. Rao, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

47.5s Power Minimization Using Simultaneous Gate Sizing, Dual-Vdd, and Dual-Vth Assignment
Ashish Srivastava, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

Session 48 — Methods/Tools — Rm: 6C

INTERCONNECT EXTRACTION

CHAIR: Yehea Massoud - *Rice Univ., Houston, TX*
ORGANIZERS: Sachin S. Sapatnekar, Jamil Kawa

This session presents new developments in the area of 3D parasitic extraction. The first paper describes capacitance extraction under multi-dielectric environments. Next, a parasitic extractor for microelectronics, multichip modules and MEMS, which combines the fast multiple method with QR matrix compression is presented. The third paper shows a method for determining inductive noise coupling. A full wave field solver for RF, analog and high-speed digital circuits is presented next. Finally, a presentation on a technique that develops closed-form expressions for distributed RC interconnects rounds out the session.

48.1 Sparse Transformations and Preconditioners for Hierarchical 3-D Capacitance Extraction with Multiple Dielectrics
Shu Yan, Vivek Sarin, Weiping Shi - *Texas A&M Univ., College Station, TX*

48.2 A Fast Parasitic Extractor Based on Low Rank Multilevel Matrix Compression for Conductor and Dielectric Modeling in Microelectronics and MEMS
Dipanjan Gope, Swagato Chakraborty, Vikram Jandhyala - *Univ. of Washington, Seattle, WA*

48.3 CHIME: Coupled Hierarchical Inductance Model Evaluation
Satrajit Gupta, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

48.4s Large-Scale Full-Wave Simulation
Sharad Kapur, David E. Long - *Integrand Software, Inc., Hoboken, NJ*

48.5s Closed-Form Expressions of Distributed RLC Interconnects for Analysis of On-Chip Inductance Effects
Yuichi Tanji - *Kagawa Univ., Takamatsu, Japan*
Hideki Asai - *Shizuoka Univ., Hamamatsu, Japan*

Session 49 — Tools — Rm: 6D

NEW FRONTIERS IN LOGIC SYNTHESIS

CHAIR: Jordi Cortadella - *Univ. Polytechnica De Catalunya, Barcelona, Spain*
ORGANIZERS: Leon Stok, Steven M. Nowick

The first paper presents a novel approach to delay variation tolerance through "voting structures". The second paper optimizes domino circuits by eliminating the need for full logic duplication. Multiplication by constants is an important problem in DSPs, and the third paper proposes a new DAG fusion approach for sharing adders. The fourth paper describes simple heuristics for decomposing asynchronous controller specifications. The last two papers extend synthesis into the quantum domain.

49.1 Re-Synthesis for Delay Variation Tolerance
Shih-Chieh Chang, Cheng-Tao Hsieh, Kai-Chiang Wu - *National Tsing-Hua Univ., Hsinchu, Taiwan*

49.2 Post-Layout Logic Optimization of Domino Circuits
Aiqun Cao, Cheng-Kok Koh - *Purdue Univ., West Lafayette, IN*

49.3s Multiple Constant Multiplication by Time-Multiplexed Mapping of Addition Chains
Peter Tummeltshammer - *Univ. of Technology Vienna, Vienna, Austria*
James C. Hoe, Markus Pueschel - *Carnegie Mellon Univ., Pittsburgh, PA*

49.4s Decomposing Specifications with Concurrent Outputs to Resolve State Coding Conflicts in Asynchronous Logic Synthesis
Hemangee K. Kapoor, Mark B. Josephs - *London South Bank Univ., London, United Kingdom*

49.5s A New Heuristic Algorithm for Reversible Logic Synthesis
Pawel Kerntopf - *Warsaw Univ. of Tech., Warsaw, Poland*

49.6s Quantum Logic Synthesis by Symbolic Reachability Analysis
William N. N. Hung - *Intel Corp., Hillsboro, OR*
Xiaoyu Song, Guowu Yang - *Portland State Univ., Portland, OR*
Jin Yang - *Intel Corp., Hillsboro, OR*
Marek Perkowski - *Portland State Univ., Portland, OR*

Session 50 — Methods/Tools — Rm: 4

NUMERICAL TECHNIQUES FOR SIMULATION

CHAIR: Joel R. Phillips - *Cadence Design Systems, Inc., San Jose, CA*
ORGANIZERS: Jacob K. White, Kartikeya Mayaram

The five papers in this session on numerical techniques address a variety of issues in simulation and analysis of analog, mixed signal, and RF circuits. The first two and last two papers describe techniques for improving circuit simulation and analysis, and the third paper addresses the problem of predicting substrate noise.

50.1 A Frequency Relaxation Approach for Analog/RF System-Level Simulation
Xin Li, Yang Xu, Peng Li, Padmini Gopalakrishnan, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

50.2 Robust, Stable Time-Domain Methods for Solving Nonlinear MPDEs of Fast/Slow System
Ting Mei, Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*
Todd S. Coffey, Scott A. Hutchinson, David M. Day - *Sandia National Labs., Albuquerque, NM*

50.3 High-Level Simulation of Substrate Noise in High-Ohmic Substrates with Interconnect and Supply Effects
Geert Van der Plas, Mustafa Badaroglu, Gerd Vandersteen, Petr Dobrovolny, Piet Wambacq, Stephane Donnay - *IMEC, Leuven, Belgium*
Georges Gielen - *Katholieke Univ. , Leuven , Belgium*
Hugo De Man - *IMEC, Leuven, Belgium*

50.4s Hierarchical Approach to Exact Symbolic Analysis of Large Analog Circuits
Sheldon Tan, Weikun Guo, Zhenyu Qi - *Univ. of California, Riverside, CA*

50.5s An Essentially Non-Oscillatory High-Order Accurate Adaptive Table Model Using Efficient Transfinite Blending Function and Dynamic Construction
Baolin Yang, Bruce MacGaughy - *Cadence Design Systems, Inc., San Jose, CA*

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Session 51 — Methods — Rm: 6A

ENERGY AND THERMAL-AWARE DESIGN

CHAIR: Jihong Kim - *Seoul National Univ., Seoul, Republic of Korea*
ORGANIZERS: Chaitali Chakrabarti, Sarma B. Vrudhula

This session covers two different aspects of energy minimization in electronic systems. The first two papers investigate the limits of DVS scaling and the applicability of DVS to gate arrays. The last two papers deal with thermal modeling and the effects of temperature on Vdd and Vth.

51.1 Theoretical and Practical Limits of Dynamic Voltage Scaling

Bo Zhai, David Blaauw, Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*
Krisztian Flautner - *ARM Ltd., Cambridge, United Kingdom*

51.2s Enabling Energy Efficiency in Via-Patterned Gate Array Devices

Reed Taylor - *Carnegie Mellon Univ., Pittsburgh, PA*
Herman Schmit - *Tabula, Inc., Mountain View, CA*

51.3 Compact Thermal Modeling for Temperature-Aware Design

Wei Huang, Mircea R. Stan, Kevin Skadron, Karthik Sankaranarayanan, Shougata Ghosh, Sivakumar Velusamy - *Univ. of Virginia, Charlottesville, VA*

51.4s Simultaneous Optimization of Supply and Threshold Voltage for Low-Power and High-Performance Circuits in the Leakage Dominant Era

Anirban Basu, Sheng-Chih Lin - *Univ. of California, Santa Barbara, CA*
Amit Mehrotra - *Berkeley Design Automation, Inc., Santa Clara, CA*
Kaustav Banerjee - *Univ. of California, Santa Barbara, CA*

Session 52 — Methods/Tools — Rm: 6B

NOISE-TOLERANT DESIGN AND ANALYSIS TECHNIQUES

CHAIR: David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
ORGANIZERS: Anirudh Devgan, Dennis Sylvester

This session deals with various sources of noise, both traditional and non-traditional, and describes both analysis and design techniques to address them. The first paper proposes macromodels to capture the response of CMOS logic gates to input noise waveforms while the second work looks at multiple sources of noise in a circuit, including soft errors, to find noise-sensitive nodes. The third paper proposes a unique keeper structure in dynamic logic to boost noise immunity. The last work studies different approaches to global interconnect pipelining under process fluctuations, which can be viewed as another source of noise.

52.1 Noise Characterization of Static CMOS Gates

Rouwaida N. Kanj - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*
Timothy Lehner, Bhavna Agrawal - *IBM Corp., Hopewell Junction, NY*
Elyse Rosenbaum - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

52.2 A Scalable Soft Spot Analysis Methodology for Compound Noise Effects in Nano-Meter Circuits

Chong Zhao, Xiaoliang Bai, Sujit Dey - *Univ. of California, San Diego, La Jolla, CA*

52.3s A Novel Technique to Improve Noise Immunity of CMOS Dynamic Logic Circuits

Li Ding, **Pinaki Mazumder** - *Univ. of Michigan, Ann Arbor, MI*

52.4s Statistical Timing Analysis in Sequential Circuit for On-Chip Global Interconnect Pipelining

Lizheng Zhang, Yuhen Hu - *Univ. of Wisconsin, Madison, WI*
Charlie Chung-Ping Chen - *National Taiwan Univ., Taipei, Taiwan*

Session 53 Methods/Tools Rm: 6C

NEW TOOLS AND METHODS FOR FUTURE EMBEDDED SOC

CHAIR: Giovanni De Micheli - *Stanford Univ., Stanford, CA*

ORGANIZERS: Marcello Coppola, Pai H. Chou

This session illustrates the wide range and variety of design tools and methodologies for future embedded systems. The first paper is unique in reporting actual measured design process results and pitfalls for a video encoder case study. The second paper reports on an innovative new tool which automates large parts of Network-on-Chip design. This is followed by two short papers, one of which looks again at the whole concept of RISC to generate extreme application oriented processors. The final paper addresses the use of domain specific languages as a new entry point for embedded design through the use of a networking application.

53.1 Debugging HW/SW Interface for MPSoC: Video Encoder System Design Case Study

Mohamed-Wassim Youssef, Sungjoo Yoo, Arif Sasongko, Yanick Paviot, Ahmed A. Jerraya - *TIMA Lab., Grenoble, France*

53.2 SUNMAP: A Tool for Automatic Topology Selection and Generation for NoCs

Srinivasan Murali, Giovanni De Micheli - *Stanford Univ., Stanford, CA*

53.3s FITS: Framework-based Instruction-Set Tuning Synthesis for Embedded Application Specific Processors

Allen Cheng - *Univ. of Michigan, Ann Arbor, MI*
Gary Tyson - *Florida State Univ., Tallahassee, FL*
Trevor Mudge - *Univ. of Michigan, Ann Arbor, MI*

53.4s Mapping a Domain Specific Language to a Platform FPGA

Chidamber Kulkarni, Gordon Brebner - *Xilinx, Inc., San Jose, CA*
Graham Schelle - *Univ. of Colorado, Boulder, CO*

Session 54 Methods/Tools Rm: 6D

NEW SCAN-BASED TEST TECHNIQUES

CHAIR: Bernd Koenemann - *Cadence Design Systems, Inc., San Jose, CA*

ORGANIZERS: Erik Jan Marinissen, Seiji Kajihara

All papers in this session give new solutions on scan-based testing.The first paper considers generating tests for scan circuits that ensure that the test only uses functionally reachable states. This is done in order to avoid reducing yield caused by tests that operate the circuits in non-functional mode. The other two papers describe new architectures for scan-based BIST which will target flexible features and simple implementation, respectively. The last paper presents a test compression method for multiple scan design.

54.1 On the Generation of Scan-Based Test Sets with Reachable States for Testing under Functional Operation Conditions

Irith Pomeranz - *Purdue Univ., West Lafayette, IN*

54.2 Scalable Selector Architecture for X-Tolerant Deterministic BIST

Peter Wohl - *Synopsys, Inc., Williston, VT*
John A. Waicukauski - *Synopsys, Inc., Tualatin, OR*
Sanjay Patel - *Synopsys, Inc., Beaverton, OR*

54.3s Scan-BIST Based on Transition Probabilities

Irith Pomeranz - *Purdue Univ., West Lafayette, IN*

54.4s Combining Dictionary Coding and LFSR Reseeding for Test Data Compression

Xiaoyun Sun, Larry Kinney, Bapiraju Vinnakota - *Univ. of Minnesota, Minneapolis, MN*

Session 55 Methods/Tools Rm: 4

CAD FOR RECONFIGURABLE COMPUTING

CHAIR: Jason Cong - *Magma Design Automation, Inc., Los Angeles, CA*

ORGANIZERS: Jens Palsberg, Scott Hauck

By combining the fast reconfiguration of microprocessors with the high-performance of hardware, FPGAs open up new challenges to the CAD designer. This session considers fast algorithms for reconfigurable computing as well as operating systems support for such systems.

55.1 Virtual Memory Window for Application-Specific Reconfigurable Coprocessors

Miljan Vuletic, Laura Pozzi, Paolo Ienne - *Swiss Federal Institute of Tech., Lausanne, Switzerland*

55.2 Dynamic FPGA Routing for Just-in-Time FPGA Compilation

Roman Lysecky, Frank Vahid, Sheldon X.-D. Tan - *Univ. of California, Riverside, CA*

55.3 An Efficient Algorithm for Finding Empty Space for Online FPGA Placement

Manish Handa, Ranga Vemuri - *Univ. of Cincinnati, Cincinnati, OH*

Tutorials

Monday, June 7 • 9:00 AM - 5:00 PM

TUTORIAL 1 - GETTING YOUR "COOL ASIC" UP TO SPEED: PRACTICAL TECHNIQUES AND TOOLS TO ACHIEVE CUSTOM LIKE PERFORMANCE IN A POWER-AWARE DESIGN FLOW

Rm: 6C

ORGANIZER: Ruchir Puri - *IBM Corp., Yorktown Heights, NY*
PRESENTERS: Stephen Kosonocky - *IBM Corp., Yorktown Heights, NY*
Ruchir Puri - *IBM Corp., Yorktown Heights, NY*
Leon Stok - *IBM Corp., Yorktown Heights, NY*
Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*

GHz frequencies are a common feature among leading edge microprocessors while ASIC designs are still hovering at the several hundred MHz range. Most of the custom design benefits come from architectural tradeoffs, use of a fabrication process with faster devices, advanced circuit families, structured logic, and flexibility to tune individual transistors. However, it is difficult to utilize some of these custom techniques in ASIC designs due to lower cost, and often lower-power constraints. For example, due to heavy emphasis on lowering cost, ASIC designs usually cannot exploit high-performance fabrication processes due to their significantly lower yields. Similarly, advanced circuit techniques such as dynamic logic are not very beneficial in ASIC designs due to their higher power dissipation and clocking overhead. In the absence of these custom techniques, how can a designer get his ASIC anywhere close to speeds achieved by custom designs while still keeping it cool? In this tutorial, we will answer this question by presenting practical techniques and tools that complement a standard ASIC flow in order to achieve performance and power improvements. This tutorial will span a breadth of techniques addressing technology, circuit and methodology issues. The topics will include: theory of power-performance trade-off with gate sizing, multiple-threshold and multiple-oxide cells, leakage vs dynamic power trade-off, advanced circuit design techniques to achieve lower power, logic/physical synthesis and methodology issues in a power-aware, high-performance design flow.

Friday, June 11 • 9:00 AM - 5:00 PM

TUTORIAL 2 - AUTOMATED MACROMODELLING TECHNIQUES FOR DESIGN OF COMPLEX ANALOG, MIXED-SIGNAL INTEGRATED SYSTEMS

Rm: 1AB

ORGANIZER: Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*
PRESENTERS: Georges G. Gielen - *Katholieke Univ., Leuven, Belgium*
Joel Phillips - *Cadence Design Systems, Inc., San Jose, CA*
Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*
Rob A. Rutenbar - *Carnegie Mellon Univ., Pittsburgh, PA*
Juan-Antonio Carballo - *IBM Corp., Austin, TX*

The use of simplified macromodels for analog circuits, both to accelerate simulation and to enhance early design exploration, has a long history in analog and mixed-signal design. Traditionally, macromodel construction has relied on design expertise to create suitably simplified circuit models. With the anticipation of complex multi-standard communication systems, semiconductor process feature sizes below 100nm, and single-chip systems integrating mixed-signal, RF, analog and digital functionalities, manual macromodeling approaches are beginning to constitute a significant design and verification bottleneck. In recent years, there has been a surge of activity in automated approaches to macromodeling that aim to address this bottleneck. There is growing consensus that such automated macromodeling approaches will be essential for realistic design space exploration and verification in current and future mixed-signal SoCs/SiPs. In this tutorial, we will provide a detailed overview of state-of-the-art methods for automated macromodeling, and outline their use in applications. Starting with an introduction to the macromodeling landscape and a review of manual macromodeling, we will proceed to cover several hot macromodeling-related topics in CAD.

Tutorials

Friday, June 11 • 9:00 AM - 5:00 PM

TUTORIAL 3 - BUFFERING INTERCONNECT: FROM BASICS TO BREAKTHROUGHS

Rm: 6B

ORGANIZER: Weiping Shi - *Texas A&M Univ., College Station, TX*
PRESENTERS: Charles J. Alpert - *IBM Corp., Austin, TX*
Jiang Hu - *Texas A&M Univ., College Station, TX*
Noel Menezes - *Intel Corp., Hillsboro, OR*
Weiping Shi - *Texas A&M Univ., College Station, TX*

With each CMOS technology node, the optimum distance between buffers continues to decrease dramatically. This buffer explosion requires design methodologies to quickly adapt. This tutorial addresses the buffering problems, issues, algorithms, and flows related to deep sub-micron effects of scaling. We focus on fast, practical techniques that can be embedded into industry physical synthesis flows.

The tutorial reviews CMOS technology scaling principles, buffering formulae, and delay and noise models that show that the number of buffers required to achieve timing closure and fix electrical violations is increasing dramatically. We present van Ginneken's classic algorithm and show how to extend it to handle a variety of practical constraints: multiple buffer types, signal polarity, area resource control, slew, capacitance, and noise. We describe techniques for constructing timing-driven, buffer-aware routes that are required to effectively drive these buffer insertion algorithms.

Inserting buffers while ignoring the layout is a recipe for disaster. We discuss buffering techniques for avoiding blockages, managing design density, and handling routing congestion. We discuss methodology issues related to both ASIC and high-performance microprocessors, including inductance for busses, hierarchy management, and flip-flop insertion. Finally, we discuss future fundamental buffering problems such as planning, place and route-flows, and integration into physical synthesis.

Friday, June 11 • 9:00 AM - 5:00 PM

TUTORIAL 4 - LINUX FOR REAL-TIME AND EMBEDDED SYSTEMS

Rm: 4

ORGANIZER: Marco Di Natale - *ReTis Lab. Scuola Superiore S. Anna, Pisa, Italy*
PRESENTERS: Ragunathan Rajkumar - *TimeSys Corp./Carnegie Mellon Univ., Pittsburgh, PA*
Edgar F. Hilton - *FSMLabs., Inc., Tallahassee, FL*
Kevin Morgan - *MontaVista Software, Sunnyvale, CA*
Giuseppe Lipari - *Scuola S. Anna, Pisa, Italy*

Embedded developers are designing and deploying Linux-based systems in an ever-increasing range of applications. Device OEMs increasingly choose Linux as a strategic platform, and Linux must be able to target multiple application types, diverse CPU architectures, varying board form-factors, special-purpose interconnects and other requirements within a single company. In this encompassing role, Linux is often supplanting a legacy RTOS, and must perform at least on a par with one in terms of responsiveness and throughput.

This tutorial addresses the current and emerging real-time capabilities offered by embedded Linux. In particular, the session details the function and performance attributes of the Preemptible Linux Kernel, the O(1) scheduler and High Resolution POSIX Timers in current implementations. Looking forward, the session covers use of prioritizable work queues in the 2.6 kernel, and the evolution of Linux to support capabilities that include prioritized queuing and priority-inheritance at critical regions, and prioritized interrupt processing. Underlying all session content is the goal of preserving the value of Linux as an open, enterprise-class, standards-compliant platform. Therefore, discussion of on-going Linux progress towards native RTOS-type performance assumes the preservation of existing APIs and semantics, without recourse to sub-kernels or other proprietary technology.

Tutorials

Friday, June 11 • 9:00 AM - 5:00 PM

TUTORIAL 5 - SILICON DEBUG: WHAT DO YOU DO WHEN YOUR ASIC DOES NOT WORK AS FAST AS EXPECTED? Rm: 6C

ORGANIZER: Doug Josephson - *Hewlett-Packard Co., Fort Collins, CO*
PRESENTERS: Bob Gottlieb - *Intel Corp., Santa Clara, CA*
Bill Huott - *IBM Corp., New York, NY*
Jason Stinson - *Intel Corp., Santa Clara, CA*
Bart Vermeulen - *Philips Semiconductor, Eindhoven, The Netherlands*

This tutorial is an overview of the complex process of silicon debug. Silicon debug is the process of ensuring that an integrated circuit is both functionally correct in its operation, and also robustly operates across its entire window of operation (frequency, voltage, processing and temperature). It entails exercising the device on automated test equipment as well as in the system it is intended to operate in, while looking for failure to operate correctly. It is a key step in the path to ensuring high yield, and hence high revenue for your silicon. Debugging entails both designer intervention and tool support, as well as proper testing equipment use.

An overview and the basic approaches of silicon debug are covered initially. Design for debug (DfD) and a review of hardware hooks to facilitate debug are presented for both microprocessors as well as core-based system chips. DfD automation is discussed and illustrated using examples. This is followed by the methods and processes used to perform silicon debug using such features as well as external debug tools. A review of CMOS circuit types is presented and the failure modes of circuits are discussed. With this foundation, the processes of logical and electrical debug are described in detail, and several case studies from actual silicon debug of microprocessors and SoC chips are presented. In conclusion, future challenges for debug are described.

Friday, June 11 • 9:00 AM - 5:00 PM

TUTORIAL 6 - SYSTEMVERILOG FOR VERIFICATION: THE UNIFICATION OF DESIGN, TESTBENCH AND ASSERTIONS IN A SINGLE LANGUAGE Rm: 6D

ORGANIZER: Tom Fitzpatrick - *Synopsys, Inc., Marlboro, MA*
PRESENTERS: Tom Fitzpatrick - *Synopsys, Inc., Marlboro, MA*
Janick Bergeron - *Synopsys, Inc., Ottawa, ON, Canada*
Alan Hunter - *ARM LTD., Cambridge, UK*
Matthew Maidment - *Intel Corp., Portland, OR*

The tutorial will be delivered in two parts. The morning session will provide a detailed overview of the SystemVerilog 3.1a language features, including enhanced modeling features to describe designs more concisely, assertions and other language enhancements to specify the designer's intent. These features enable Design for Verification, which makes models that are inherently easier to verify, both in simulation and formal verification. We will continue with a detailed overview of the testbench and verification features of SystemVerilog, including the object-oriented, constrained, random data-generation and functional coverage features of the language required to assemble the verification infrastructure discussed in the afternoon session.

The afternoon session will present a recommended coverage-driven verification methodology using SystemVerilog. We will show how object-oriented coding techniques, constrained-random stimulus and functional coverage can be used to create a layered testbench environment that exercises design features with greater confidence but with less effort and in less time. We will conclude with a discussion of system-level verification and hardware-assisted verification methodologies, including the reuse of testbench components to verify the design at different levels of abstraction, from SystemC models at the transaction level, through RTL implementation in SystemVerilog down to hardware-assisted platforms, such as accelerators and emulators. The tutorial will conclude with a discussion of modeling guidelines to allow verification IP to be reused at the system level and in a hardware-assisted environment.

UML for SoC Design Workshop — Sunday, June 6 • 9:00 AM – 5:00 PM

41 SAN DIEGO DAC JUNE 7 - 11, 2004

ORGANIZERS: Wolfgang Mueller - *Paderborn Univ.* Grant E. Martin - *Tensilica, Inc.*

UML 2.0 is nearing its final acceptance as an OMG standard and several industrial and academic groups from the EDA, embedded software and systems, and design communities around the world have started to apply it to Systems-on-Chip (SoC) designs.

The DAC UML-SoC workshop is intended to coordinate those efforts, to initiate discussions, and to exchange experiences and information between those groups with a focus on UML application to SoC design and general hardware-related aspects.

REGISTRATION INSTRUCTIONS:
No Conference Registration is required.
$50.00 *ACM/IEEE Members*
$75.00 *Non-Members*

SCHEDULE: Room: 6F

9:00 AM Opening Remarks by the Workshop Organizers

UML and SoC in Japan

9:10 AM An Introduction to the UML for SoC Forum in Japan
T. Hasegawa - *Fujitsu Labs., Japan*

9:25 AM Integrating UML into the SoC Design Process
Q. Zhu, T. Nakata, K. Kuroki, Y. Endo, T. Hasegawa, M. Mine - *Fujitsu Labs., Japan*

10:00 AM A Difference of Model Driven Process between SoC and Software Development and a Brief Demonstration of the Tool XModelink
K. Asari, H. Yoshida, M. Watanabe - *CATS Co., Ltd., Japan*

10:35 AM Break

Executable and Translatable UML

11:00 AM Why Systems-on-Chip Needs More UML Like a Hole in the Head
S. Mellor, J.R. Wolfe, C. McCausland - *Project Technology, USA*

UML and FPGAs

11:35 AM UML-Based Development of Applications for Run-Time Reconfigurable Architectures
Th. Beierlein, Hochschule Mittweida, D. Fröhlich, B. Steinbach - *Technical Univ. Bergakademie, Freiberg, Germany*

12:10 PM UML for FPGA Synthesis
T. Schattkowsky, A. Rettberg - *Paderborn Univ., Germany*

12:45 PM Lunch (Room: 3)

UML and SystemC

1:45 PM Synthesizable SystemC Code from UML Models
W.H. Tan, P.S. Thiagarajan, W.F. Wong, Y. Zhu, National Univ. of Singapore, S.K. Pilakkat - *Institute for Infocomm Research, Singapore*

2:20 PM MDA for SoC Design: UML To SystemC Experiment
P. Boulet, A. Cuccuru, J.-L. Dekeyser, C. Dumoulin, Ph. Marquet, M. Samyn - *Université des Sciences et Technologies de Lille*
R. De Simone, INRIA, G. Siegel - *Esterel Technologies, Inc.*
Th. Saunier - *Thales Communications, France*

2:55 PM Break

UML and SoC Methodologies

3:25 PM UML in an Electronic System Level Design Methodology
M. Lajolo, NEC Labs., USA M. Prevostini - *Univ. of Lugano, Switzerland*

4:00 PM Enhancing UML to Support the Specification of Behavior for Embedded Systems-on-a-Chip
P. Green, M. Edwards - *UMIST, Manchester, UK*

4:35 PM Conclusions, Final Remarks, and Group Discussion

Please check http://www.c-lab.de/uml-soc for up to date information and organizational details.

41 SAN DIEGO DAC JUNE 7 - 11, 2004

The Last Interoperability Workshop — Monday, June 7 • 12:00 PM - 5:00 PM

ORGANIZERS: John Darringer - *IBM Corp.*
Scott Makinen - *Hewlett-Packard Co.*
Rahul Goyal - *Intel Corp.*
Scott Peterson - *LSI Logic Corp.*

REGISTRATION INSTRUCTIONS:

No Conference Registration is required.

$50.00 ACM/IEEE Members

$75.00 Non-Members

This year DAC will host the fifth and final Workshop on Interoperability, a subject of perpetual and passionate interest. Since the first meeting in 2000 there has been remarkable progress in advancing interoperability. There is now the Open Access coalition of 23 companies promoting an open standard API and open database implementation, based on technology from Cadence. Synopsys has established an API for accessing their Milkyway data model and there is a GoldenGate project developing a bridge between the two models. A growing number of EDA companies are migrating their tools to these new interfaces to provide customers with much tighter and more efficient coupling of key applications - enabling a major advance in interoperability needed for design systems to keep pace with advancing technology. The scope has widened to include data management, design constraints and even mask development. The Workshop will consist of an update on the movement followed by presentations from industry leading companies on how these efforts address the interoperability challenges facing the electronics industry, and close with a Panel discussion open to your questions.

SCHEDULE: Rm: 6D

12:00 PM Lunch

Introduction

1:00 PM Welcome: John Darringer - *IBM Corp.*
1:05 PM Milkyway Plans and Status
Rich Goldman - *Synopsys, Inc.*
1:20 PM Open Access Plans and Status
Scott Peterson - *LSI Logic Corp. & Chair: OA Coalition*
1:35 PM Open Access Implementation Status
Joe Santos - *Cadence Design Systems, Inc.*

Industrial Experience *Chair:* Scott Makinen - *Hewlett-Packard Co.*
1:50 PM Jim Brewer - *Hewlett-Packard Co.*
2:00 PM Kevin Cleerman - *LSI Logic Corp.*
2:10 PM Joachim Glas - *Infineon Tech.*
2:20 PM Kazuhiko Kobayashi - *Renesas Technology Corp.*

EDA Vendor Experience *Chair:* Rahul Goyal - *Intel Corp.*
2:30 PM Michael Buehler Garcia - *PDF Solutions, Inc.*
2:40 PM Joe Kwan - *Mentor Graphics Corp.*
2:50 PM Venk Shukla - *Magma Design Automation, Inc.*
3:00 PM Ivo van Zandoort - *Sagantec*

3:10 PM Break

New Directions *Chair:* Scott Peterson - *LSI Logic Corp.*
3:30 PM Data Management
Jim Brewer - *Hewlett-Packard Co.*
3:40 PM Timing and Library Representation
Tim Ehrler - *Philips Semiconductor*
3:50 PM Golden Gate "Bridge"
Jim Wilmore - *Hewlett-Packard Co. and WG Chair*
4:00 PM Design-to-Mask
Steve Schultz - *Silicon Integrated Initiative, Si2, Inc.*

4:10 PM Panel: Are We Done?
Chair: Richard Goering - *EE Times*
Panelists selected from speakers above.

5:00 PM Adjourn

Workshop for Women in Design Automation — Monday, June 7 • 1:00 PM – 5:00 PM

41 SAN DIEGO DAC JUNE 7 - 11, 2004

Career and Life Drivers – "Passion vs. Ambition"

WORKSHOP CHAIR: **Ann Marie Rincon,** *Engineering Fellow, AMI Semiconductor*

STEERING COMMITTEE:

Nanette Collins - *Publicity Chair, 41st DAC*
Marie R. Pistilli – *Co-Chair, Board of Directors, MP Associates, Inc.*
Sonja Wilkerson - *VP Human Resources, Vitria Technology, Inc.*

ROOM:3 **SCHEDULE:**

1:00 PM - 2:00 PM	Registration and buffet lunch
2:00 P M - 3:45 PM	Keynote Address and Panel
3:45 P M - 4:15 PM	Achievement Award Ceremony: Join us as we honor Mary Jane Irwin as this year's Marie R. Pistilli Women in EDA Achievement Award.
4:15 PM	Wine/Cheese Reception: Sponsored by the EDA Consortium

Keynote Address **Duy-Loan Le** - *Senior Fellow, Texas Instruments*

Duy-Loan started as a memory design engineer at the age of 19 with Texas Instruments (TI) and currently serves as the Digital Signal Processor(DSP)Advanced Technology Ramp Manager. In 2002, Duy-Loan became the first East Asian and the first woman to get elected TI Senior Fellow in TI's 70+ years of history, joining 4 other men who hold this prestigious title world wide. Duy-Loan holds 20 patents with 9 pending applications and has published numerous papers. Her long list of accolades include receiving the following awards: "Top 20 Women in Technology Award", "Women on The move" with Congressional recognition for civic leadership, "Women in Technology International Hall of Fame", "Times People" by EE Times , and "National Technologist of the Year".

Corp.

Panel: Transition and Change: How Do I Successfully Navigate My Career Through Turbulent Times?

What drives the decisions you make- pursuit of your passions? What truly interests you and what do you love to do? What do you believe you need to do to move up to the next rung on your career ladder? What are the trade-offs? Are these two ambitions mutually exclusive? How do you feel about the results you've achieved? The Panel will also address ways to "Keep the Passion Alive" as you continue through your career and life. This panel includes women from very diverse backgrounds.

Don't miss the opportunity to learn how prominent professionals in the industry have made career choices to achieve a rewarding personal and professional life experience.

Moderator: Terri Timberman - *Senior Vice President Human Resources, AMI Semiconductor*

Panelists:

Joan L. Mitchell - *IBM Fellow, IBM Printing Systems Division*
Mar Hershenson - Co-Founder/Consulting Assistant Professor, *Barcelona Design/Stanford Univ.*
Darlene Gerry - General Counsel, *AMI Semiconductor*
Deborah Saweuyer-Parks - President and CEO, *Homestead Capital*
Margaret Paroski - Dean of Medical School and BioMedical Sciences, *Univ. of Buffalo*

REGISTRATION INSTRUCTIONS:

No Conference Registration is required.

$50.00 *ACM/IEEE Members*
$75.00 *Non-Members*

I WG Chair

ve, Si2, Inc.

Introduction to Chips and EDA for a Non-Technical Audience

Monday, June 7 • 10:00 AM - 12:00 PM

Rm: 1A

ORGANIZER/SPEAKER: Karen Bartleson, Synopsys, Inc., Mountain View, CA

Have you ever wondered what everyone is talking about at the Design Automation Conference? Do the terms "semiconductor", "synthesis", "DFT", "simulation", "Design for Manufacturing" and "tape-out" sound familiar, but their definitions escape you? If so, then please plan to attend this workshop to gain a basic understanding of chip design and of the wonderful world of Electronic Design Automation (EDA).

This workshop provides:

- A simplified explanation for the layperson of how chips are made
- A portrayal of chip design using Electronic Design Automation
- An opportunity to see and touch the parts that make up chips and electronic products
- A non-threatening, fun event with a working knowledge to take away

This workshop is for:

- Non-engineering staff from technology companies
- Analysts and media people unfamiliar with EDA and semiconductor industries
- Educators and students who are curious about chip technology and design automation
- Friends and relatives of technical people

REGISTRATION INSTRUCTIONS:

No Conference Registration is required.

$10.00 Registration Fee

Tutorial Objectives:

- Provide a basic understanding of EDA and semiconductors to non-technical people
- Present information in simple, easy-to-understand terms
- Use hands-on parts (wafers, chips, masks) for enhanced experience
- Encourage people to join the EDA industry
- Address ongoing requests to help non-technical people understand the EDA industry

Please note:

This workshop is the same as the one presented at DAC 2003. The workshop is for non-technical attendees.

Maximum class size: 50

Hands-on Tutorials

General Information

Hands-on tutorials are three-hour tutorials presented by exhibitors to demonstrate their solutions to a particular issue. This year DAC is offering three hands-on tutorials on Design Methods for Structured ASICs and four hands-on tutorials on Design Methods for Power Minimization. This is an opportunity for attendees with a need to learn about or evaluate products in these area a chance to see, in an in-depth manner, a variety of solutions. Demonstrations are done with the attendees working from Sun workstations while the presenters lead the discussion. The tutorials are limited to the first 30 attendees with a student to workstation ratio of 2:1. Due to the proprietary nature of the discussions, presenting companies have the right to refuse access to employees or contractors of competitors. The cost per tutorial is $75 and attendees are encouraged to enroll in more than one tutorial. Attendees must register for a minimum of an exhibits only registration in order to be eligible to enroll in a Hands-on Tutorial.

A) System-Level Power Management

CoWare, Inc., ChipVision Design Systems AG, and PowerEscape, Inc.

Monday 9:00 AM - 12:00 PM Rm: 11B

Historically, designers have focused on performance and cost but the proliferation of battery operated devices such as MP3 players, digital cameras, digital camcorders, and integrated wireless phones is turning design for low power into a mainstream design challenge. Energy efficient systems must be energy efficient in both standby and active mode and especially the latter is very difficult to achieve with traditional low power hardware techniques and fabrication processes only. Energy efficient systems also require energy efficient software, algorithms and architectures. In this seminar we will start with the core C algorithm of a common consumer device, and take it through a design flow that leads to a low power implementation of that C algorithm using tools from PowerEscape, ChipVision and CoWare.

Using the PowerEscape tools, participants will determine the optimal cache configuration and memory architecture for low power, highlight the energy bottlenecks in the C code and replace them with functionally equivalent C algorithms that accesses memory less frequently and therefo re consumes less energy.

Using the ChipVision tools, participants will explore the energy efficiency of different hard w a re architectures of the top energy bottlenecks, and then do a similar analysis using the more energy efficient C algorithm.

Finally, CoWare will briefly demonstrate how these results flow in its hardware/softwareco-design environment.

Participants will leave the tutorial with a good understanding of the benefits and main tasks involved in approaching design for low power from the system/algorithmic level.

B) Low-Power Design Methodologies and Tools

BullDAST s.r.l., Accent, Inc. and STMicroelectronics

Monday 2:00 PM - 5:00 PM Rm: 11A

Today's designers are facing limitations due to the power dissipation while still being required to deliver increased performance. This tutorial will introduce innovative methodologies for proactively dealing with power estimation and optimization and will offer to the attendees the opportunity of experimenting with the BullDAST PowerChecker design environment. The tutorial will first provide a brief insight of innovative techniques for power estimation at the RTL level. Then, it will be entirely devoted to the practical use of the BullDAST PowerChecker environment on actual designs provided by the partner companies Accent and STMicroelectronics.

The attendees will be given complete design examples and will be guided into the PowerChecker tool flow. First, power consumption of the considered designs will be estimated by PCE, the RTL power estimation engine available within PowerChecker. Next, based on the results of the estimation step, the attendees will invoke the optimization engines available in PowerChecker (i.e., MemArt, CoolBus, CGCap and LPClock). More specifically, MemArt performs automatic partitioning of monolithic memory components; CoolBus allows the exploration of different encoding schemes, suggests the power optimal one and updates the RTL netlist accordingly; CGCap optimizes power consumption of control and steering logic by detecting idle conditions that cannot be captured by simple topological analysis; LPClock automatically generates the clock tree structure for a RTL netlist based on both switching activity and placement information by providing, as output, constraints for the clock synthesis tool.

This hands-on tutorial will demonstrate to the trainees how opportunities for power optimization do exist while shortening the design time and enhancing the design productivity.

C) Using Predictive Analysis to Guide Low Power Design Methodology - Atrenta, Inc.

Tuesday 2:00 PM - 5:00 PM Rm: 11A

Every low power design is different and tends to have its own interesting set of issues to solve. You have to think through various elements of chip design if you want to operate at very low power levels and you have to introduce appropriate design techniques early in the design cycle. This hands-on tutorial discusses predictive analysis techniques provided by Atrenta's SpyGlass LP product as means to help guide the construction of design description that is low power methodology aware. Typical low power design methodology now include gated clock domains for reducing design activity, voltage domains to reduce overall dynamic power, and power domains to reduce leakage power consumption. These techniques add complexity to the design process that must be taken into account early in the design cycle to create a power aware RTL. SpyGlass LP provides a comprehensive set of RTL techniques addressing clock and voltage management needs of a design targeting low power goals. The use of multiple voltage domains introduces new issues in the design process. For example, signals that cross these voltage domain boundaries must be correctly level-shifted. Leakage power is a major concern with designs using the 90 nm process technology and more so for future process technologies. Shutting down portions of the design is the most effective way of dealing with leakage in the stand-by mode of operation. The design methodology involving multiple power domains in a design presents its own set of challenges. Being able to customize your project requirements is an important aspect of ensuring low power methodology goals. We will also briefly introduce the ability to customize your low power requirements using SpyGlass LP.

D) Flows For Power Minimization

Magma Design Automation, Inc. and Infineon Technologies

Wednesday 9:00 AM - 12:00 PM Rm: 11A

Minimizing power has become a major design concern today. However, managing power effectively in a design flow has become extremely difficult since it involves making tradeoffs such as timing-versus-power and area-versus-power at different stages of the design flow. In order to achieve this efficiently, an integrated flow that addresses power concerns from RTL-to-GDSII is required. This tutorial describes the most significant power dissipation and distribution considerations and highlights the requirements for a true low-power design environment.

The attendees will learn how to apply various techniques at the synthesis stage such as power-aware clock gating. They will then be introduced to an automated methodology to handle multiple voltage domains and also techniques to address leakage power using multiple threshold voltage cells.

The attendees will learn how to perform power-aware cell placement to minimize dynamic power consumption. Voltage drop analysis will be performed at various stages and these early results will be used to fine tune the floor plan or the power grid, if needed. Transient analysis that accounts for the capacitive and inductive effects will be demonstrated and the attendees will learn how to perform what-if analysis with on-chip decoupling capacitors to minimize these transients.

The attendees will be introduced to a unique approach for performing power grid synthesis. Instead of the manual power grid design approach they will learn how to perform automatic power grid synthesis to obtain optimal power grid sizes based on user-defined constraints.

Hardware: The tools will run on SUN and Linux computers.

E) Structured ASIC/Platform ASIC Design Methodology

Synplicity, Inc., LSI Logic Corp., and NEC Corp.

Wednesday 2:00 PM - 5:00 PM Rm: 11A

A new breed of design methodology, called Structured ASICs, and Platform ASICs, is answering the needs of hardware designers who are currently choosing between the compromises of FPGA and the cost and effort of cell-based ASIC design platforms. These new methodologies enable designers to build system on a chip devices rivaling ASIC performance at a fraction of the cost of FPGAs, and with a shorter design turnaround time than standard cell ASICs.

This tutorial will focus on the technical and methodology details of both Structured and Platform ASICs across multiple vendors, and will demonstrate these concepts with two leading devices architectures: NEC Electronics' Instant Solution Silicon Platform (ISSP) Structured ASIC architecture, and LSI Logic's RapidChip Platform ASIC device. The tutorial will also demonstrate the customized software flows used by both NEC Electronics' and LSI Logic to address issues in Structured and Platform ASIC design that are different from cell-based ASIC design.

At the tutorial's conclusion, attendees will have the information they need to accurately judge the competitive advantages afforded to them by using a Structured and / or Platform ASIC solution in their next project.

F) Physical Design of Structured ASICs

ViASIC, Inc.

Thursday 9:00 AM - 12:00 PM Rm: 11B

The tutorial will begin with an in-depth exploration of two major classes of structured ASIC architectures: via-programmed and metal-programmed. Participants will learn how these architectures work and the advantages and disadvantages of each, with an emphasis on comparing masks costs, real-world density, design flows, time to market and the yield and signal integrity advantages that come with architectural regularity. We will also review footprint selection, foundry process and other technical design considerations, while looking at the forces driving the rapid adoption of structured ASICs.

Participants will take a real design through the complete design flow, from RTL to tape-out, as they build a via-programmed structured ASIC using leading tools and technologies. Get hands-on experience with the ViaMask 0.13 library and the ViaPath physical implementation tool while performing placement, memory generation, and routing; investigate strategies and techniques for insertion of test, clock and power. The tutorial will also feature a review of the design flow for metal-programmed structured ASICs using physical synthesis and ViASIC's metal routing engine.

G) Designing A Structured ASIC through FPGA Prototyping

Altera Corp. and Synopsys, Inc.

Thursday 2:00 PM - 5:00 PM Rm: 11A

Synopsys has collaborated with Altera to minimize the transition from FPGA prototyping to production. With FPGA prototyping, the customer has the option to continue production with FPGAs, migrate directly to Altera's HardCopy structured ASIC or transition to a more traditional ASIC. The anchor of the design flow is DC-FPGA which allows a customer to design directly to an FPGA or an Altera's HardCopy structured ASIC. FPGA prototype to ASIC conversion is facilitated by script and constraint compatibility between DC-FPGA and the extremely popular DC. This Hands-On Tutorial will guide the attendee from RTL to an Altera HardCopy structure ASIC prototype utilizing the Synopsys design environment.

Adjunct Meetings

North America SystemC Users Group (NASCUG) Meeting – Hosted by Open SystemsC Initiative

www.nascug.org

Monday, June 7 2:00 PM – 5:00 PM Rm: 33A

The inaugural North American SystemC User's Group (NASCUG) meeting will be held Monday afternoon at DAC. A central component of the half-day user's group meeting will be technical presentations on SystemC design experiences. Topics include architectural modeling; Transaction-Level Modeling; Software co-design; Platform design; SystemC tool flows. Come and participate in the first semi-annual NASCUG meeting. A mini suppliers expo will start at 1:30 pm, immediately following the System-level design technical symposium. Find out the latest offerings from SystemC suppliers and sign up for a private demo. And don't miss the beer reception at 5:00 pm!

Denali Users Group – Hosted by Denali Software, Inc.

Monday, June 7 3:00 PM – 9:00 PM Rms: 31ABC & 32AB

The Denali Users Group Meeting gives designers the opportunity to meet with other users to exchange ideas, discuss methodologies, and share problems and solutions for designing and verifying complex chip interfaces. DUG is a technical forum emphasizing presentations on real-world experiences from Denali users. The meeting also gives users the chance to meet with Denali executives and developers to learn more about new product developments and to help drive new directions for Denali products and technologies. The free event includes dinner and cocktails, and features opening remarks and technology roadmap presentation from Denali President Sanjay Srivastava and CTO Mark Gogolewski.

Additional Meetings

CODES-ISSS 2004

CODES-ISSS Program Committee meeting will be held Sunday, June 6, 2004 from 8:00 AM - 5:00 PM in the San Diego Convention Center.

System-Level Design 2004: Here and Now Technical Symposium – Hosted by Open SystemsC Initiative

Monday, June 7 12:00 PM – 1:30 PM Rm: 33A

www.systemc.org lunch provided

The Open SystemC Initiative (OSCI) invites you to learn how recent advancements in SystemC development and adoption apply to you today and moving forward. The symposium features presentations from industry experts on recent SystemC advancements and using SystemC for doing real world system-level design. Status updates on the LRM, technology roadmap and SystemC 2.1 and SCV will be presented.

Will (C)MOS Grow Before Leakage Is Licked? Panel – Hosted by Sequence Design

Monday, June 7 12:00 PM - 2:00 PM Rm: 22

Transistor leakage has become a critical design issue and every indication is that it will become significantly more challenging with each new process generation. Circuit designers, process developers, and EDA tool developers are beginning to spend substantial amounts of effort devising solutions to the leakage problem, and multiple approaches have already been proposed and studied. These include non traditional device structures such as FinFETs and new or modified design techniques such as MTCMOS and VTCMOS. But deploying any of these solutions raises new questions that will be explored in this panel session sponsored by EETimes and Sequence Design. Lunch will be served. Moderator: Brian Fuller, Editor-in-Chief, EETimes. Panelists: Shrekhar Borkar, Director, Circuit Research Lab Intel; Robert Pitts, Senior member of technical staff, Texas Instruments; Scott Becker, CTO, Artisan Components; Jerry Frenkil, VP, Advanced Development, Sequence Design, Inc.; Kaushik Roy, Professor, Purdue University.

Additional Meetings

X Initiative Breakfast – Hosted by X-Initiative & Cadence Design Systems, Inc.

Tuesday, June 8 7:30 AM – 9:00 AM Rm: 20D

The X Initiative welcomes all DAC attendees to its 3rd anniversary breakfast. The event will highlight presentations by member companies on X Architecture silicon results and progress in "2004: The Year of First Production X Chips." The X Initiative, a group of 40+ leading companies from throughout the semiconductor industry, is chartered with accelerating the availability and fabrication of X Architecture, a revolutionary interconnect architecture based on the pervasive use of diagonal routing. For more information, visit www.xinitiative.org.

PSL Consortium – Hosted by PSL Consortium & Cadence Design Systems, Inc.

Tuesday, June 8 11:30 AM – 2:00 PM Rm: 24

The Accellera standard PSL is a mature and popular assertion language supported by many EDA vendors and increasingly accepted by engineers. Come and join other users and vendors to share your experiences and insights on the use of PSL and to hear the latest news on its standardization and implementation. The PSL Consortium is an independent association with the mission to promote the use of PSL and speed its adoption. The event will also feature presentations on a variety of PSL-based methodologies and pertinent technical information.

Electronic System-Level (ESL): Fueling the Future of Sub-Micron Silicon A Language and Methodology Roadmap – Hosted by Summit Design

Summit Design hosts Gartner Dataquest, Synopsys, Mentor, ARM and Verisity

Tuesday, June 8 12:00 PM – 2:00 PM Rm: 33ABC

Registration & Information: www.sd.com lunch provided

The increasing complexity of electronic systems is pushing design, integration, verification, and performance to a breaking point. And yet, companies must develop electronic content that offers clear differentiation and distinct competitive advantage. This panel of experts will discuss the real challenges for future SoC and embedded systems, and the role of ESL in this increasingly complex landscape. Technological challenges, and the roadmap to address new languages (such as SystemVerilog and SystemC) and verification concepts (such as assertion and architecture analysis) will be featured.

SIGDA Ph.D. Forum

Tuesday, June 8 6:30 PM – 8:00 PM Rm: Sails Pavilion

ACM/SIGDA will hold an open member meeting. SIGDA members are invited, as are all members of the EDA community. Light refreshments will be served at 7:00 PM. There will be a brief presentation on SIGDA's programs, but the main focus of the meeting will be the Ph.D. Forum. Aimed at strengthening the ties between academia and industry, students will present posters and discuss their Ph.D. dissertation research with interested attendees. The Ph.D. Forum gives the students feedback on their research, and gives the DA community a preview of work in progress. For more information, see http://www.sigda.org/programs.php.

Electronic System Level Design: Your Future May Depend on It! – Hosted by CoWare, Inc. & Cadence Design Systems, Inc.

Wednesday, June 9 7:30 AM – 9:00 AM Rm: 24

At this free breakfast meeting organized by Cadence and CoWare, find out why your future may depend on the adoption of electronic system level (ESL) tools and methodologies. Experts will discuss worldwide economic and technological pressures driving adoption of ESL methods for design and verification. Many major companies have already made the move. Representatives of some of these companies will discuss their experiences with ESL and why it's giving them an edge in the market. Don't be left behind as the industry moves to ESL! Come find out what you need to know to remain competitive.

Accellera Open Membership Meeting – Hosted by Accellera

Wednesday, June 9 10:00 AM – 11:30 AM Rm: 26AB

Accellera will hold its annual membership meeting to provide an update on its current technical activities including SystemVerilog, Verlog AMS, and PSL, as well as a discussion about exciting plans for the OpenKit project and the new Harmony committee. This meeting is open to all DAC attendees.

Additional Meetings

The Real World Advantages of an RTL Handoff Methodology: Unleashing the New Wave In Silicon (A Technology Symposium) – Hosted by ThinkBold Communications

Wednesday, June 9 12:00 PM – 2:00 PM Rm: 33ABC

Register at http://thinkbold.com/events/rtlhandoff/ lunch provided

According to Gartner Dataquest, "silicon virtual prototyping" from RTL is the most difficult technical challenge in EDA, and yet appears to be the only way to get around the design bottleneck of gate-level sign-off methodologies. While it is believed that the challenges of sub-100-nanometer chips will impose a shift from today's traditional gate-level ASIC handoff to register-transfer-level handoffs, it is also believed that this move will have tremendous impact on users and suppliers of EDA tools and methodologies. Join us as innovative and influential industry leaders discuss the critical issues, as well as their real-world experiences with RTL handoff methodology. Panelists include representatives from Broadcom, IBM, Sony, NEC and Kawasaki Microelectronics. Gary Smith of Gartner Dataquest will serve as the moderator.

Second Annual Hacks & Flacks Roundtable Discussion

Wednesday, June 9 3:30 PM – 4:40 PM Rm: 21

Analysts, Investors and Public Relations Discuss Their Intersecting Needs.

In the EDA community, competition for attention from prospects, customers, the media, and the investment community is increasing. As a company grows, more effort is focused on investor relations (IR). Is the need to communicate with investment analysts only necessary for a public company? How can PR professionals and the investment community help meet one another's needs for exposure and information? What can we do to work together more effectively? This discussion will give analysts and PR people a chance to exchange ideas and develop ways to fulfill company objectives.

Birds-of-a-Feather (BOF) Meetings

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather". All BOF meetings are held at the San Diego Convention Center, Wednesday, June 9, 6:30 PM - 8:00 PM. DAC will facilitate common interest group meetings to discuss DA related topics. To arrange a BOF meeting sign up at the Information Desk located in Lobby C. A room will only be assigned if ten or more people sign up. An LCD projector and screen will be provided. Check DACnet and the Birds-of-a-Feather board at the Information Desk.

CANDE Meeting

Wednesday, June 9 6:00 PM Rm: 25C

CANDE - the Computer Aided Design Technical Committee of the IEEE Circuits and Systems Society - provides a place where EDA/CAD professionals can hold open and long-range discussions on emerging topics through a yearly workshop. Planning sessions for the workshop are held at DAC and ICCAD each year. For more information, please refer to www.cande.net.

Verilog-A for Compact Modeling

Wednesday, June 9 6:00 PM

To discuss the proposed extensions to Verilog-AMS for supporting compact modeling of semiconductor devices.

42nd DAC Call for Papers

42nd DESIGN AUTOMATION CONFERENCE® Anaheim Convention Center, Anaheim, CA • June 13-17, 2005

DAC is the premier conference devoted to Design Automation (DA) and the application of DA tools in designing electronic systems. Four types of submissions are invited: regular papers, special topic sessions, panels and tutorials. Submissions should be made electronically at www.dac.com. Panel and Tutorial suggestions and Special Session submissions are due NO later than **November 3, 2004, 5:00 PM MST**; Regular Papers are due NO later than **November 22, 2004, 5:00 PM MST**.

Requirements for Submission

ALL SUBMISSIONS MUST BE MADE ELECTRONICALLY AT: WWW.DAC.COM

Regular paper submissions must be in PDF format only. Each paper should contain an abstract of approximately 60 words clearly stating the significant contribution, impact and results of the submission AND be no more than 6 pages (including figures, tables and references), double columned, 9pt or 10pt font (format templates are available on the DAC web site for your convenience, but are not required). To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript, abstract or bibliographic citations. Submissions exceeding the 6 page limit with fonts smaller than 9pt, or identifying the authors or their affiliations will be automatically rejected. Previously published papers, or papers simultaneously submitted to another conference, will be automatically rejected.

Regular Papers — Due Nov. 22, 2004, 5 PM MST

All regular papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage. Authors of accepted papers must sign a copyright release form for their paper. Authors must also provide MP Associates a copy of their presentation materials and grant permission for the publication of the presentation and presentation materials on the DAC web site. **Notice of acceptance will be sent via email by March 11, 2005.**

Special Sessions — Due Nov. 3, 2004, 5 PM MST

Special session submissions must include descriptions of suggested papers and speakers, and the importance of the special session to the DAC audience. DAC reserves the right to restructure all special sessions.

Panel and Tutorials — Due Nov. 3, 2004, 5 PM MST

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panels and tutorials.

Student Design Contest — Due Dec. 13, 2004, 5 PM MST

Students are invited to submit descriptions of original electronic designs, either circuit level or system level. Submissions should contain the title of the project, a 60-word abstract, a complete description of the design, not exceeding 4000 words, and not more than 10 diagrams and tables. The submission should clarify the originality, distinguishing features, and measured performance of the design. Two categories of designs - operational and conceptual - are eligible for awards. For operational designs, proof-of-implementation is required, while for conceptual designs, complete simulation is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2003. Submitted designs should not have received awards in other contests. Winners will be presented with their prizes at the 42nd DAC, they will also be invited to present a poster at ISSCC in February 2005.

Topics of Interest

Authors are invited to submit original technical papers describing recent and novel research or engineering developments in all areas of design automation. Topics of interest include, but are not limited to the listing on the following page.

Design Tools Track

The Design Tools track (T) is devoted to contributions to the research and development of design tools and their supporting algorithms. Focus is on innovation of specific modeling, analysis and optimization techniques.

T1.1 Electrical-level circuit and timing simulation
T1.2 Discrete simulation
T1.3 Static timing analysis and timing verification
T1.4 Power analysis and estimation
T2.1 Testing, fault modeling and simulation, TPG, test validation and DFT
T2.2 Transaction-level, RTL and gate-level modeling and validation: simulation, equivalence checking, functional formal (and semi-formal) verification
T3.1 RT-level design partitioning, physical floorplanning and placement
T3.2 Global and detailed routing
T3.3 Module generation, sizing and library optimization, physical verification
T4.1 Technology-independent, combinational logic synthesis
T4.2 Technology-dependent logic synthesis, library mapping, cell-based-design, interactions between logic design and layout
T4.3 Sequential and asynchronous logic synthesis and optimization
T4.4 System, logic and physical synthesis for reconfigurable computing
T4.5 High-level synthesis
T5.1 Interconnect and package modeling and extraction
T5.2 Signal integrity and reliability analysis
T5.3 Analog, mixed-signal MEMS and/or RF design tools
T5.4 System-in-package design and integration tools
T5.5 Design for yield; design-to-manufacturing interface
T6.1 IP protection and reuse for designs, tools, and algorithms
T6.2 Frameworks, intertool communication, design environments and databases

Design Methods Track

The Design Methods track (M) deals with innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art designs. Submissions for this track will be judged on how innovatively tools are combined into a new methodology that is effectively applied to real-world design problems. Papers focusing on algorithmic advances in modeling, analysis and optimization should be submitted to the design tools track.

Design methodologies and case studies for specific design tasks

M1.1 Design entry and specification
M1.2 Electrical-level simulation and modeling
M1.3 Discrete simulation and modeling
M1.4 Static timing and performance analysis
M1.5 Functional design verification
M1.6 Testing, test generation and debugging
M1.7 Physical design, module generation, design for manufacturing
M1.8 Logic synthesis, including interaction with physical synthesis
M1.9 High-level and architectural synthesis

Design methodologies and case studies for specific application domains and platforms

M2.1 Overall design flows and methodologies for specific design applications
M2.2 Configurable computing, FPGAs and rapid prototyping
M2.3 Deep sub-micron: signal integrity, interconnect modeling and extraction
M2.4 High-performance design: timing, clocking and power distribution
M2.5 Low-power design
M2.6 Analog, mixed signal, and RF design
M2.7 Process technology development, extraction, modeling and new devices
M2.8 MEMS, sensors, actuators

Integration and management of DA systems

M3.1 Management of DA systems, design interfaces, standards
M3.2 Distributed, networked, and collaborative design
M3.3 Intellectual property, design reuse and design libraries

Embedded Systems Topics:

Embedded Systems are characterized by mixed hardware and software components with limited processing, I/O and storage resources. The increasing role played by software components and their associated support introduces a host of new system design issues. To focus on these, the 42nd DAC will have embedded systems sessions covering both the "tools" and the "methods" aspects of the following topics:

E1 Low-power design: compilation, scheduling and partitioning
E2 Embedded software: retargetable compilation, memory/cache optimization, real-time single-processor scheduling
E3 HW/SW co-design: specification, modeling, co-simulation and performance analysis, system-level scheduling and partitioning
E4 Hardware and software platform design: IP-based design, communication design, embedded HW
E5 Case studies

Sponsors

The 41st Design Automation Conference is sponsored by IEEE/CASS /CANDE (Institute of Electrical and Electronics Engineers/Circuits and Systems Society), the ACM/SIGDA (Association for Computing Machinery/Special Interest Group on Design Automation), and the EDA Consortium (Electronic Design Automation Consortium). Membership information is available on the sponsors web site or at the conference at the ACM and IEEE booths.

IEEE Circuits and Systems Society

The IEEE Circuits and Systems Society (CASS) is one of the largest societies within IEEE and in the world devoted to the analysis, design, and applications of circuits, networks, and systems. It offers its members an extensive program of publications, meetings and technical and educational activities, encouraging an active exchange of information and ideas. The Society's peer reviewed publication activities include: Trans. on CAD; Trans. on CAS-Part I (Regular Papers); Trans. on CAS-Part II (Express Briefs); Trans. on VLSI; Trans. on CAS for Video Technology; Trans. on Multimedia; and the new Transactions on Mobile Computing which is co-sponsored with IEEE sister societies. CASS also sponsors or co-sponsors a number of international conferences, which include the Design Automation Conference (DAC), the Int'l Conference on Computer-Aided Design (ICCAD) and the Int'l Symposium on Circuits & Systems (ISCAS). A worldwide comprehensive program of advanced workshops including a new series on "Emerging Technologies in Circuits and Systems", as well as our continuing education short courses bring to our worldwide membership the latest developments in cutting-edge technologies of interest to industry and academia alike. The IEEE/CASS has been serving its membership for over 50 years with such member benefits as:

- Discounts on all Society publications, conferences and workshops (including co-sponsored and sister society publications and conferences)
- The Society Magazine which includes articles on emerging technologies, society news and current events
- Opportunities to network with peers and experts within our 17 focused committee meetings, the local events of over 60 chapters and more than 20 annual conferences/workshops
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- And all the personal and professional benefits of IEEE/CASS membership

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Sponsors/Proceedings

ACM/SIGDA -The Resource for EDA Professionals

ACM/SIGDA, one of the three organizations that sponsor DAC, has a long history of supporting DAC and the EDA profession. In addition to sponsoring DAC, SIGDA sponsors ICCAD, DATE, and ASP-DAC, and many smaller EDA conferences, symposia and workshops.

SIGDA has pioneered electronic publishing of EDA literature since 1989, and now produces CD-ROM proceedings for most major EDA conferences and symposia. For the past 10 years, SIGDA has also produced an annual CDROM Compendium of those proceedings, which has grown this year to a Super-Compendium DVD containing 10 years of EDA literature; this Compendium is sent to our members yearly as a member benefit. Further, SIGDA provides strong support for the ACM journal TODAES (Transactions on Design Automation of Electronic Systems).

SIGDA also publishes two electronic "newsletters". SIGDA's E-Newsletter is sent to all members twice each month, and contains information on upcoming conferences and funding opportunities. SIGDA's DA TechNews provides all SIGDA members with a summary of the latest EDA news twice each month.

In addition to electronic publishing, SIGDA provides a broad array of additional resources to its members and to the EDA profession in general. SIGDA organizes and provides partial funding for the University Booth and Ph.D. Forum at DAC and the CADathlon at ICCAD, and funds various scholarships and awards. SIGDA also publishes its Monthly Planner several times per year, helping EDA professionals plan their conference activities. For further information on SIGDA's programs and resources, see http://www.sigda.org.

In addition, SIGDA members may also want to consider joining our parent organization, ACM. ACM membership provides access to a variety of ACM products and resources, including discounts on conferences, subscriptions to ACM journals and magazines, and the ACM Digital Library, an invaluable IT resource. For further details, see ACM's home page at http://www.acm.org.

As an EDA professional, isn't it time YOU joined SIGDA?

SIGDA/DAC University Booth

Each year SIGDA organizes the University Booth. The booth is an opportunity for university researchers to display their results and to interact with visitors from industry. Priority is given to presentations that complement the conference technical program. Demos that highlight benchmark results are also encouraged. The Design Contest winners will give demonstrations presenting their designs at the University Booth, Tuesday, June 8, 12:00 PM - 2:00 PM. The schedule of presentations will be published at the conference and will also be available on the SIGDA website. We thank the Design Automation Conference for its continued support of this project.

41st DAC Proceedings

The 41st DAC proceedings will contain 163 papers, panels, and special sessions. DAC is offering each conference and student registrant 41 years of DAC proceedings on DVD. One hardbound copy of this year's proceedings will be available to registrants for $35 at the time of registration. Should you wish to purchase additional copies, you may do so at the ACM kiosk in Lobby D via self-help on-line computer orders. After the conference, mail orders should be sent to ACM or IEEE. The addresses for mail orders are:

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EDA Consortium

The EDA Consortium is the international association of companies that provide tools and services that enable engineers to create the world's electronic products.

EDA Consortium addresses issues that are common to its members and the community they serve. Recent accomplishments include simplification of international EDA export regulation and publication of an industry Operating Systems Roadmap.

Companies that become EDA Consortium members are eligible for a 10% discount on DAC Exhibit Space. Contact EDA Consortium today about membership opportunities.

DAC/ISSCC Student Design Contest

The purpose of the Student Design Contest is to promote excellence in the design of electronic systems by providing competition between graduate and undergraduate students at universities and colleges. This year we received over 50 submissions in two categories: "Conceptual" and "Operational". Operational designs are those which have been implemented and tested. Conceptual designs have not yet been fabricated and tested but must have been thoroughly simulated. Students compete for cash prizes donated by a number of industrial supporters, as well as the conference. Prize winners are listed here in the final program and have been invited to show their work at the University Booth on the show floor. Awards will be given at the DAC Pavilion, on Wednesday, June 9, 2004 from 3:00 PM - 3:45 PM.

DAC/ISSCC 2004 Student Design Contest Winners

Operational Category:

1st Place (Best Overall) *A Single Chip Ultra-Wideband Transceiver*

Fred S. Lee, Anantha P. Chandrakasan, Raúl Blázquez - *Massachusetts Institute of Technology, Cambridge, MA*
Puneet P. Newaskar - *Silicon Labs, Austin, TX*

2nd Place *81 MS/s JPEG 2000 Single-Chip Encoder with Rate-Distortion Optimization*

Hung-Chi Fang, Yu-Wei Chang, Liang-Gee Chen - *National Taiwan Univ., Taipei, Taiwan*

3rd Place (tie) *An 80Gbps FPGA Implementation of a Universal Hash Function based Message Authentication Code*

Bo Yang, Ramesh Karri - *Polytechnic Univ., Brooklyn, NY*
David A. McGrew - *Cisco Systems, Inc., San Jose, CA*

3rd Place (tie) *A Modular 32-Site Wireless Neural Stimulation Microsystem*

Maysam Ghovanloo, Khalil Najafi - *Univ. of Michigan, Ann Arbor, MI*

Conceptual Category:

1st Place *The Economical Aphotic Sieving Machine*

Kamran Kashef, Matt Hardy - *Univ. of Michigan, Ann Arbor, MI*

2nd Place *VIRAM1: A Media_Oriented Vector Processor with Embedded DRAM*

Joseph Gebis, Sam Williams, David Patterson - *Univ. of California, Berkeley, CA*
Christos Kozyrakis - *Stanford Univ., Palo Alto, CA*

3rd Place *SiGe Prototype Chip Design Implementing CMOS Fixed Bit-Load Drivers and Receivers for Next Generation High-Speed Board-Level Interconnect*

Jason D. Bakos, Amit Gupta, Leo Selavo, Donald Chiarulli - *Univ. of Pittsburgh, Pittsburgh, PA*

Award Contributors:

Awards

Marie R. Pistilli Women in EDA Achievement Award

- Mary Jane Irwin - *A. Robert Noll Chair of Engineering, Penn State Univ., University Park, PA*

For her significant contributions in helping women advance in the field of EDA technology.

The P. O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering

The objective of the P. O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering and Computer Science from under-represented groups (women, African American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship and SIGDA continues to administer the program for DAC. DAC normally funds two or more $4000 scholarships, renewable up to 5 years, to graduating high school seniors.

The 2004 winners are:

Conner Skye Riley - attending Franklin W. Olin College of Engineering, Boston, MA

Hans Edgar Anderson - attending Massachusettes Institute of Technology, Cambridge, MA

For more information about the P. O. Pistilli scholarship, please contact Dr. Cherrice Traver, ECE Dept., Union College, Schenectady, NY 12308, email: traverc@union.edu.

Design Automation Conference Graduate Scholarships

Each year the Design Automation Conference sponsors several $24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in "design and test automation of electronic and computer systems". Each scholarship is awarded directly to a university for the Faculty Investigator to expend in direct support of one or more DA graduate students.

The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are: the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Prof. Jiang Hu - Texas A&M Univ., College Station, TX
Student: Chin-Ngai Sze
Integrated Placement and Skew Optimization for Variation Tolerant and Low Power Clock Network

Prof. Adrian Nunez-Aldana - Syracuse Univ., Syracuse, NY
Students: Amit Varde, Chandrasekar Rajagopal
Synthesis of High-Performance Digital Circuits

Information on next year's DAC scholarship award program will be available on the DAC web page: http://www.dac.com.

ACM Transaction on Design Automation of Electronic Systems (TODAES) 2004 Best Paper Award

Cluster Assignment for High-Performance Embedded VLIW Processors, Volume 7, Issue 3, July 2002
Viktor S. Lapinskii, Margarida F. Jacome, Gustavo A. DeVeciana - Univ. of Texas, Austin, TX

Awards

The Association for Computing Machinery/Special Interest Group on Design Automation (ACM/SIGDA) presents its Distinguished Service Awards

• James P. Cohoon - *Univ. of Virginia, Charlottesville, VA*
For exemplary service to SIGDA, to ACM, to DAC, and to the EDA profession as a whole.

2003 Phil Kaufman Award for Distinguished Contributions to EDA

• A. Richard Newton - *Dean of the College of Engineering, Univ. of California, Berkeley, CA*
For contributions to advancing the EDA industry are numerous and significant, directly impacting the success of our users-electronic designers.

IEEE CASS Mac Van Valkenburg Award

Gary D. Hachtel - Univ. of Colorado, Boulder, CO
For a distinguished career of fundamental innovations across the broad spectrum of semiconductor Electronic Design Automation: from process and device modeling through circuit simulation and optimization to logic synthesis and formal verification.

IEEE CASS Meritorious Service Award

Bing J. Sheu - Nassda Corp., Santa Clara, CA
For outstanding leadership and innovative/significant service contributions to CASS as Society President, Vice President, Editor-in Chief, and Chair of numerous committees.

IEEE CASS Chapter-of-the-Year Award

France Chapter
Chapter Chair - Amara Amara - ISEP, Paris, France
Chapter Vice Chair - Agnieszka Konczykowska - Alcatel R&I / OPTO+, Marcoussis, France
Chapter Secretary - Thomas Ea - ISEP, Paris, France

2004 IEEE Fellows

• Xuemin Chen - *Broadcom Corp., San Diego, CA*
For contributions to video coding standardization and its implementation for satellite and cable communication systems.

• Rajesh K. Gupta - *Univ. of California, San Diego, CA*
For contributions to high-level synthesis and computer aided design of digital circuits and systems.

• Graham Reginald Hellestrand - *VaST Systems Technology Corp., Sunnyvale, CA*
For contributions to computer system architecture simulations.

• Xianlong Hong - *Tsinghua Univ., Beijing, China*
For contributions to the physical design of integrated circuits.

• Leon Stok - *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
For the development and application of high-level and logic synthesis algorithms.

IEEE CASS Donald O. Pederson Award

Synthesis of Reversible Logic Circuits, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 22, no. 6, pp. 710-722, June 2003.
Vivek V. Shende, Aditya K. Prasad, Igor L. Markov, John P. Hayes - Univ. of Michigan, Ann Arbor, MI

IEEE CASS Guillemin-Cauer Award

Phase Noise and Timing Jitter in Oscillators With Colored-Noise Sources, IEEE Transactions on Circuits and Systems - Part I: Fundamental Theory and Applications, vol. 49, no. 12, pp. 1782-1791, December 2002.
Alper Demir - Koc Univ., Sanyer-Istanbul, Turkey

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Exhibitor Liaison Committee/Student Design Contest Judges

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Wayne Dietrich
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