call for papers

TOPICS OF INTEREST

Authors are invited to submit original technical papers describing recent and novel research or engineering developments in all areas of design automation. Topics of interest include, but are not limited to:

DESIGN TOOLS TRACK

The Design Tools track (T) is devoted to contributions to the research and development of design tools and their supporting algorithms. Focus is on innovation of specific modeling, analysis and optimization techniques.

T0.1 Fundamental CAD Algorithms, e.g., BDDs, graph coloring, partitioning
T1.1 Electrical-level circuit and timing simulation
T1.2 Discrete simulation
T1.3 Static timing analysis and timing verification
T1.4 Power estimation
T2.1 Testing, fault modeling and simulation, TPG, test validation and DFT
T2.2 Design and implementation verification (excluding layout verification)
T3.1 Floorplanning and placement
T3.2 Global and detailed routing
T3.3 Module generation and compaction, transistor sizing and cell library optimization, layout verification
T4.1 Technology-independent, combinational logic synthesis
T4.2 Technology-dependent logic synthesis, library mapping, interactions between logic design and layout
T4.3 Sequential and asynchronous logic synthesis and optimization
T4.4 System, logic and physical synthesis techniques for reconfigurable computing
T4.5 High-level synthesis
T5.1 Interconnect and package modeling and extraction
T5.2 Signal integrity and reliability analysis
T5.3 Analog and mixed-signal design tools and RF
T5.4 Microsensor and microactuator design tools
T5.5 Statistical design and yield maximization
T6.1 IP protection and watermarking techniques for designs, tools, and algorithms
T6.2 Frameworks, intertool communication, WWW-based tools and databases

DESIGN METHODS TRACK

The Design Methods track (M) deals with innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art designs. Submissions for this track will be judged on how innovatively tools are combined into a new methodology that is effectively applied to real-world design problems. Papers focusing on algorithmic advances in modeling, analysis and optimization should be submitted to the design tools track.

Design methodologies and case studies for specific design tasks

M1.1 Design entry and specification
M1.2 Electrical-level simulation and modeling
M1.3 Discrete simulation and modeling
M1.4 Static timing and performance analysis
M1.5 Functional design verification
M1.6 Testing, test generation and debugging
M1.7 Physical design, module generation, design for manufacturing
M1.8 Logic synthesis, including interaction with physical synthesis
M1.9 High-level and architectural synthesis

Design methodologies and case studies for specific application domains and platforms

M2.1 Overall design flows and methodologies for specific design applications
M2.2 Configurable computing, FPGAs and rapid prototyping
M2.3 Deep sub-micron: signal integrity, interconnect modeling and extraction
M2.4 High-performance design: timing, clocking and power distribution
M2.5 Low power design
M2.6 Analog, mixed signal, and RF design
M2.7 Process technology development, extraction, modeling and new devices
M2.8 MEMS, sensors, actuators

Integration and management of DA systems

M3.1 Management of DA systems, design interfaces, standards
M3.2 Distributed, networked, and collaborative design
M3.3 Intellectual property, design re-use and design libraries

EMBEDDED SYSTEMS TOPICS

Embedded Systems are characterized by mixed hardware and software components with limited processing, I/O and storage resources. The increasing role played by software components and their associated support introduces a host of new system design issues. To focus on these, the 39th DAC will have embedded systems sessions covering both the "tools" and the "methods" aspects of the following topics:

E1 Low-power design: compilation, scheduling and partitioning
E2 Embedded software: retargetable compilation, memory/cache optimization, real-time single-processor scheduling
E3 HW/SW co-design: specification, modeling, co-simulation and performance analysis, system-level scheduling and partitioning
E4 Hardware and software platform design: IP-based design, communication design, embedded HW
E5 Case studies

SUBMISSION DEADLINES

Panels and Tutorials Nov. 1st, 2001, at 5 pm MST. Regular papers and special topic sessions by Dec. 7th, 2001, 5 pm MST. Student Design Contest Submissions are due Dec. 20th, 5 pm MST.

REQUIREMENTS FOR SUBMISSIONS

All DAC Submissions must be made electronically in PDF format. Reference the DAC web page (www.dac.com) for instructions on electronic submissions. Please submit **ONE PDF** file:

- The paper should contain an abstract of approximately 60 words clearly stating the significant contribution, impact and results of the submission. The paper should be formatted in double columns with a minimum 10pt font, not to exceed 8-pages including all figures, tables and references (format templates are available on the DAC website for your convenience, they are not required). Submissions exceeding the 8 page limit, fonts smaller than 10pt, or identifying the authors or their affiliations will be automatically rejected.

The following information will be needed when submitting your paper:

- Name, affiliation, and complete address for each author
- A designated contact person including his/her phone number, fax number, and email address
- A designated presenter, should the paper be accepted
- A list of topic numbers (taken from the lists above) most clearly matching the content of the paper. This list should be ordered by relevance.
- The following statement: "*All appropriate organizational approvals for the publication of this paper have been obtained. If accepted, the author(s) will prepare the final manuscript in time for inclusion in the Conference Proceedings and will present the paper at the Conference*".
- Authors of accepted papers must sign a copyright release form for their paper. Authors must also provide MP Associates a copy of their presentation materials and grant permission for the publication of the presentation and presentation materials on the DAC web site.

To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript, abstract or bibliographic citations. The papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage. **Notice of acceptance will be mailed to the contact person by March 8, 2002.**

PANELS, TUTORIALS, SPECIAL TOPICS

Panel and tutorial suggestions should not exceed two pages in length and should describe the topic and intended audience. They should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure and modify submitted panel and tutorial suggestions, including moderators and participants. **Panel and tutorial suggestions must be electronically submitted NO later than November 1, 2001 (5:00pm MST).**

Special Topic Sessions may be either independent papers with a common theme or a set of closely related papers describing an overall system. In both cases, independent reviews of each paper and evaluation of the session as a whole will be used to select sessions. **Suggestions for Special Topic Sessions should be submitted along with the list of papers to be included in the session and should describe the session's theme. These submissions must be electronically submitted NO later than December 7, 2001 (5:00pm MST).**

STUDENT DESIGN CONTEST

Submissions of original electronic designs (circuit or system), developed at universities and research organizations after June 2000 and resulting in operational implementations are invited. Submissions should contain the title of the project, a 60-word abstract and a complete description of the design, not exceeding 4000 words in text. The submission should clarify the originality, distinguishing features, and the measured performance metrics of the design. Proof-of-implementation in the form of die or board photographs and measurement data is a must. Submitted designs should not have received awards in other contests. Submissions will be reviewed by a special committee of experts. Selected designs will be presented and exhibited at the conference. **These submissions must be electronically submitted NO later than December 20, 2001 (5:00pm MST).**

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EDA

2002 39th design automation conference®

The Design Automation Conference (DAC) is the world's premier event for the design of electronic circuits and systems. Leading industry experts will be presenting the latest developments in design automation tools and methodologies, silicon solutions, and embedded system-on-chip. DAC also unites EDA users & developers, silicon strategists and embedded system developers for collaboration on tools and design methodologies for effective system and IC design.

Five types of submissions are invited:
regular papers, special topic sessions, student design contest, panels, and tutorials.

VISIT OUR WEBSITE FOR INFORMATION ON THE ELECTRONIC SUBMISSION PROCESS & DEADLINES:
www.dac.com

call for papers

39th design automation conference®

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new orleans, louisiana, usa
june 10-14, 2002

call for papers

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