CONFERENCE PROGRAM & EXHIBITS GUIDE

58 DESIGN AUTOMATION CONFERENCE

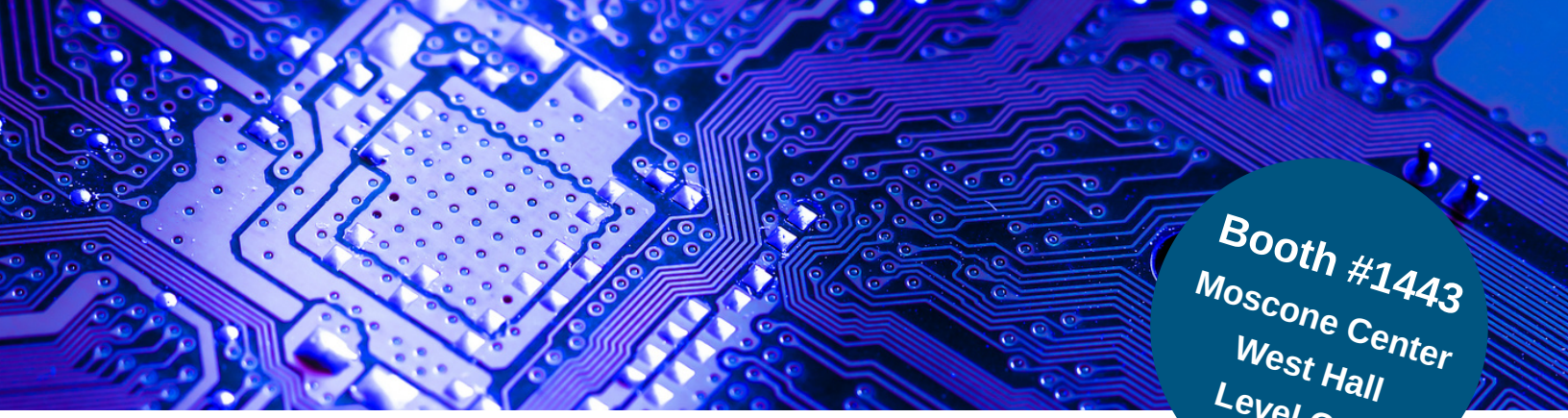
Sponsored by: SIGDA (acm), CEDA® IEEE Council on Electronic Design Automation

In Technical Cooperation with SSCS

#DAC58

DECEMBER 5-9, 2021 • Moscone West Convention Center

Moscone West, San Francisco, CA



Booth #1443
Moscone Center
West Hall
Level One

License Asset Manager™ with Usage Monitoring

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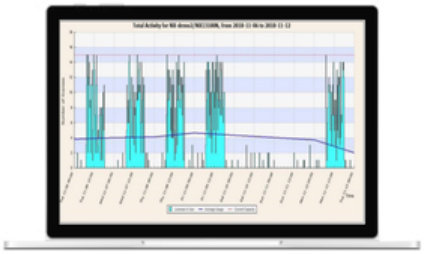
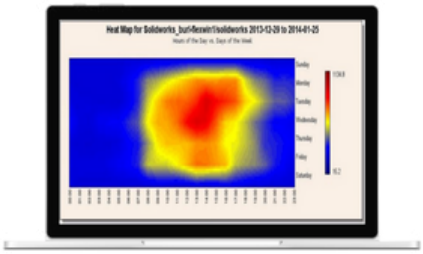
LAMUM™ is a comprehensive software asset management tool for consolidating all engineering software assets, licenses, and vendor information while providing complete current and historical usage information. Our proprietary software monitors the leading EDA Programs: Cadence, Synopsys and Mentor Graphics as well as many other EDA, CAD, Simulation and testing software tools.

Current Overview Gas Gauges

License Concurrency



Usage Activity



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Software License Management for Engineering Applications

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Info@Teameda.com

WELCOME!

Dear Colleagues,

Welcome to the 58th Design Automation Conference, and welcome back to the beautiful city by the bay—San Francisco!

DAC has always been a unique event and this year is no exception. After all, DAC is the only event that brings together the entire design and design automation ecosystem, which includes academic and industrial researchers, electronic executives and managers, IC and systems designers and developers, educators, and of course vendors.

Planning the 58th DAC involved over a year's worth of hard work. And despite a mountain of challenges and hurdles encountered along the way, I couldn't be prouder of what this year's DAC executive committee along with hundreds of other volunteers were able to accomplish. Indeed, this year's DAC has encountered many firsts. For example, this is the first DAC to be rescheduled from its normal early summer timeframe to December due to the COVID-19 pandemic. In addition, this is the first DAC to co-locate with both the RISC-V Summit and SEMICON West. And I am excited to announce that this is the first DAC to go hybrid by offering both a live and virtual component, which should expand our global reach.

Here is a look at the 58th DAC's vast content by the numbers:

- 4 Keynote Speakers
- 3 Pavilion SkyTalks (Short Keynotes)
- 2 Pavilion Industry Analysis Reviews
- 4 Pavilion Invited TechTalks
- 4 Pavilion Panels
- 10 Tutorials
- 3 Workshops
- 215 Research Manuscript Talks
- 32 Research Special Invited Session Talks
- 5 Research Panels
- 10 Research Late Breaking Result Short Papers
- 66 Research Work-in-Progress Posters
- 70 Industry Focused Designer, IP, and Embedded Systems Talks
- 93 Industry Focused Designer, IP, and Embedded Systems Posters
- 4 Training Day Sessions

Be sure to join our networking event daily at 6:00pm where you can meet up with old friends or make some new ones. So, don't be shy, come by and say hi!

Enjoy the #58thDAC!

HARRY FOSTER

58th DAC General Chair

SIEMENS EDA

TABLE OF CONTENTS

General Chair's Welcome 3
Conference Information 5
Networking Receptions 6
Keynotes 7-8
SkyTalk 9-10
TechTalks 10-11
In Memoriam 13-15
2021 Awards 16-17
DAC Pavilion – Booth 2240 18-21
Panels 22
Workshops 23-24
Monday 25-37
Tuesday 38-49
Wednesday 50-62
Thursday 63-67
Virtual Program 67-96
Additional Meetings 97
I Love DAC 98
Design on Cloud Theater 99
Exclusive Sponsorships 100
Conference Sponsors 100
Exhibitor List 101-103
Committees 104-105

Program information as of November 9. All session information subject to change. Please check the DAC mobile app for the most recent information.

CONFERENCE INFORMATION

Exhibit Hours

Exhibit Halls on Level 1 and Level 2

Monday, December 6

Exhibits Open: 10:00 am – 6:00 pm

Tuesday, December 7

Exhibits Open: 10:00 am – 6:00 pm

Wednesday, December 8

Exhibits Open: 10:00 am – 6:00 pm

Registration Hours

Location: Level 1 Lobby

Friday, December 3	12:00 pm – 6:00 pm
Saturday, December 4	8:00 am – 6:00 pm
Sunday, December 5	7:00 am – 7:00 pm
Monday, December 6	7:00 am – 7:00 pm
Tuesday, December 7	7:00 am – 7:00 pm
Wednesday, December 8	7:00 am – 7:00 pm
Thursday, December 9	7:00 am – 5:00 pm

Online Proceedings

To view the proceedings, please visit – **https://ssl.linklings.net/organizations/dac/dac2021_proceedings/views/at_a_glance.html**

Stay Connected

Complimentary Wifi is provided for all attendees.

Network Name: **DAC2021**

Password: **58DAC2021**

'Birds of a Feather' Meetings

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal, non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather" (BOF).

All BOF Meetings are held at the Moscone Center West, Tuesday December 7 from 7:00 pm – 8:30 pm in rooms 3014, 3016, and 3018. To arrange a BOF meeting, please email DAC Show Management at **info@dac.com**.

First Aid Room

Moscone West First Aid Office is located on the 1st floor near the Howard Street entrance (behind Registration). Phone: 415.974.4159

REPORT ALL MEDICAL EMERGENCIES IMMEDIATELY

To report a medical emergency, call "511" on any white House Phone, or on a call phone dial 415.974.4021

DAC Mobile App

Download the official DAC 58 Mobile App for the most up to date schedule, speaker changes, and general announcements!

To download the mobile app, visit **app.dac.com**.

Or scan the QR code below.

COVID-19 Guidelines

For the most up-to-date information regarding DAC's Health and Safety Guidelines, download the mobile app or visit **www.dac.com/Attend/COVID-19-Precautions**

DAC NETWORKING OPPORTUNITIES

Networking Receptions

Sunday, December 5

Welcome Reception

6:00 pm – 7:30 pm | Level 3 Lobby

TPC Reception (invitation-only)

7:30 pm – 9:00 pm | Level 2 Lobby

Monday, December 6

Design/IP/Embedded Track Poster Session and Networking Reception

5:00 pm – 6:00 pm | Exhibit Hall Level 2

Monday Networking Reception Honoring Women in Electronic Design

Guest Speakers:

- Renu Mehra, 2021 DAC Marie Pistilli Award Recipient & R&D Group Director for the Digital Design Group at Synopsys
- Caroline Herzog, Executive Vice President, General Counsel Arm

6:00 pm – 7:30 pm | Level 2 Lobby

Women's Reception is sponsored by

arm SYNOPSYS®

Tuesday, December 7

Design/IP/Embedded Track Poster Session and Networking Reception

5:00 pm – 6:00 pm | Exhibit Hall Level 2

Networking Reception & Work-in-Progress Poster Session

6:00 pm – 7:00 pm | Level 2 Lobby

Wednesday, December 8

Design/IP/Embedded Track Poster Session and Networking Reception

5:00 pm – 6:00 pm | Exhibit Hall Level 2

Networking Reception & Work-in-Progress Poster Session

6:00 pm – 7:00 pm | Level 2 Lobby

Thank You to Our Jazz Band

methodics Jazz by Perforce

KEYNOTE PRESENTATIONS

JEFF DEAN

SVP, Google Research & Google Health

The Potential of Machine Learning for Hardware Design

Monday, December 6, 2021 | 8:45 am – 9:45 am

In this talk Jeff Dean will describe the tremendous progress in machine learning over the last decade, how this has changed the hardware we want to build for performing such computations, and describe some of the areas of potential for using machine learning to help with some difficult problems in computer hardware design. Dean will also briefly touch on some future directions for machine learning and how this might affect things in the future.

Jeff Dean (ai.google/research/people/jeff) joined Google in 1999 and is currently a Google Senior Fellow and SVP for Google Research and Google Health. His teams are working on systems for speech recognition, computer vision, language understanding, and various other machine learning tasks. He has co-designed/implemented many generations of Google's crawling, indexing, and query serving systems, and co-designed/implemented major pieces of Google's initial advertising and AdSense for Content systems. He is also a co-designer and co-implementor of Google's distributed computing infrastructure, including the MapReduce, BigTable and Spanner systems, protocol buffers, the open-source TensorFlow system for machine learning, and a variety of internal and external libraries and developer tools.

Jeff Dean received a Ph.D. in Computer Science from the University of Washington in 1996, working with Craig Chambers on whole-program optimization techniques for object-oriented languages. He received a B.S. in computer science & economics from the University of Minnesota in 1990. He is a member of the National Academy of Engineering, and of the American Academy of Arts and Sciences, a Fellow of the Association for Computing Machinery (ACM), a Fellow of the American Association for the Advancement of Sciences (AAAS), and a winner of the 2012 ACM Prize in Computing.

BILL DALLY

Chief Scientist, NVIDIA

GPUs, Machine Learning, and EDA

Tuesday, December 7, 2021 | 8:45 am – 9:45 am

GPU-accelerated computing and machine learning (ML) have revolutionized computer graphics, computer vision, speech recognition, and natural language processing. We expect ML and GPU-accelerated computing will also transform EDA software and as a result, chip design workflows. Recent research shows that orders of magnitudes of speedups are possible with accelerated computing platforms and that the combination of GPUs and ML can enable automation on tasks previously seen as intractable or too difficult to automate. This talk will cover near-term applications of GPUs and ML to EDA tools and chip design as well as a long term vision of what is possible. The talk will also cover advances in GPUs and ML-hardware that are enabling this revolution.

Bill Dally joined NVIDIA in January 2009 as chief scientist, after spending 12 years at Stanford University, where he was chairman of the computer science department. Dally and his Stanford team developed the system architecture, network architecture, signaling, routing and synchronization technology that is found in most large parallel computers today. Dally was previously at the Massachusetts Institute of Technology from 1986 to 1997, where he and his team built the J-Machine and the M-Machine, experimental parallel computer systems that pioneered the separation of mechanism from programming models and demonstrated very low overhead synchronization and communication mechanisms. From 1983 to 1986, he was at California Institute of Technology (CalTech), where he designed the MOSSIM Simulation Engine and the Torus Routing chip, which pioneered "wormhole" routing and virtual-channel flow control. He is a member of the National Academy of Engineering, a Fellow of the American Academy of Arts & Sciences, a Fellow of the IEEE and the ACM, and has received the ACM Eckert-Mauchly Award, the IEEE Seymour Cray Award, and the ACM Maurice Wilkes award. He has published over 250 papers, holds over 120 issued patents, and is an author of four textbooks. Dally received a bachelor's degree in Electrical Engineering from Virginia Tech, a master's in Electrical Engineering from Stanford University and a Ph.D. in Computer Science from CalTech. He was a cofounder of Velio Communications and Stream Processors.

JOE COSTELLO

Executive Chairman at Arrikto, Metrics, KWIKBIT

When the Winds of Change Blow, Some People Build Walls and Others Build Windmills

Wednesday, December 8, 2021 | 8:45 am – 9:45 am

Joe Costello is considered to have founded the EDA industry when in the late 1980s he became President of Cadence Design Systems and drove annual revenues to over $1B—the first EDA company to achieve that milestone. In 2004, he was awarded the Phil Kaufman Award by the Electronic System Design Alliance in recognition of his business contributions that helped grow the EDA industry. After leaving Cadence, Joe has led numerous startups to successful exits such as Enlighted, Orb Networks, think3, and Altius. He received his BS in Physics from the Harvey Mudd College and also has a master's degree in Physics from both Yale University and UC Berkeley.

KURT KEUTZER

Professor, University of California, Berkeley

AI, Machine Learning, Deep Learning: Where are the Real Opportunities for the EDA Industry?

Thursday, December 9, 2021 | 8:45 am – 9:45 am

Kurt Keutzer is a Professor of the Graduate School in EECS at University of California, Berkeley, where he is also a member of the Berkeley AI Research (BAIR) Lab and co-director of the Berkeley Deep Drive research consortium. His research covers all aspects of making Deep Learning efficient. His "Squeeze" family of Deep Neural Nets were among the first neural nets suitable for mobile and IOT applications. His collaboration on the LARS and LAMB algorithms reduced the training time of ImageNet and BERT to minutes. Previously, Kurt was CTO at Synopsys, and his contributions to Electronic Design Automation were recognized at the 50th Design Automation Conference where he was noted as a Top 10 most-cited author, author of a Top 10 cited paper, and one of only three people to win four Best Paper Awards in the fifty-year history of that conference. As an entrepreneur Kurt has been an investor and advisor to over 30 startups. His most recent exits have been DeepScale (where he was co-founder), acquired by Tesla, and BabbleLabs (investor and advisor), acquired by Cisco. He was the first investor in Coverity, and he was among the first group of investors in Tensilica, and, more recently, Covariant.

SKYTALK PRESENTATIONS

WILLIAM CHAPPELL

CTO, Azure Global

Cloud & AI Technologies for Faster, Secure Semiconductor Supply Chains

Monday, December 6, 2021 | 1:00 pm – 1:45 pm

Semiconductors are deeply embedded in every aspect of our lives, and recent security threats and global supply chain challenges have put a spotlight on the industry. Significant investments are being made both by nation states and commercial industry, to manage supply chain dependencies, ensure integrity and build secure, collaborative environments to foster growth. These shifts provide unique opportunities for our industry. This talk blends insights and experiences from government initiatives and Azure's Special Capabilities & Infrastructure programs, to outline how Cloud + AI technologies, along with tool vendors, fabless semiconductor companies, IP providers, foundries, equipment manufacturers and other ecosystem stakeholders can contribute to building a robust, end-to-end, secure silicon supply chain for both commercial and government applications, while generating value for their businesses.

Dr. William Chappell is the CTO of Azure Global. He is currently bootstrapping efforts for Microsoft in Space, Critical Infrastructure, and Secure Hardware Design. He was formerly the director of the Defense Advanced Research Projects Agency (DARPA) Microsystems Technology Office (MTO). Serving in this position, he focused the office on three key thrusts important to National Security. These thrusts included ensuring unfettered use of the electromagnetic spectrum, building an alternative business model for acquiring advanced DoD electronics that feature built-in trust, and developing circuit architectures for next-generation machine learning. He created and kicked off the Electronics Resurgence Initiative (ERI), the nation's largest investment in the foundation of electronics. Also, as office director, he helped structure and authorize the Spectrum Collaboration Challenge (SC2), the first DARPA RF grand challenge, continuing his focus on adaptive and collaborative RF systems. As a program manager at DARPA, he led efforts on adaptive and high-performance RF systems. He developed the arrays at commercial timescales (ACT) and managed the Adaptive RF Technologies (ART) portfolio. These activities led to next generation RF components and systems, such as the RF FPGA, and ultra-high-speed digitizers for direct RF sampling. Prior to his DARPA appointment, Dr. Chappell served as a professor in the Electrical and Computer Engineering Department of Purdue University, where he led the Integrated Design of Electromagnetically Applied Systems (IDEAS) Laboratory. Dr. Chappell's research focused on high-frequency components, specifically the unique integration of RF and microwave components based on electromagnetic analysis. Dr. Chappell is the recipient of numerous research and teaching awards. He received his Bachelor of Science (summa cum laude), Master of Science, and Doctor of Philosophy degrees in Electrical Engineering, all from the University of Michigan.

KAILASH GOPALAKRISHNAN

IBM Fellow and Sr. Manager, Accelerator Architectures and Machine Learning

The precision scaling powered performance roadmap for AI Inference and Training systems

Tuesday, December 7 | 1:00 pm – 1:45 pm

Over the past decade, Deep Neural Network (DNN) workloads have dramatically increased the computational requirements of AI Training and Inference systems ≠ significantly outpacing the performance gains obtained traditionally using Moore's law of silicon scaling. New computer architectures, powered by low precision arithmetic engines (FP16 for training and INT8 for Inference), have laid the foundation for high performance AI systems ≠ however, there remains an insatiable desire for AI compute with much higher power-efficiency and performance. This talk will outline some of the exciting innovations as well as key technical challenges – that can enable systems with aggressively scaled precision for inference and training, while fully preserving model fidelity.This talk will also highlight some key complementary trends, including 3D stacking, sparsity and analog computing, that can enable dramatic growth in the AI system capabilities over the next decade.

Kailash Gopalakrishnan is an IBM Fellow and a senior manager of the accelerator architectures and machine learning group at the IBM T. J. Watson Research Center, where he has worked in the areas of computer architecture, deep learning, semiconductor devices, circuit design and emerging memory devices. Over the past decade, his primary research has centered around the invention and development of specialized platforms that have dramatically improved industry-wide AI systems' performance and revolutionized the incorporation of AI capabilities within IBM Systems. He has a Ph.D. in Electrical Engineering from Stanford University and his current research interests include accelerator microarchitectures, machine learning and approximate computing.

SAM NAFFZIGER

Senior Vice President, Corporate Fellow, and Product Technology Architect, AMD

Cross-Disciplinary innovations Required for the Future of Computing

Wednesday, December 8, 2021 | 1:00 pm – 1:45 pm

With traditional drivers of compute performance a thing of the past, innovative engineers are tapping into new vectors of improvement to meet the world's demand for computation. Like never before, the future of computing will be owned by those who can optimize across the previously siloed domains of silicon design, processor architecture, package technology and software algorithms to deliver performance gains with new capabilities. These approaches will derive performance and power efficiency through tailoring of the architecture to particular workloads and market segments, leveraging the much greater performance/Watt and performance/area of accelerated solutions. Designing and verifying multiple tailored solutions for markets where a less efficient general purpose design formerly sufficed can be accomplished through modular architectures using 2.5D and 3D packaging approaches. Delivering on modular solutions for high volume markets requires simultaneously optimizing across packaging, silicon, interconnect technologies where in the past, silicon design was sufficient. This talk will cover these trends with the vectors of innovation required to deliver these next generation compute platforms.

Samuel Naffziger is AMD senior vice president, Corporate Fellow, and Product Technology Architect. Naffziger works across the company to optimize product technology choices and deployment with a continued focus on driving best practice power/performance/area methodology to maximize product competitiveness, efficiency, and cost. Naffziger has been the lead innovator behind many of AMD's low-power features and chiplet architecture. He has over 32 years of industry experience with a background in microprocessors and circuit design at Hewlett Packard, Intel and AMD. Naffziger received a Bachelor of Science degree in Electrical Engineering from the California Institute of Technology (CalTech) and a Master of Science from Stanford. Naffziger holds more than 130 U.S. patents in the field and authored dozens of publications and presentations on processors, architecture and power management. He is an IEEE Fellow.

TECHTALK PRESENTATIONS

SERGE LEEF

Program Manager, Defense Advanced Research Projects Agency (DARPA)

Reimagining Digital Simulation

Monday, December 6, 2021 | 11:30 am – 12:30 pm

In the last few decades, digital event-driven simulation has largely relied on underlying hardware for performance gains; core algorithms have not undergone truly transformative changes. Past efforts to accelerate simulation with special purpose hardware has repeatedly fallen behind the ever-improving performance of general-purpose computers, enabled by Moore's Law. Emulation-based strategies have also reached a performance ceiling. We are now at the end of the road with Moore's Law, and the time is right to fundamentally rethink simulation algorithms, methodologies, and computational strategies: considering hyperscaling, facilitated by the cloud, and advances in domain specific computing. This talk will examine the past and a possible future of simulation, a key technology enabler for advanced chip designs.

Serge Leef joined DARPA in August 2018 as a program manager in the Microsystems Technology Office (MTO). His research interests include computer architecture, chip design tools, simulation, synthesis, semiconductor intellectual property (IP), cyber-physical modeling, distributed systems, secure design flows, and supply chain management. He is also interested in the facilitation of startup ecosystems and business aspects of technology.

NEERAJ KAUL

Vice President of Engineer, Digital Design Group, Synopsys

Delivering Systemic Innovation to Power in the Era of SysMoore

Monday December 6, 2021 | 3:00 pm – 4:00 pm

The SysMoore era is characterized by the widening gap between what is realized through classic Moore's Law scaling and massively increasing system complexity. The days of traditional System-on-a-chip complexity are giving way to systems-of-chips complexity, with the continued need for smaller, faster, and lower-power process nodes coupled with large-scale multi-die integration methodologies to coalesce new breeds of intelligence and compute, at scale. To enable such systems, we need to look beyond targeted but piece-meal innovation to something much broader and more able to deliver holistically and on a grander scale.

Systemic thinking coupled with systemic innovation is key to addressing both prevailing and future industry challenges and approaching them comprehensively is necessary to deliver the technological and productivity gains demanded to drive the next wave of transformative products.

This presentation will outline some of the myriad prevailing challenges facing designers in this era of SysMoore and the systemic innovations across the broad, silicon-to-software spectrum to address them. Join us to learn, how a combination of intelligent, autonomous, and analytics-driven design, is paving the way to reliable, autonomous, always-connected vehicles and how this hyper-integrated approach to innovation is being deployed to deliver the secure, AI-enabled, multi-die HPC compute systems of tomorrow. And much more!

Neeraj Kaul is the VP of R&D at Synopsys leading Physical Design R&D team and ICCII product and is a member of Platform R&D team. Neeraj has spent over 20 Years serving EDA industry in the areas of Physical Design and Implementation, Placement, Clock Synthesis, Floorplanning, Simulation, Timing , Optimization and Abstraction. Neeraj holds B.Tech from IIT, Delhi, Ph.D. from Vanderbilt University, both in Electrical Engineering. Neeraj has over 10 journal and conference publications and holds 4 US patents.

MICHAEL JACKSON

Corporate VP - Reasearch & Development, Cadence Design Systems, Inc.

More than Moore and Charting the Path Beyond 3nm

Tuesday, December 7, 2021 | 11:30 am – 12:30 pm

For more than fifty years, the trend known as Moore's Law has astutely predicted a doubling of transistor count every twenty-four months. As 3nm technology moves into production, process engineers are feverishly working to uphold Moore's Law by further miniaturizing the next generation of semiconductor technology. Meanwhile, a second trend referred to as "More than Moore" was coined in 2010 to reflect the integration of diverse functions and subsystems in 2D SoCs and 2.5D and 3D packages. Today, the trends of Moore's Law and "More than Moore" synergize to produce ever higher value systems.

Working together, advances in both process technology and electronic design automation (EDA) have driven fundamental evolutions behind these two important semiconductor trends. This talk will examine the amazing and innovative developments in EDA over the years, culminating in the era of 3DIC and Machine Learning-based EDA to chart the path to 3nm and More than Moore.

Michael Jackson joined Cadence in 2019 and is a Corporate Vice President of R&D in the Digital and Signoff Group where he leads Cadence's electrical and physical signoff products. He joined Synopsys in 2002 and led engineering for their synthesis, test and physical design products and later led marketing, business development and strategy for Synopsys' Design Group. Prior to joining Synopsys, he led engineering for Avant!'s physical design and simulation product lines and he also led the design technology group in Motorola's Semiconductor Products Sector. Michael earned a BS in Electrical Engineering from the University of Arizona and a Ph.D. in Electrical Engineering and Computer Sciences from the University of California at Berkeley.

STEVE RODDY

VP, Machine Learning Group, Arm Ltd.

The AI Hype Cycle is Over. Now What?

Wednesday, December 8, 2021 | 11:30 am – 12:30 pm

The expectations around AI and ML have been enormous, which fueled investment and innovation as companies scrambled for scalable approaches to building and deploying AI and ML solutions. Experimentation, in both hardware and software, has been the order of the day:

- Ramping up the core technology to improve accuracy and take on more use cases.
- Experimenting with the technology (models and processors) to understand what was possible, what worked, what didn't and why.

The exuberance of the moment, however, created some unintended consequences. Take, for example, a fully parameterized, complex Transformer network. In an analysis by Northeastern University, the 300 million parameter model took 300 tons of carbon to train. Since then, accuracy and efficiency have improved gradually. Today, as the shouting dies down, the biggest trend – one that is having profound effects in helping teams innovate – is around hardware. The days of general-purpose hardware anchoring AI and ML are quickly giving way to specialized compute that allows engineers to not only tune their solutions for accuracy and efficiency but deploy their solutions more effectively across the compute spectrum. Industry veteran Steve Roddy, head of AI and ML product for Arm, will describe how a new era of democratized design is accelerating innovation in AI and design teams who embrace are speeding ahead of the pack.

Steve Roddy began his career as an engineer in the 1980s, designing supercomputer processors. With over 20 years' experience in the semiconductor IP business, at companies including Tensilica and Cadence, he holds patents in cell library architecture and analog design.

IN MEMORIAM

Edmund M. Clarke

July 7, 1945 – December 22, 2020

Mr. Clarke was best known for his work in model checking, an automated method for detecting design errors in computer hardware and software. In the early 1980s, Mr. Clarke and his Harvard University graduate student, E. Allen Emerson — as well as Joseph Sifakis of the University of Grenoble, who was working separately — developed model checking, which has helped to improve the reliability of complex computer chips, systems and networks. For their work, the Association for Computing Machinery gave the three scientists the prestigious A.M. Turing Award — computer science's Nobel Prize — in 2007.

Mr. Clark's citation on the Turing Award website said Microsoft and Intel and other companies use model checking to verify designs for computer networks and software. Model checking allowed engineers to analyze the logic beneath a design similar to how a mathematician uses a proof to determine that a theorem is correct, according to CMU. It considers every possible state of a hardware or software design and determines if it is consistent with the designer's specifications.

Mr. Clarke joined the computer science faculty at CMU in 1982. In 1995, was the first recipient of an endowed chair in the School of Computer Science called the FORE Systems Professorship.

Nick English

1950 – February 2021

Nick was a long-term member of the semiconductor and EDA communities. He began his career at Harris Semiconductor, where he did pioneering work in transistor modeling. Nick also worked at Cadence, Conexant and Si2, where he was vice president of development until his retirement in 2014.

Charles Geschke

1939 – 2021

Geschke was working at Xerox's Palo Alto Research Center in the 1970s when he began developing the computer language Interpress, which was intended to provide high quality printing. When Xerox wasn't interested in moving forward with Interpress, Geschke and his colleague John Warnock left the company and founded Adobe Inc. There, they reworked Interpress into PostScript. Working together with Steve Jobs (1955–2011), they incorporated PostScript into Apple's LaserWriter printer. The combination became the first desktop publishing software, leading to a revolution in the printing industry. Adobe's other notable software includes Acrobat, Flash, and Illustrator. As Adobe grew, Geschke served as its COO and then president until his 2000 retirement, though he remained co-chairman of the board until 2017. He was awarded the National Medal of Technology and Innovation by President Barack Obama in 2008. Geschke, was an ACM Fellow and received the Computer Entrepreneur Award from IEEE.

Aaron Grenat

1975 – September 2021

Grenat graduated with honors from Purdue University. After graduation he moved to Austin, Texas where he officially began his career as an electrical engineer for Advanced Micro Devices (AMD). At AMD worked in physical design, clocking and power management and received several promotions and earned several patents.

IN MEMORIAM

James Hogan

November 25, 1951 –
February 27, 2021

Jim is noted as an industry investor, mentor, benefactor, and philanthropist. He was a man who genuinely cared about many individuals and humankind. He touched many lives on a day to day basis, from his international business colleagues to the people he worked shoulder to shoulder with on personal projects. Jim graduated from WC Overfelt high school in 1969and was a proud graduate of San Jose State University. He graduated with a Bachelor of Science degree in Computer Science/ Mathematics and later earned an MBA. Jim's involvement with San Jose State University went far beyond his graduation. He donated and participated in the progression of the engineering department, even being chosen as the keynote speaker at an engineering graduation ceremony.

Many who knew him described Jim as the "heart and soul" of the chip tool EDA and IP industry. The catchphrase heard so often around Silicon Valley was, "You should talk to Jim". And they were right. His insights, experience in all aspects of the EDA and IP industries, and connections made him the "go-to" person to know.

In addition to serving as a startup investor, advisor, or board member for over 20 startups during his long tenure in the semiconductor EDA space, Jim also founded the **Heart of Technology** project to give back to the community. Since 2009, the Heart of Technology has raised over $200,000 to benefit charities and nonprofits in need. In addition to his professional work, Jim loved modern and classic cars, collecting and fixing them as much as he could. Jim also loved music. Throughout his life he was a member of many different bands. In his home he dedicated a room to playing music and his collection of instruments. He had played several notable venues including House of Blues and The Fillmore. Some of his closest bonds were made through the comradery of musicianship and they lasted a lifetime.

Chung Laung (Dave) Liu

1934 – 2020

Dr. C. L. Liu was an internationally renowned pioneer and educator in IT sciences. He received countless awards for his outstanding contributions in numerous fields including computer-aided design and discrete mathematics. Also, his selfless mentorship produced many distinguished talents in academia and industries. In addition to these enormous achievements, Dr. Liu was also a passionate lover of poetry, a strong advocate for humanities, and a lifelong learner. He could quote Shakespeare when explaining AI and draw the connection between the poems of Microsoft Xiaoice and love letters of Tang Bohu. All in all, Dr. Liu epitomized the ideal of understanding the present by studying the past.

Alice Recoque

1929 – 2021

Alice Recoque had led the development of the Mitra 15 minicomputer, marketed in the 1970s. A graduate of the Higher School of Physics and Industrial Chemistry (ESPCI), she led the development of the Mitra 15 minicomputer, designed as part of the Calculus plan desired by General de Gaulle. Marketed since 1971, the Mitra 15 controlled robots or security systems in nuclear power plants, piloted missiles or ships, and calculated scientific experiments. More than 8,000 units have been sold. Recoque was also one of the first French scientists to be interested in artificial intelligence. In 1985, she was appointed to lead the AI mission at Bull. The engineer also participated in the founding meeting of the CNIL in 1978.

IN MEMORIAM

Prof. Dr. Wolfgang Rosenstiel

1954 – 2020

Prof. Rosenstiel was an established professor and directing chair for computer engineering department and dean of the Faculty of Science at the University of Tübingen. In these and many other roles, he worked with admirable enthusiasm and principle up until his passing. In the recent years, he also played a major role in the positive development of both the faculty and department. Prof. Rosenstiel, is recognized as a highly esteemed colleague, an outstanding scientist and teacher, and a forward-looking and highly committed leader.

As a researcher, he was significantly involved in shaping the German research landscape in electronic design automation. Prof. Rosenstiel was one of the pioneers in synthesizing digital circuits from algorithmic specifications. His research activities in the 1980s resulted in the high-level synthesis tool “Carlsruhe Digital Design sYstem (CADDY)” and the hardware description language “Digital Specification Language (DSL)”. CADDY was one of the world’s earliest high-level synthesis systems for automated synthesis of digital hardware, such as microprocessors, from program-like behavioral descriptions. The high performance and the potential productivity benefits of the approach resulted in an early commercialization by Siemens Semiconductor (CALLAS). Later, he advocated the establishment of SystemC as a system-level language for virtual prototyping. As he broadened his interests, he proposed a highly reliable coarse-grained reconfigurable computer architecture, as well as system-on-chip platforms that can autonomously adapt to changing operating conditions. Since the early 1990s, Prof. Rosenstiel produced progressive research on optimized usage of machine learning techniques in various technical and medical applications. He recognized early on the importance of machine learning for intelligent prosthesis control and brain computer interfaces.

Don Thomas (Donald Earl Thomas, Jr. PhD)

1951-2020

Don Thomas earned his PH.D. in computing engineering in 1977 from Carnegie Mellon University where he served in various teaching and professor roles in electrical and computer engineering (ECE) until his retirement in 2016. A published author many times over, Don’s technical journal papers and textbooks have had a profound influence in electrical and computer engineering at Carnegie Mellon and other institutions. It is estimated that Don positively influenced every electrical and computer engineering student at Carnegie Mellon University since the late 1970s. A dedicated colleague, mentor, and friend, Don Thomas’ legacy will live on in the faculty and students who worked with him.

DAC AWARDS AND SCHOLARSHIPS

2021 DAC Under-40 Innovators Award

In recognition for technical contributions of notable impact in the field of design and automation of electronic circuits and systems.

Anna-Katrina Shedletsky, CEO & Co-Founder, Instrumental

Dr. Jason Oberg, Co-Founder and CTO, Tortuga Logic

Tung-Chieh Chen, Chief Executive Officer (CEO), Maxeda Technology Inc.

Ying Wang, Associate Professor, Institute of Computing Technology, Chinese Academy of Sciences

2021 Marie R. Pistilli Women in Engineering Achievement Award

For displaying equality, diversity, and acceptance while visibly helping to advance women in electronic design.

Renu Mehra, Group Director, R&D, Digital Design Group, Synopsys

P.O. Pistilli Undergraduate Scholarship for Advancement in Computer Science and Electrical Engineering

Devonte Billings

IEEE/CEDA

2021 Phil Kaufman Award for Distinguished Contributions to ESD Hall of Fame Inductee

Jim Hogan

2021 Phil Kaufman Award for Distinguished Contributions to ESD Hall of Fame Inductee

Ed McCluskey

IEEE CEDA Outstanding Service Award

For outstanding service to the EDA community as DAC General Chair in 2020.

Zhuo Li, Cadence Design Systems, Inc.

IEEE Fellow

For contributions to quantum circuit synthesis and optimization, and compiling for quantum computers.

Dmitri Maslov, IBM

IEEE Fellow

For contributions to hardware intellectual property protection and security.

Gang Qu, University of Maryland

IEEE Fellow

For contributions to energy efficiency of computer systems.

Yung-Hsiang Lu, Purdue University

IEEE Fellow

For contributions to system-on-chip validation and design automation of embedded systems.

Prabhat Mishra, University of Florida

IEEE/ACM A Richard Newton Technical Impact Award in Electronic Design Automation

John A. Waicukauski, Synopsys

Eric Lindbloom, IBM (retired)

Barry K. Rosen, IBM Research Division (retired)

Vijay S. Iyengar, IBM (retired)

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems Donald O. Pederson Best Paper Award

DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement

Authors: **Yibo Lin**; **Zixuan Jiang**; **Jiaqi Gu**; **Wuxi Li**; **Shounak Dhar**; **Haoxing Ren**; **Brucek Khailany**; **David Z. Pan**

Hardware/Software Co-Exploration of Neural Architectures

Authors: **Weiwen Jiang**; **Lei Yang**; **Edwin Hsing-Mean Sha**; **Qingfeng Zhuge**; **Shouzhen Gu**; **Sakyasingha Dasgupta**; **Yiyu Shi**; **Jingtong Hu**

ACM/SIGDA

2021 ACM Todaes Best Paper Award

Authors: **Sumit K. Mandal, Ganapati Bhat, Janardhan Rao Doppa, Partha Pratim Pande**, and **Umit Y. Ogras**

Title: An Energy-Aware Online Learning Framework for Resource Management in Heterogeneous Platforms

Publication: Volume 25, Issue 3, Article No 28, May 2020.

ACM SIGDA Distinguished Service Award

Deming Chen, University of Illinois Urbana-Champaign, for distinguished contributions to the design automation and reconfigurable computing communities.

Evangeline F. Y. Young, Chinese University of Hong Kong, for outstanding leadership in promoting diversity in the ACM/SIGDA community.

ACM SIGDA Outstanding New Faculty Award

Zheng Zhang, University of California, Santa Barbara.

ACM FELLOW

Yiran Chen, Duke University, for Contributions to Nonvolatile Memory Technologies.

ACM SIGDA Outstanding Ph.D. Dissertation Award

Ahmedullah Aziz, for his dissertation "Device-Circuit Co-Design Employing Phase Transition Materials for Low power Electronics", Purdue University, Advisor: Sumeet Gupta.

SIGDA Pioneering Achievement Award

For pioneering and fundamental contributions to manufacturing testing and fault-tolerant operation of computing systems.

Prof. Jacob A. Abraham, UT Austin

SIGDA Service Award

Bei Yu, Chinese University of Hong Kong, for service as SIGDA Web Chair from 2016 to 2021, SIGDA Student Research Competition Chair in 2018 and 2019, and other SIGDA activities.

Best Paper Award for TRETS in 2021

Kevin E. Murray, Oleg Petelin, Sheng Zhong, Jia Min Wang, Mohamed Eldafrawy, Jean-Philippe Legault, Eugene Sha, Aaron G. Graham, Jean Wu, Matthew J. P. Walker, Hanqing Zeng, Panagiotis Patros, Jason Luu, Kenneth B. Kent, and **Vaughn Betz**

"VTR 8: High-performance CAD and Customizable FPGA Architecture Modelling"

ACM Transactions on Reconfigurable Technology and Systems, Volume 13, Issue 2, June 2020

Systems Design Contest Winners

1st place

Team Name: **SkrSkr**

Team Members: **Zhiqi Zhou** (ShanghaiTech Univeristy), **Shaoyi Chen** (ShanghaiTech Univeristy), **Weixiong Jiang** (ShanghaiTech Univeristy), **Songyang Zhang** (ShanghaiTech Univeristy), **Qi Deng** (ShanghaiTech Univeristy), **Wen Chen** (Southeast University), **Jianwen Luo** (ShanghaiTech Univeristy), **Xinzhe Liu** (ShanghaiTech Univeristy), **Heng Yu** (University of Nottingham Ningbo China), **Yajun Ha** (ShanghaiTech Univeristy)

2nd place

Team name: **iSmart**

Team members: **Yao Chen** (Advanced Digital Sciences Center, Singapore); **Xinheng Liu** (University of Illinois at Urbana-Champaign); **Junhao Pan** (University of Illinois at Urbana-Champaign); **Prakhar Ganesh** (Advanced Digital Sciences Center (ADSC), Singapore); **Jinjun Xiong** (University at Buffalo, IBM); **Deming Chen** (University of Illinois at Urbana-Champaign, ADSC)

3rd place

Team name: **SJTU_microe**

Organization name: Shanghai Jiao Tong University

Team members: **Peidong Du** (School of Electronic, Information and Electrical Engineering, Shanghai Jiao Tong University), **Guochao Deng** (School of Electronic, Information and Electrical Engineering, Shanghai Jiao Tong University), **Yaoyao Kong** (School of Electronic, Information and Electrical Engineering, Shanghai Jiao Tong University), **Qin Wang** (School of Electronic, Information and Electrical Engineering, Shanghai Jiao Tong University), **Naifeng Jing** (School of Electronic, Information and Electrical Engineering, Shanghai Jiao Tong University), **Jianfei Jiang** (School of Electronic, Information and Electrical Engineering, Shanghai Jiao Tong University)

DAC PAVILION SCHEDULE

Sponsored by cadence

Level 2 Exhibit Hall, Booth #2260

Monday, December 6

10:15 am – 11:30 am

2021: INDUSTRY REPORT

Speakers: Joe Sawicki, Executive Vice President, IC EDA, Siemens

11:30 am – 12:30 pm

TECHTALK: REIMAGINING DIGITAL SIMULATION

Speaker: Serge Leef, VP, Machine Learning Group

In the last few decades, digital event-driven simulation has largely relied on underlying hardware for performance gains; core algorithms have not undergone truly transformative changes. Past efforts to accelerate simulation with special purpose hardware has repeatedly fallen behind the ever-improving performance of general-purpose computers, enabled by Moore's Law. Emulation-based strategies have also reached a performance ceiling. We are now at the end of the road with Moore's Law, and the time is right to fundamentally rethink simulation algorithms, methodologies, and computational strategies: considering hyperscaling, facilitated by the cloud, and advances in domain specific computing. This talk will examine the past and a possible future of simulation, a key technology enabler for advanced chip designs.

1:00 pm – 1:45 pm

SKYTALK: CLOUD & AI TECHNOLOGIES FOR FASTER, SECURE SEMICONDUCTOR SUPPLY CHAINS

Speaker: William Chappell, CTO, Azure Global

Semiconductors are deeply embedded in every aspect of our lives, and recent security threats and global supply chain challenges have put a spotlight on the industry. Significant investments are being made both by nation states and commercial industry, to manage supply chain dependencies, ensure integrity and build secure, collaborative environments to foster growth. These shifts provide unique opportunities for our industry. This talk blends insights and experiences from government initiatives and Azure's Special Capabilities & Infrastructure programs, to outline how Cloud + AI technologies, along with tool vendors, fabless semiconductor companies, IP providers, foundries, equipment manufacturers and other ecosystem stakeholders can contribute to building a robust, end-to-end, secure silicon supply chain for both commercial and government applications, while generating value for their businesses.

2:00 pm – 2:45 pm

PANEL: TRUST AND VERIFY

Moderator: Brian Santo, Editor in Chief, EEtimes

Panelist: Will Ruby, COO, FortifyIQ; Mike Borza, Principal Security Technologist, Synopsys; Prabhat Mishra, Professor, University of Florida

Overcoming costly and piecemeal approaches to pre-silicon side-channel attack vulnerability analysis and verification.

3:00 pm – 3:45 pm

TECHTALK: DELIVERING SYSTEMIC INNOVATION TO POWER IN THE ERA OF SYSMOORE

Speaker: Neeraj Kaul, Vice President of Engineering, Digital Design Group, Synopsys

The SysMoore era is characterized by the widening gap between what is realized through classic Moore's Law scaling and massively increasing system complexity. The days of traditional System-on-a-chip complexity are giving way to systems-of-chips complexity, with the continued need for smaller, faster, and lower-power process nodes coupled with large-scale multi-die integration methodologies to coalesce new breeds of intelligence and compute, at scale. To enable such systems, we need to look beyond targeted but piece-meal innovation to something much broader and more able to deliver holistically and on a grander scale.

Systemic thinking coupled with systemic innovation is key to addressing both prevailing and future industry challenges and approaching them comprehensively is necessary to deliver the technological and productivity gains demanded to drive the next wave of transformative products.

This presentation will outline some of the myriad prevailing challenges facing designers in this era of SysMoore and the systemic innovations across the broad, silicon-to-software spectrum to address them. Join us to learn, how a combination of intelligent, autonomous, and analytics-driven design, is paving the way to reliable, autonomous, always-connected vehicles and how this hyper-integrated approach to innovation is being deployed to deliver the secure, AI-enabled, multi-die HPC compute systems of tomorrow. And much more!

4:30 pm – 5:30 pm

GLADIATOR ARENA POSTER BATTLE

See the 2021 Designer, IP and Embedded Tracks Poster Gladiator finalist present their posters in a speed round. Attendees and judges vote for the best Poster Gladiator! Come to the Pavilion and cast your vote.

DAC PAVILION SCHEDULE

Sponsored by cadence

Level 2 Exhibit Hall, Booth #2260

Tuesday, December 7

10:15 am – 11:30 am

2021: INDUSTRY REPORT

Speakers: Jay Vleeschouwer, Griffin Securities

11:30 am – 12:30 pm

TECHTALK: CHARTING THE PATH TO 3NM & MORE THAN MOORE

Speaker: Michael Jackson, VP, Cadence Design Systems, Inc.

For more than fifty years, the trend known as Moore's Law has astutely predicted a doubling of transistor count every twenty-four months. As 3nm technology moves into production, process engineers are feverishly working to uphold Moore's Law by further miniaturizing the next generation of semiconductor technology. Meanwhile, a second trend referred to as "More than Moore" was coined in 2010 to reflect the integration of diverse functions and subsystems in 2D SoCs and 2.5D and 3D packages. Today, the trends of Moore's Law and "More than Moore" synergize to produce ever higher value systems.

Working together, advances in both process technology and electronic design automation (EDA) have driven fundamental evolutions behind these two important semiconductor trends. This talk will examine the amazing and innovative developments in EDA over the years, culminating in the era of 3DIC and Machine Learning-based EDA to chart the path to 3nm and More than Moore.

1:00 pm – 1:45 pm

SKYTALK: ARCHITECTURES AND MACHINE LEARNING

Speaker: Kailash Gopalakrishnan, IBM Fellow and Sr. Manager, Accelerator

Over the past decade, Deep Neural Network (DNN) workloads have dramatically increased the computational requirements of AI Training and Inference systems – significantly outpacing the performance gains obtained traditionally using Moore's law of silicon scaling. New computer architectures, powered by low precision arithmetic engines (FP16 for training and INT8 for Inference), have laid the foundation for high performance AI systems – however, there remains an insatiable desire for AI compute with much higher power-efficiency and performance. In this talk, I'll outline some of the exciting innovations as well as key technical challenges – that can enable systems with aggressively scaled precision for inference and training, while fully preserving model fidelity. I'll also highlight some key complementary trends, including 3D stacking, sparsity and analog computing, that can enable dramatic growth in the AI system capabilities over the next decade.

2:00 pm – 2:45 pm

PANEL: HOW SYSTEM COMPANIES ARE RE-SHAPING REQUIREMENTS

Moderator: Frank Schirrmeister, Sr. Group Director, Solutions & Ecosystem, Cadence Design Systems, Inc.

Panelists: Chris Bergey – Arm Ltd., SVP and GM, Infrastructure line of business; Rebecca Lipon Weekly – Intel, Vice President, GM, Hyperscale Strategy and Execution; Amir Salek – Google, Head of Silicon – Google Cloud and Infrastructure; Alex Starr – AMD, Corporate Fellow; Drew Wingard – Facebook, Director of SoC Enablement at Facebook Reality Labs

As predicted by Hennessy/Patterson in 2018, the electronics industry is entering an era of domain-specific architectures and domain-specific languages that enable hyperscale computing at never-before-seen complexity, advanced edge processing, and a new breed of consumer devices. As a result, industry verticals like automotive, consumer, mobile, networking, and data center compute are re-shaping to new vertical integration and specialization levels. For example, consumer devices will deliver new user experiences at form factors and power envelopes that were hard to imagine just years ago and will exist in a hyperconnected, always-on world. In addition, hyper-convergence for infrastructure in data centers re-balances memory, storage, network, and computing at never before seen pace. This panel will discuss the resulting new sets of EDA and System Analysis requirements, including new innovative approaches for 3DIC integration, Low-Power/Thermal and Electromagnetic Analysis, and enablement for workload-optimized server and AI/ML chips and systems across data centers, networks, edges, and consumer devices. The panel will also discuss the changes in the overall supply chain for data-center silicon and system development.

Level 2 Exhibit Hall, Booth #2260

Tuesday, December 7 cont.

3:00 pm – 3:45 pm

PANEL: HANDLING SOC VERIFICATION: CHANGING THE PARADIGM IN VERIFICATION APPROACHES

Moderator: Brian Bailey, Semiconductor Engineering
Panelists: Balachandran Rajendran, Dell EMC; Mike Chin, Intel Corporation; Adnan Hamid; Breker Verification Systems; Neil Hand, Siemens EDA

Modern SoC complexity is driving a new verification frontier. The verification of an SoC has always been a departure from the more standardized techniques employed in large block or sub-system, both in terms of test requirements as well as sheer complexity and size. However, new issues such as safety, security, processor instruction flexibility layered on top of advanced applications including 5G, AI, Quantum Computing, etc. have driven the need for different thinking.

Simulators, emulators and formal-based apps are essential tools in the verification teams' armament. But what is the most effective way to augment the core capabilities to deliver these intensely complex chips on time? For example, do we invest in accelerating test content production through techniques such as Portable Stimulus. Or should the focus be on additional and advanced static verification methods.

Moderator Brian Bailey, technology editor/EDA for Semiconductor Engineering, will lead two well-known, senior engineers who are responsible for next generation verification flow development. They will consider and discuss next generation needs and the directions they can take. Two vendor CEOs will attempt to address those needs and explain why their method is the most effective use of time and budget.

Come and witness an animated and lively discussion as we watch an open and frank conversation, often held behind closed doors in many semiconductor and electronic systems companies.

4:30 pm – 5:30 pm

GLADIATOR ARENA POSTER BATTLE

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DAC PAVILION SCHEDULE

Sponsored by cadence

Level 2 Exhibit Hall, Booth #2260

Wednesday, December 8

11:30 am – 12:30 pm

TECHTALK: THE AI HYPE CYCLE IS OVER. NOW WHAT?

Speaker: Steve Roddy, VP, Machine Learning Group, Arm Ltd.

The expectations around AI and ML have been enormous, which fueled investment and innovation as companies scrambled for scalable approaches to building and deploying AI and ML solutions. Experimentation, in both hardware and software, has been the order of the day:

- Ramping up the core technology to improve accuracy and take on more use cases.
- Experimenting with the technology (models and processors) to understand what was possible, what worked, what didn't and why.

The exuberance of the moment, however, created some unintended consequences. Take, for example, a fully parameterized, complex Transformer network. In an analysis by Northeastern University, the 300 million parameter model took 300 tons of carbon to train. Since then, accuracy and efficiency have improved gradually. Today, as the shouting dies down, the biggest trend – one that is having profound effects in helping teams innovate – is around hardware. The days of general-purpose hardware anchoring AI and ML are quickly giving way to specialized compute that allows engineers to not only tune their solutions for accuracy and efficiency but deploy their solutions more effectively across the compute spectrum. Industry veteran Steve Roddy, head of AI and ML product for Arm, will describe how a new era of democratized design is accelerating innovation in AI and design teams who embrace are speeding ahead of the pack.

1:00 pm – 1:45 pm

SKYTALK: CROSS-DISCIPLINARY INNOVATIONS REQUIRED FOR THE FUTURE OF COMPUTING

Speaker: Sam Naffziger, Senior Vice President, Corporate Fellow, and Product Technology Architect, AMD

With traditional drivers of compute performance a thing of the past, innovative engineers are tapping into new vectors of improvement to meet the world's demand for computation. Like never before, the future of computing will be owned by those who can optimize across the previously siloed domains of silicon design, processor architecture, package technology and software algorithms to deliver performance gains with new capabilities. These approaches will derive performance and power efficiency through tailoring of the architecture to particular workloads and market segments, leveraging the much greater performance/Watt and performance/area of accelerated solutions. Designing and verifying multiple tailored solutions for markets where a less efficient general purpose design formerly sufficed can be accomplished through modular architectures using 2.5D and 3D packaging approaches. Delivering on modular solutions for high volume markets requires simultaneously optimizing across packaging, silicon, interconnect technologies where in the past, silicon design was sufficient. This talk will cover these trends with the vectors of innovation required to deliver these next generation compute platforms.

2:00 pm – 2:45 pm

PANEL: DESIGN AND VERIFICATION ENGINEER 2.0 – A NEW GENERATION OF A PIPE DREAM?

Organizers: Sandeep Srinivasan, CEO, VerifAI Inc.

Moderator: John Blyler, Senior Editor for DesignNews

Panelist: Aman Joshi, Senior Director of Western Digital; Duaine Pryor, Ph.D., Chief Technologist , Siemens EDA; Sandeep Srinivasan, CEO VerifAI Inc.; Sashi Obilisetty, Synopsys

The tremendous advances in Integrated Circuit (IC) Design that have spawned amazing innovation have also increased the complexity of Design Verification (DV).

DV today takes up more than half the time and cost of designing an IC. Additionally, DV requires a significant amount of engineering talent, simply put, there just aren't enough DV engineers being produced to meet this demand.

To address the future challenges of verification, DV engineers must reinvent themselves and evolve into the DV Engineer 2.0. In this panel we will debate if ML/AI and Software 2.0 – the move toward a more abstracted way of designing electronics chips and systems – will play a role in helping the Design and Verification Engineer 2.0 to take on the challenge of reducing the cost and time of design and verification, while challenging the traditional Software 1.0 stack. Our debate will include the following areas:

- Deep Neural Network (DNN) Models and Software 2.0
- Functional Verification and Coverage improvement using ML
- Formal Verification
- Language models
- Machine Learning Model Deployment in Production
- How EDA companies need to evolve to meet these new challengers

With the proliferation of Software 2.0 and Machine Learning, will the Design and Verification Engineer 2.0 be twice as productive as they are today? Will they acquire the skill sets to model complex algorithms using Machine Learning Models and challenge traditional software 1.0 from EDA companies? We'll offer a multitude of expert perspectives.

4:30 pm – 5:30 pm

GLADIATOR ARENA POSTER BATTLE

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RESEARCH PANELS

The following panels were recorded prior to 58DAC, and will be available for viewing each day on the second floor mezzanine of Moscone West. Check the mobile app for presentation times.

Autonomous Robot Design: How Can EDA Help?

Organizer: Iris Bahar, Brown University

Moderator: Iris Bahar, Brown University

Panelists: Hadas Kress-Gazit, Cornell University; Sonia Chernova, Georgia Tech; Sabrina Neuman, Harvard University; Shaoshan Liu, Perceptin

The Robots are coming, and they are everywhere, but how can the electronic design automation community help? In this panel, we hear opinions from four expert researchers working in the robotics field. They will give their opinions on what they see as current trends in the use of autonomous robots, where they are headed, what they see as the biggest challenges in advancing the capabilities of autonomous robots, and how the EDA community can get involved.

Quantum Computing: An Industrial Perspective

Organizer: Michael Niemier, Notre Dame

Moderator: Robert Wille, Johannes Kepler University Linz

Panelists: Leon Stok, IBM; Krysta Svore, Microsoft; Austin Fowler, Google

The Robots are coming, and they are everywhere, but how can the electronic design automation community help? In this panel, we hear opinions from four expert researchers working in the robotics field. They will give their opinions on what they see as current trends in the use of autonomous robots, where they are headed, what they see as the biggest challenges in advancing the capabilities of autonomous robots, and how the EDA community can get involved.

Homomorphic Computing as a Foundational Technology: Theory, Practice, and Future Business

Organizer: Yiorgos Makris, The University of Texas at Dallas

Moderator: Mihalis Maniatakos, New York University

Panelists: Kurt Rohloff, Duality; Kim Laine, Microsoft Research; Ingrid Verbauwhede, KU Leuven

Come here from experts in industry and academia on the current status of homomorphic encryption as a foundational technology. The panelist will cover all levels, from hardware to compilers to software and to theory, and will also discuss the business ecosystem that may eventually arise around this technology.

Environmentally-Sustainable Computing

Organizer: Carole-Jean Wu, Facebook & Arizona State University

Moderator: Carole-Jean Wu, Facebook & Arizona State University

Panelists: Karen Strauss, Microsoft; Fahmida Bangert, ITRenew; David Brooks, Harvard University; Andrew Byrnes, Micron

The computing community faces many environmental challenges in the path toward sustainable computing. In this panel we will hear from experts from industry and academia as they discuss what is means to have environmental sustainability as a first design principle and how DAC participants and the broader community can help steer us toward an environmentally sustainable future.

WORKSHOP: PRIVACY AND SECURITY BY DESIGN & DEFAULT: UNDERSTANDING THE CONVERGENCE OF LAW, POLICY, AND TECHNOLOGY

Time: 8:00 am – 12:00 pm
Room: 3014
Event Type: Workshop

Organizer(s): Jordan Fischer, XPAN Law Group, LLC, Philadelphia, PA

Increasingly, each country, and even each state, is providing unique legal solutions to data privacy and security. For businesses that cross borders, both national and domestic, this creates distinct challenges to building effective solutions. These evolving privacy, security and technology requirements are impacting the growth and innovation within companies, requiring strategic decisions regarding risk, legal liability, and strategic planning.

Often, the concepts of security and privacy by design and by default are built into these legal requirements. But, understanding the requirements of the law, and translating those requirements into technological solutions can be challenging. This workshop will provide in-depth understanding of those legal requirements, and provide a framework to help the industry incorproate these core concepts of design within technology.

The Workshop will start with an overview of general privacy and security legal and policy principles, and then will focus on two key laws that are pushing the privacy and security laws: the European Union's General Data Protection Regulation ("GDPR") and the California Consumer Privacy Act of 2018 ("CCPA"). Using these laws, we will discuss case studies, and how to communicate, plan, and strategize on products and solutions that incorporate privacy and security requirements.

The Workshp will include both lecture and hands-on exercises. The goal is for attendees to take away tools and strategies to bring this conversation to their teams and departments.

WORKSHOP: EDA GROWTH ACCELERATES AS MOORE'S LAW SLOWS

Room: Level 3 Lobby
Event Type: Networking

Organizer: Charles Shi, PhD, Vice President, Research Analist, Needham & Company LLC

It may be counter-intuitive to argue that electronic design automation (EDA) industry could see accelerated growth because Moore's Law is slowing down. In this presentation, I will walk you through my reasons why such could be the case. We believe the slowing Moore's Law has led to design diversification with domain-specific chip designs replacing one-size-fits-all designs, has motivated systems companies to enter the silicon race, and has nurtured the recent renaissance of semiconductor startups. EDA, IP, and foundry are key enablers and beneficiaries of these trends. In addition, the slowing Moore's Law means chip-level scaling must be complemented with package- or system-level scaling, which creates a greater need for system design and analysis that will significantly expand the scope of EDA as well as its market size. We are convinced that the strong growth of EDA in 2020 and 2021 was not a "Covid phenomenon" but the beginning of a new era that will feature strong double-digit growth for the EDA industry. Last but not least, we believe EDA can play a key role in mitigating the global chip shortage that may last beyond 2022, as foundries push more designs migrating to sub-20nm nodes. We argue design migration to sub-20nm nodes is an underappreciated alternative to ease chip shortage other than massive capacity additions at 28nm and above.

Please note: Throughout the program you'll find sessions listed 'Combined Sessions'. Some of the presentations that were originally included in these session have shifted to virtual. During the 'Combined Session' you will see presentations from multiple different sessions that will span different tracks. The time listed next to each presentation will still be accurate, ensuring you are able to view the specific presentations you are interested in.

Visit the DAC Virtual Event at https://58dac.digitellinc.com/ starting December 13 to access remaining presentation recordings.

WORKSHOP: 2ND ROAD4NN WORKSHOP: RESEARCH OPEN AUTOMATIC DESIGN FOR NEURAL NETWORKS

Time: 8:00 am - 5:00 pm
Room: 3016
Event Type: Workshop

Organizer(s): Zhenman Fang, Simon Fraser University, Burnaby, Canada; Yanzhi Wang, Northeastern University, Boston, MA; Zhe Chen, University of California, Los Angeles, Los Angeles, CA

In the past decade, machine learning, especially neural network based deep learning, has achieved an amazing success. Various neural networks, such as CNNs, RNNs, LSTMs, BERT, GNNs, and SNNs, have been deployed for various industrial applications like image classification, speech recognition, and automated control. On one hand, there is a very fast algorithm evolvement of neural network models, almost every week there is a new model from a major academic and/or industry institute. On the other hand, all major industry giants have been developing and/or deploying specialized hardware platforms to accelerate the performance and energy-efficiency of neural networks across the cloud and edge devices. This include NVIDIA GPU, Intel Nervana/Habana/Loihi ASICs, Xilinx FPGA, Google TPU, Microsoft Brainwave, Amazon Inferentia, to name just a few. However, there is a significant gap between the fast algorithm evolvement and staggering hardware development, hence calling for broader participation in software-hardware co-design from both academia and industry.

In this workshop, we focus on the research open automatic design for neural networks, a holistic open source approach to general-purpose computer systems broadly inspired by neural networks. More specifically, we discuss full stack open source infrastructure support to develop and deploy novel neural networks, including novel algorithms and applications, hardware architectures and emerging devices, as well as programming, system, and tool support. We plan to bring together academic and industry experts to share their experience, discuss challenges they face as well as potential focus areas for the community. Below is the planed workshop content.

KEYNOTE: THE POTENTIAL OF MACHINE LEARNING FOR HARDWARE DESIGN

Jeff Dean, Google, Palo Alto, CA

8:45 am – 9:45 am

Room: 3008

In this talk Jeff will describe the tremendous progress in machine learning over the last decade, how this has changed the hardware we want to build for performing such computations, and describe some of the areas of potential for using machine learning to help with some difficult problems in computer hardware design. I'll also briefly touch on some future directions for machine learning and how this might affect things in the future.

Biography: Jeff Dean (ai.google/research/people/jeff) joined Google in 1999 and is currently a Google Senior Fellow and SVP for Google Research and Google Health. His teams are working on systems for speech recognition, computer vision, language understanding, and various other machine learning tasks. He has co-designed/implemented many generations of Google's crawling, indexing, and query serving systems, and co-designed/implemented major pieces of Google's initial advertising and AdSense for Content systems. He is also a co-designer and co-implementor of Google's distributed computing infrastructure, including the MapReduce, BigTable and Spanner systems, protocol buffers, the open-source TensorFlow system for machine learning, and a variety of internal and external libraries and developer tools.

Jeff received a Ph.D. in Computer Science from the University of Washington in 1996, working with Craig Chambers on whole-program optimization techniques for object-oriented languages. He received a B.S. in computer science & economics from the University of Minnesota in 1990. He is a member of the National Academy of Engineering, and of the American Academy of Arts and Sciences, a Fellow of the Association for Computing Machinery (ACM), a Fellow of the American Association for the Advancement of Sciences (AAAS), and a winner of the 2012 ACM Prize in Computing.

TUTORIAL: CLOSING THE HARDWARE SOFTWARE CODESIGN LOOP WITH OPEN SOURCE FLOWS

Time: 10:30 am – 12:00 pm
Room: 3000
Event Type: Tutorial
Topic Area(s): EDA

Recent trends in chip manufacturing resulting in a plateau in clock rates and peak power dissipation have made architecture specialization one of the most promising methods of achieving continued performance scaling. In concert with this, there has been significant growth in open-source hardware – both IP blocks as well as complete design flows. The RISC-V ISA with it's associated software stack and many of its implementations are excellent examples of how open-source designs can begin permeating many areas of the market. However, many of these implementations are targeted point design leaving hardware designers to face familiar challenges if they wish to customize. Multiple high-level synthesis techniques and more powerful HDLs, such as Chisel, address the hardware generation portion of customization but these techniques frequently do not include the ability to generate any of the required software required to program and use your customized processor. Going further, frequently a general-purpose processor, such as RISC-V based CPU, is only a small part of a system – many implementations require custom accelerators, integration of existing IP or tailored memory systems to achieve performance targets.

This tutorial will introduce participants to multiple open-source hardware development flows to demonstrate how they can be used to accelerate their own designs. This tutorial will leverage a powerful, open-source, hardware generation and co-design environment – OpenSoC System Architect to walk participants through the creation of a basic, RISC-V like processor complete with a tailored LLVM compiler. Participants will then be shown how to extend the base ISA with a custom instruction of their definition and then re-generate their processor and compiler with their new instruction support to create a tight, co-design loop with open-source tools. Simple kernels will be provided for participants to test their new compilers against.

As a demonstration of how designers may create custom systems that go beyond ISA extensions, we will demonstrate how to attach a custom, configurable, cache coherent memory system to your RISC-V based core through the Open2C plug-in for OpenSoC System Architect.

As an open-source tool, OpenSoC System Architect is designed to be customized and extended through the use of standard plug-in interfaces. Plug-ins allow a designer to incorporate their own custom IP blocks – including accelerators, memory systems, I/O devices, etc. into the OpenSoC System Architect design flow.

At the conclusion of this tutorial participants will have a good understanding of how to use open-source hardware development flows to create their own RISC-V based processors with custom extensions and how to design their own plug-ins to incorporate additional IP as their needs dictate.

Organizers: David Donofrio, Tactical Computing Laboratories, San Francisco, CA; John Leidel, Tactical Computing Laboratories, Muenster, TX

Presenters: David Donofrio, Tactical Computing Laboratories, San Francisco, CA ;Jeffrey Young, Georgia Institute of Technology, Atlanta, GA

TUTORIAL: REINFORCEMENT LEARNING IN DIGITAL SYSTEM SIMULATION

Time: 10:30 am – 12:00 pm
Room: 3018
Event Type: Tutorial
Topic Area(s): Machine Learning/AI

This tutorial discusses Reinforcement Learning (RL) and its application in the Digital Simulation domain. We will demonstrate a working case study of an agent deriving optimal stimulus using RL principles for a simple digital system.

We start by introducing the fundamentals of a Reinforcement Learning (RL) Framework agnostic of any particular domain. This includes the definition of the Agent, Environment, Actions and Cumulative Reward. We define the Markov property of states that will allow us to use Markov Decision Process (MDP) techniques to arrive at an optimal solution. We explore in detail one such method (Q-Learning) used in our case study.

We rigorously show how Digital Simulation can be treated as an RL episodic task with a discrete state space and a finite set of actions. The Stimulus RL agent starts with no knowledge of the environment and the desired goal of the stimulus is expressed as the cumulative reward in the RL framework. We implement Q-Learning to derive a table to map an optimal action for each state of the Digital System.

For our hands-on case study we will use an open-source environment based on Verilator and Cocotb. Verilator is an open-source System Verilog to C++ cycle-based simulator. Cocotb is a COroutine based Cosimulation TestBench environment implemented in Python for verifying VHDL and SystemVerilog RTL. All the code runs in a docker container that can be downloaded from docker hub

Our example is an N deep fifo and the goal of the stimulus agent is to alternate between filling and emptying the fifo as many times as possible in a 200 cycle interval. We derive a reward function that captures this goal. The set of actions for this design would be any combination of a fifo push or pop each clock cycle. The simulation will be run live to demonstrate how the agent learns optimal stimulus.

Lastly, we will tackle approaches to solving real world problems with large state spaces of the order of 10200. We demonstrate use of a Deep Q Network (DQN) to approximate this lookup. The advantage of having a test bench in python becomes apparent, since we leverage the PyTorch Machine Learning framework in building our DQN. We show how the DQN comes up with the same optimal policy as Q-Learning. We discuss possibilities for future work in this area, such as applying policy based methods and relaxing the strict Markov property requirement.

Organizers: Sananda Velacheri, Samsung, Austin, TX; Phillip Wagner, FOSSI Foundation, Halifax, United Kingdom

Presenters: Sananda Velacheri, Samsung, Austin, TX; Phillip Wagner, FOSSI Foundation, Halifax, United Kingdom

TUTORIAL: PRACTICAL APPLICATION OF AI/ML TO EDA PROBLEMS

Time: 10:30 am – 12:00 pm
Room: 3014
Event Type: Tutorial
Topic Area(s): EDA, Machine Learning/AI

In this tutorial, a cross-section of industry presenters will lead attendees through case studies of real applications. Our goal is to ease the path to AI/ML adoption in EDA by bridging education, openness, and trust gaps. Starting from generic concepts (neural networks, data representation, model training, and related software tools), we will develop step-by-step AI/ML flows geared towards solving concrete problems in parasitic estimation and analog design automation.This tutorial will update the EDA end-users and tool developers on current industry advances in AI/ML for EDA. The target audience is engineers and tool developers from industry and academia who want a practical guide to using AI/ML in their daily work. Each case study will include: why is this problem important, how to discover and label the EDA-data feature set, a demonstration of the ML methodology, and practical instruction for applying these methods.

Post-layout Parasitic Estimation – Use AI/ML to quickly and conservatively estimate post-layout parasitics (eg, capacitances) from pre-layout circuit netlists. This promises to provide a fast replacement for the time-consuming layout extraction step, which can significantly reduce the time it takes for an analog design to reach market.

Neural Network Based Analog Circuit Sizing – A neural network based analog circuit sizing engine will be built in a step-by-step approach. Using python ML libraries, a free circuit simulator, a free PDK and an unsized circuit schematic, a reference model for the miller amplifier will be trained. The model will be used to optimize the amplifier performance to meet target specifications. No proprietary data is needed for this tutorial.

Analog IC Layout Generation – An ML-augmented, automated approach which greatly simplifies analog layout generation. Using schematic netlist, along with foundry design rules as inputs, this flow will handle topology-based constraint extraction, optimization, as well as subsequent place and route (PnR) steps.

Organizers: Leigh Anne Clevenger, Terry Berke, Silicon Integration Initiative, Inc., Austin, TX

Presenters: Siddhartha Joshi, Brett W Shook, Intel Corporation, Hillsboro, OR; Boon Siang Cheah, Synopsys, Foxborough, MA; Ramy Iskander, Intento Design, Paris, France

TUTORIAL: ADDING MACHINE LEARNING TO THE MIX OF EDA OPTIMIZATION ALGORITHMS

Time: 10:30 am – 12:00 pm

Room: 3016

Event Type: Tutorial

Topic Area(s): EDA, Machine Learning/AI

Advances in computing power and the availability of big data have ignited innovations in EDA. These advances rely on efficient algorithms that can produce optimal results in a short period of time. Many of the existing algorithms take advantage of mathematical optimization techniques to improve their solution quality. These techniques can find optimal solutions and require some level of insight into the nature of the problem by the designer. However, mathematical optimization relies heavily on the developed models and is often not robust concerning the variations in the presence of large data sets. That is why machine learning and deep learning techniques have gained popularity. Machine learning techniques can solve large-scale problems efficiently once they are trained. These methods do not use traditional modelling approaches and are often not sufficiently understood.

The main purpose of this tutorial is to show how optimization and machine learning can be used in a virtuous cycle to use the data to develop better models and use the models to generate more data to improve the accuracy and robustness of our models and develop with more innovative methods to solve the very challenging problems we face today. We would also like to address the false dichotomy that it is either optimization or machine learning and show how by combining these two methods we can improve our results. We will demonstrate the application of this approach to several EDA problems including estimation models during placement, smart solution space exploration during synthesis and physical design, improving convergence of iterative algorithms by running an ML model on the solution from the previous iteration

In this interactive tutorial, we will discuss the algorithm-driven nature of the optimization techniques and compare that to the data-driven nature of the machine learning techniques. Then, we will discuss how optimization and ML can be made into a virtuous cycle to solve the problems of scaling both in numbers and transistor sizes. We will show some examples of EDA problems and how they have been solved using optimization, machine learning, or both.

Organizers: Laleh Behjat, University of Calgary, Calgary, Canada; Ismail Bustany, Xilinx, San Jose, CA

Presenters: Ismail Bustany, Xilinx, San Jose, CA; Andrew Kahng, University of California, San Diego, San Diego, CA; Padmini Gopalakrishnan, Xilinx, Hyderabad, India

TUTORIAL: ENABLING FV AND SIMULATION USING FUNCTIONAL SPECIFICATIONS: THE OPEN-SOURCE ILA METHODOLOGY

Time: 1:30 pm – 5:00 pm

Room: 3018

Event Type: Tutorial

Topic Area(s): Design

A major challenge in hardware design and verification (either FV or simulation based) is the lack of a functional specification that can be used in a consistent way for verification at different stages. In current flows, high-level C/C++/SystemC executable models are manually developed for early functional verification using simulation. However, these are based on informal specifications and often there is no way to guarantee that the final RTL matches these higher-level models. Further, it is hard to use formal verification (FV) with the RTL designs as the properties to be checked are difficult for the designers to manually provide and often far from complete.

Recent work has developed the Instruction-Level Abstraction (ILA) as a functional specification for modules that addresses the above gaps in the design and verification flow. The ILA model of a component is a functional model that defines the response of the component to commands at its interface. It is inspired by the Instruction Set Architecture (ISA) for processors which specifies the processor's functional response to each instruction in the form of updates to its architectural state. For a processor the architectural state is the state that is persistent across instructions. Similar to a processor, the ILA model specifies the architectural state of a component as the state that is persistent across its commands, and the response to a command (which is treated as an instruction for this component) in terms of the updates to this state. The ILA model is then used to automatically generate (i) a functional simulator and (ii) a set of properties for FV that checks the component's response to each command - and is thus complete in its coverage of the functional specification. This fills in important gaps in existing design and verification flows. One of the challenges in using FV for property verification is the scalability of the property-checking tools. We will then discuss the open-source, word-level, SMT-based model checker Pono which addresses this. This tutorial will walk through the ILA model specification and FV and simulation flows using this ILA model. We will demonstrate the use of the open-source ILA and Pono tools and design repository that have been developed to support these flows (https://upscale.stanford.edu/).

Organizer: Sharad Malik, Princeton University, Princeton, NJ; Clark Barrett, Stanford University, Stanford, CA

Presenters: Aarti Gupta, Hongce Zhang, Sharad Malik, Princeton University, Princeton, NJ; Clark Barrett, Stanford University, Stanford, CA

TUTORIAL: APPROXIMATE SYNTHESIS: STATE-OF-THE-ART AND FUTURE DIRECTIONS

Time: 1:30 pm – 5:00 pm
Room: 3014
Event Type: Tutorial
Topic Area(s): EDA

Approximate computing is an emerging paradigm that enables reduced design area and power consumption by relaxing the requirement for full accuracy. This paradigm is particularly attractive in applications where the underlying computation has inherent resilience to small errors, which include, among many others, machine learning, computer vision and signal processing. In circuit design, a major challenge is the capability to synthesize approximate circuits automatically, without manually relying on the expertise of designers. In this tutorial, we will (1) overview error metrics and error estimation methods, (2) overview all major methods devised to synthesize approximate circuits given their exact functionality, (3) provide video tutorials for available open-source approximate synthesis tools, and (4) discuss future prospects of approximate logic synthesis.

We will outline the importance of a preliminary error-modeling phase aimed at guiding Approximate Logic Synthesis (ALS) algorithms towards efficient solutions. We will discuss the state of the art approaches for error-modeling, along with their strengths and weaknesses. Available design and benchmark circuits will be overviewed together with their associated quality metrics.

For Approximate Logic Synthesis, we will provide a categorization of existing techniques illustrating the differences between netlist transformation, where a netlist is manipulated by modifying its structure, and Boolean rewriting, whereby the logic of the circuit is first captured in a formal Boolean representation that is modified to yield an approximate Boolean representation; this is, in turn, synthesized to a gate-based netlist. For the first category, we review four different techniques: (i) greedy heuristics for netlist pruning (ii) greedy heuristics for netlist manipulation (iii) stochastic netlist transformation; and (iv) exhaustive exploration for netlist pruning. For Boolean rewriting instead, we review the following techniques: (i) logic rewriting by Boolean optimization; (ii) logic rewriting by Boolean matrix factorization; (iii) logic rewriting by binary decision diagrams; and (iv) logic rewriting by and-inverter graphs. We will provide a quantitative comparison of the performance of some of existing ALS techniques.

Approximate High-Level Logic Synthesis (AHLS) focuses on the highest level of abstraction for ALS, where the function is described at behavioural level, such as in RTL Verilog or C language. We overview AHLS techniques that (i) identify acceptable reductions to numerical precisions, (ii) simplify arithmetic expressions, (ii) deploy approximate arithmetic instead of exact arithmetic units, and (iii) utilize mixed-precision loop control and loop perforation. We will show how machine learning methods based on genetic programming can be used to approximate gate- and RT-level circuits. As many candidate approximate circuits are automatically generated by these methods, it is essential to quickly evaluate these circuits in terms of approximation error and electrical parameters. State of the art methods effectively combining search algorithms and error evaluation will be discussed.

We will also provide an overview and video demos of existing open-source tools for approximate synthesis. In particular, we will overview (i) the BACS benchmark set, (ii) ABACUS, which is a tool for AHLS, (iii) BLASYS, which is a tool for ALS; (iv) Partition and Propagate, which is a tool for error estimation.

Organizers: Laura Pozzi, Università della Svizzera italiana, Lugano, Switzerland; Sherief Reda, Brown University, Providence, RI

Presenters: Sherief Reda, Brown University, Providence, RI; Kaushik Roy, Purdue University, West Lafayette, IN; Ilaria Scara, Università della Svizzera italiana, Lugano, Switzerland; Lukas Sekanina, Brno University of Technology, Brno, Czech Republic

TUTORIAL: FROM EDA TO TEES, SECURITY TOOLS FOR UNDERSTANDING AND MITIGATING SIDE-CHANNEL AND FAULT INJECTION ATTACKS

Time: 1:30 pm – 5:00 pm
Room: 3020
Event Type: Tutorial
Topic Area(s): EDA

In this tutorial, we aim to bring together a collection of high quality security tools and infrastructure (from open-source academic tools, to industry-level ones) to demonstrate attacks and side-channel vulnerabilities. Also, we demonstrate a memory model that enhances performance of processors while keeping them secure.

In the Internet of Things (IoT) era where electronic devices are prevalent, attackers readily have physical access to electronic devices. These electronic devices are subject to fault injection and side channel attacks, which can compromise the entire security of a system. For example, laser fault injection can perturb these devices by directly injecting faults into them to retrieve secrets or create catastrophic consequences and side-channel attacks can observe electrical properties of the target device to reveal confidential information. Electronic design automation tools that help facilitate security evaluation at design time are critically needed to protect against the attacks.

Trusted-execution environments (TEE), like Intel SGX, isolate user-space applications into secure enclaves without trusting the OS. Thus, TEEs reduce the trusted computing base, but add one to two orders of magnitude slowdown. The performance cost stems from a strict memory model, which we call the spatial isolation model, where enclaves cannot share memory regions with each other. A memory model that can improve the performance while still maintaining the level of security is essential.

The tutorial demonstrates three electronic design automation (EDA) tools against fault attacks and side channel attacks, and one novel fast and secure memory model. The first EDA tool is a framework that can both generate laser fault injection attacks and integrate hardware-based redundancy to a design. The second EDA tool provides various security evaluation accuracy levels at different design steps against side-channel attacks. The third EDA tool helps verify the resilience of an embedded system handling confidential information against side-channel attacks. The memory model called Elasticlave provides one to two orders of magnitude performance improvements over the previous model.

Organizer: Trevor Carlson, National University of Singapore, Singapore, Singapore

Presenters: Burin Amornpaisannon, National University of Singapore, Singapore, Singapore; Romain Poussier, Nanyang Technological University, Singapore, Singapore; Sylvain Guilley, Secure-IC, Rennes, France; Shweta Shinde, ETH Zürich, Zurich, Switzerland

TUTORIAL: CROSSBAR MEMORY SYSTEMS FOR MACHINE LEARNING: CIRCUITS, ARCHITECTURE, AND EVALUATION FRAMEWORKS

Time: 1:30 pm – 5:00 pm
Room: 3000
Event Type: Tutorial
Topic Area(s): Machine Learning/AI, Design

Traditional computing systems based on the von Neumann architecture are fundamentally bottlenecked by data transfers between processors and memory. The emergence of data-intensive workloads, such as machine learning (ML), creates an urgent need to address this bottleneck by designing computing platforms that utilize the principle of collocated memory and processing units. Such an approach, known as "in-memory computing," can potentially eliminate data movement costs by computing inside the memory array itself. Crossbars based on resistive nonvolatile memory (NVM) devices have shown immense promise in serving as the building blocks of in-memory computing systems for ML workloads. This is because their high density can lead to higher on-chip storage capacity, while they can also perform massively parallel, in situ matrix-vector multiplication (MVM) operations, thereby accelerating the main computational kernel of ML workloads. However, resistive crossbar-based analog computing is inherently approximate due to the device- and circuit-level nonidealities. Such non-idealities can significantly degrade the algorithmic efficacy of large-scale deep neural networks (DNNs) when mapped on NVM crossbars. Furthermore, the area and energy costs of peripheral circuits for conversions between the analog and digital domains can greatly diminish the intrinsic efficiency of crossbar-based MVM computation.

In this tutorial, we present a comprehensive overview of the emerging paradigm of computing using NVM crossbars for accelerating ML workloads. We describe the design principles of resistive crossbars, including the devices and associated circuits that constitute them. We discuss test-chip data illustrating device challenges as well as circuits and peripherals that address these challenges. We further discuss intrinsic approximations arising from the device and circuit characteristics and study their functional impact on the MVM operation. Next, we present an overview of spatial architectures that exploit the high storage density of NVM crossbars. We will discuss how compilers can be designed for memory mapping that address device variations as well as reduce the latency gap between arrays. Furthermore, we elaborate on evaluation frameworks to perform performance and functional simulation for large-scale DNNs mapped on NVM crossbars. The performance simulation framework evaluates hardware metrics such as energy, latency and area considering aforementioned spatial architectures. The functional simulation framework effectively captures device-circuit-architecture characteristics to evaluate the algorithmic performance of large-scale DNNs using resistive crossbar-based hardware. Finally, we discuss open challenges and future research directions that need to be explored in order to realize the vision of resistive crossbars as the building blocks of future computing platforms.

Organizer: Aayush Ankit, Microsoft, Sunnyvale, CA

Presenters: Aayush Ankit, Microsoft, Sunnyvale, CA; Arijit Raychowdhury, Georgia Institute of Technology, Atlanta, GA; Jing Li, University of Pennsylvania, Philadelphia, PA; Takashi Ando, IBM, Yorktown Heights, NY

TUTORIAL: DESIGN AND CONSUMPTION OF IPS FOR FAIL-SAFE AUTOMOTIVE ICS

Time: 1:30 pm – 5:00 pm
Room: 3016
Event Type: Tutorial
Topic Area(s): Design, EDA

Industry-leading innovations in automotive electronics has immensely contributed in the development of advanced safety mechanism resulting in exponential growth in the amount of electronics that is being added while at the same time it continues to challenge safety target. The usage of high quality automotive IP becomes extremely important in the success of automotive IC design. To comply with ISO26262 and zero DPPM test quality, IP providers and consumers need to consider the impact of functional safety on test. This has initiated an inevitable collaboration between functionally safe electronics developers and technology providers to accomplish unparalleled safety and integrity of automotive ICs.

This tutorial will focus on how both the creation and consumption of automotive IP, looking at the various technologies and methodologies that can be used to standardize and automate this process.

For IP creation we will be looking at the overall design flow and methodologies that can be used to create automotive-ready IP. Starting from the concept of SEooC^3, we will explain the challenges in creating a safety concept around a general purpose, commercial off-the-shelf IP component. We'll move on looking at what a reasonable tailoring of the ISO 26262 looks like for an IP and what are the critical activities in the path. We'll look at how the concept of traceability is challenged when defining a block that contributes to hundred, perhaps thousands of architectural features. For IP consumption we will discuss the challenges of using 3rd party IPs within Automotive SoCs. We will introduce the concept of IP screening and acceptance testing to ensure smooth integration at SOC level to guarantee zero DPPM and improved reliability. We will also look how this fits into the overall manufacturing challenges when taking the SOC from inception to low cost volume over a multi-year program.

Organizer: Lee Harrison, Siemens EDA, Newbury, United Kingdom

Presenters: Lee Harrison, Siemens EDA, Newbury, United Kingdom; Nilanjan Mukerjee, Siemens EDA, Wilsonville, OR; Ghani Kanawati, Arm Ltd., Austin, TX

TUTORIAL: DIGITALIZATION - THE RETURN TO OUTSIZE GROWTH FOR THE SEMICONDUCTOR INDUSTRY

Time: 10:15 am – 11:15 am
Room: DAC Pavilion
Event Type: Analyst Review

In just one short year, a decade of digitalization occurred across all industries fueled by innovation in the semiconductor industry. Dramatic growth occurred in use of the cloud, work from anywhere and telemedicine, while online collaborative tool usage increased a staggering 4000%.

Impressive as this all is, it is just the beginning of a massive reinvigoration of the semiconductor industry. Emerging new compute and telecom infrastructures, with IoT starting to deliver its long-promised value, coupled with new technologies such as artificial intelligence are reshaping the competitive landscape at break-neck speed. Despite valid concerns over trade wars, there is no doubt the semiconductor market is once again on a dramatic growth trajectory.

Presenter: Joe Sawicki, Executive Vice President, Siemens EDA

GETTING STARTED ON CLOUD PLAYBOOK

Thank You to Our Sponsor SIEMENS

Time: 10:30 am – 12:00 pm
Room: 2008
Event Type: Designer, IP and Embedded Systems Track Presentations
Topic Area(s): Cloud

Chair/Co-Chair: Derek Magill, (NTT Data)

This session focuses on how to build advocacy in your organization to leverage public cloud platforms to help accelerate throughput and time to market. In this session, we'll walk through the advocacy playbook, hear from a company that used those principles to get a proof of concept started, and end with a panel session with EDA on cloud experts.

Moderator: Preeth Chengappa, Microsoft

Panelists: Philip Steinke, AMD; Sridhar Panchapakes, Synopsys; Prashant Varshney, Microsoft Azure; Michael Hale, NVIDIA; Derek Magill, NTT Data

EMBEDDED SYSTEMS! PROJECTS AND SOLUTIONS

Time: 10:30 am – 11:30 am
Room: 2008
Event Type: Designer, IP and Embedded Systems Track Presentations
Topic Area(s): Embedded Systems

Chair/Co-Chair: Mark Kraeling (Wabtec)

Embedded systems have become a necessity in every aspect of our daily life. Embedded systems design and deployment pose significant challenges in the areas of compute, power, privacy, security, connectivity, scalability and reliability. DAC Embedded systems track brings together embedded system software developers, IC designers, security experts and product managers to analyze and discuss current and future trends in the embedded systems field. In this Embedded systems session we will be discussing the challenges in security, real-time software design, Machine learning hardware accelerators, and performance modeling software design challenges.

CHRISTMAS LIGHTS DISPLAYS AS EMBEDDED SYSTEMS

***James Roberts**, IBM, Austin, TX*

PERFORMANCE MODELING OF DIGITAL PROCESSING SYSTEMS

***Rajesh Chandra**, Northrop Grumman, Linthicum, MD; **Deepak Shankar**, Mirabilis Design Inc., Sunnyvale, CA*

SOC ARCHITECTURAL EXPLORATION FOR AI AND ML ACCELERATORS WITH RISC-V

***Simon Davidmann**, Duncan Graham, **Larry Lapides**, Man Wai (Manny) Wright, Imperas Software Ltd., Thame, United Kingdom*

TECH TALK: REIMAGINING DIGITAL SIMULATION

Time: 11:30 am – 12:30 pm
Room: DAC Pavilion
Event Type: Tech Talk

In the last few decades, digital event-driven simulation has largely relied on underlying hardware for performance gains; core algorithms have not undergone truly transformative changes. Past efforts to accelerate simulation with special purpose hardware has repeatedly fallen behind the ever-improving performance of general-purpose computers, enabled by Moore's Law. Emulation-based strategies have also reached a performance ceiling. We are now at the end of the road with Moore's Law, and the time is right to fundamentally rethink simulation algorithms, methodologies, and computational strategies: considering hyperscaling, facilitated by the cloud, and advances in domain specific computing. This talk will examine the past and a possible future of simulation, a key technology enabler for advanced chip designs.

Speaker: Serge Leef, DARPA, Washington, DC

SKY TALK: CLOUD & AI TECHNOLOGIES FOR FASTER, SECURE SEMICONDUCTOR SUPPLY CHAINS

Time: 1:00 pm – 1:45 pm
Room: DAC Pavilion

Semiconductors are deeply embedded in every aspect of our lives, and recent security threats and global supply chain challenges have put a spotlight on the industry. Significant investments are being made both by nation states and commercial industry, to manage supply chain dependencies, ensure integrity and build secure, collaborative environments to foster growth. These shifts provide unique opportunities for our industry.

This talk blends insights and experiences from government initiatives and Azure's Special Capabilities & Infrastructure programs, to outline how Cloud + AI technologies, along with tool vendors, fabless semiconductor companies, IP providers, foundries, equipment manufacturers and other ecosystem stakeholders can contribute to building a robust, end-to-end, secure silicon supply chain for both commercial and government applications, while generating value for their businesses.

Speakers: William Chappell, Azure Global, Redmond, VA

ALL ROUTES LEAD TO CLOSING TIMING

Thank You to Our Sponsor PERFORCE

Time: 1:30 pm – 2:10 pm (Combined Session)
Room: 2008
Event Type: Designer, IP and Embedded Systems Track Presentations
Topic Area(s): Back-End Design

Chair/Co-Chair: Greg Ford (Marvell Semiconductor)

This session focuses on how to build advocacy in your organization to leverage public cloud platforms to help accelerate throughput and time to market. In this session, we'll walk through the advocacy playbook, hear from a company that used those principles to get a proof of concept started, and end with a panel session with EDA on cloud experts.

METHODOLOGY FOR EARLY TIMING AND FLOORPLANNING CLOSURE IN CUSTOM CIRCUIT DESIGN

Geoffrey Wang, Philip M. Bassett,Tai Cao, Saiful Islam, Michael J. Lee, Ryan Myers, ***Hema Ramamurthy****, IBM, Austin, TX*

ROUTING LAYER RE-OPTIMIZATION IN PHYSICAL SYNTHESIS

Nancy Zhou, IBM Systems, Austin, TX; ***Lakshmi Reddy****, IBM Research, Yorktown Heights, NY; Alex Suess, Cindy Washburn, IBM Systems, Poughkeepsie, NY*

AGING TIMING ANALYSIS BASED ON EMPYREAN-XTIME

Qi Wei, Chenfei Wu, Sanechips Technology Co., Ltd, Nanjing, China; Jiayong Li, Keqing Ouyang, Sanechips Technology Co., Ltd, Shenzhen, China; Minghao Hu, Changxin Du, Empyrean Technology, Beijing, China; ***An-Jui Shey****, Empyrean Technology, San Francisco, CA*

HOW AI AND CLOUD ENABLE A VIRTUOUS CYCLE IN SILICON DESIGN AND MANUFACTURING

Thank You to Our Sponsor SIEMENS

Time: 3:30 pm – 5:00 pm
Room: 2010/2012
Event Type: Designer, IP and Embedded Systems Track Presentations
Topic Area(s): Machine Learning/AI

Chair/Co-Chair: Ambar Sarkar (NVIDIA)

Over the last few years, companies in the chip design space have rushed to adopt AI/ML enabled tools and technologies, built AI-powered flows and supported a thriving community of researchers and academicians. It is indeed rare to see a company that is not actively engaged in adopting AI. However, how ready are we to incorporate at scale? A recent study by McKinsey indicates steady gains in benefits from AI; but a lack of benefits at scale.

Cloud computing was well in place before the AI revolution; however, it has gained more prominence with the advent of AI-enabled use cases in automotive, IoT and image processing – to name a few.

Through three sessions, we will explore how the semiconductor industry's gains can be exponentially improved by adopting a cloud-based technology foundation for AI-related tasks pertaining to data ingestion, model training, inference, and model deployment.

Session Organizer: Sashi Obilisetty, Synopsys, Santa Clara, CA

Presenters: Hamid Shojaei, Amir Yazdanbakhash, Google, Mountain View, CA; Chandramouli Kashyap, Prateek Bhansali, Intel Corporation, Santa Clara, CA; Avishek Panigrahi; Sashi Obilisetty, Google, Santa Clara, CA

TRUST AND VERIFY. OVERCOMING COSTLY AND PIECEMEAL APPROACHES TO PRE-SILICON SIDE-CHANNEL ATTACK VULNERABILITY ANALYSIS AND VERIFICATION

Time: 2:00 pm - 2:45 pm
Room: DAC Pavilion
Event Type: DAC Pavilion Panels

Side-channel vulnerabilities strike fear into the hearts of design engineers – as well as corporate lawyers and executives. But analyzing and uncovering potential vulnerabilities can be costly and time-consuming. Existing EDA tool flows aren't adequate to meet the challenges, so analysis is typically performed after the first-silicon prototype tapeout. This requires expertise and can prompt expensive silicon re-spins. The clear and present danger of side channel attacks, and the lack of a robust EDA security analysis methodology are creating a critical need for dedicated physical attack simulation tools that can root out vulnerabilities before prototype.

Panelists will discuss the gaps and downsides of current and new tools as well as a path forward to timely, efficient, and thorough pre-silicon side-channel attack vulnerability analysis. How can you better secure your design without hampering your design schedule and cost? Bring your questions – it should be a lively discussion!

Moderator: Brian Santo, EETimes, Portland, OR

Panelists: Will Ruby, FortifyIQ, San Jose, CA ;Mike Borza, Synopsys, Ottawa, Canada ;Prabhat Mishra, University of Florida, Gainesville, FL

TECH TALK: DELIVERING SYSTEMIC INNOVATION TO POWER THE ERA OF SYSMOORE

Time: 3:00 pm – 3:45 pm
Room: DAC Pavilion
Event Type: Tech Talk

The SysMoore era is characterized by the widening gap between what is realized through classic Moore's Law scaling and massively increasing system complexity. The days of traditional System-on-a-chip complexity are giving way to systems-of-chips complexity, with the continued need for smaller, faster, and lower-power process nodes coupled with large-scale multi-die integration methodologies to coalesce new breeds of intelligence and compute, at scale. To enable such systems, we need to look beyond targeted but piece-meal innovation to something much broader and more able to deliver holistically and on a grander scale.

Systemic thinking coupled with systemic innovation is key to addressing both prevailing and future industry challenges and approaching them comprehensively is necessary to deliver the technological and productivity gains demanded to drive the next wave of transformative products.

This presentation will outline some of the myriad prevailing challenges facing designers in this era of SysMoore and the systemic innovations across the broad, silicon-to-software spectrum to address them. Join us to learn, how a combination of intelligent, autonomous, and analytics-driven design, is paving the way to reliable, autonomous, always-connected vehicles and how this hyper-integrated approach to innovation is being deployed to deliver the secure, AI-enabled, multi-die HPC compute systems of tomorrow. And much more!

Presenter: Neeraj Kaul, Synopsys

CHIP DESIGN AND CLOUD: THE GOOD, THE EMERGING, AND THE POTENTIAL

Thank You to Our Sponsor SIEMENS

Time: 3:30 pm – 5:00 pm
Room: 2008
Event Type: Designer, IP and Embedded Systems Track Presentations
Topic Area(s): Cloud

Chair/Co-Chair: Sashi Obilisetty (Synopsys)

In this first-of-its-kind session, you will hear multiple perspectives, from educators to researchers to practitioners on how they have leveraged cloud for their work. Cloud provides a foundational platform to accelerate silicon workflows by providing seemingly limitless capacities. Presentations in this session cover how cloud enabled enhanced delivery of academic courses, technologies to implement hybrid flows, real-world experience from a cloud-based foundry, cloud-native EDA tools or "EDA 3.0", and finally, workloads that see oversized benefits from cloud.

CLOUD INFRASTRUCTURE FOR REMOTE AND SCALABLE EDA HARDWARE TRAINING

*Matthew Morrison, University of Notre Dame, South Bend, IN; **Owain Jones**, Kevin Dobie, CMC Microsystems, Kingston, Canada*

THE REALITY AND OPPORTUNITIES OF SEMICONDUCTOR DESIGN ON THE CLOUD

***Taeil Kim**, Naya Ha, Jongho Kim, Kyungtae Do, Sangyun Kim, Samsung, Gyeonggi-do, South Korea*

UTILIZING THE CLOUD TO INCREASE LIBRARY CHARACTERIZATION THROUGHPUT AND REDUCE SCHEDULE BOTTLENECKS

*Kenneth Chang, Amazon, Santa Clara, CA; Dnyanesh Digraskar, Amazon, Austin, TX; Matthieu Fillaud, Siemens EDA, Grenoble, France; **Wei-Lii Tan**, Siemens EDA, Fremont, CA*

NEXA: CLOUD NATIVE PLATFORM FOR COLLABORATIVE HARDWARE LOGIC DESIGN IN STEP-WISE REFINEMENT IMPLEMENTATION FLOWS

***Arun Joseph**, IBM, Bangalore, India ;Sampath Baddam, Shashidhar Reddy, Balaji Pulluru, Pradeep Joy, Ajay Gopalakrishnan, Shiladitya Ghosh, IBM, Bangalore, India; Arvind Haran, Wolfgang Roesner, IBM, Austin, TX; Anthony Saporito, IBM, Poughkeepsie, NY*

NEW FILE SYSTEM TO AUTOMATICALLY "SPILL" WORKLOADS ACROSS DATACENTER AND CLOUD

*Alok Sinha, **Rajeev Prasad**, Jasmin Ajanovic, Spillbox, San Francisco, CA*

IP ENABLING THE INTENDED FUNCTION. THE UNLOVED IP

Time: 1:30 pm – 3:00 pm
Room: 2010/2012
Event Type: Designer, IP and Embedded Systems Track Presentations
Topic Areas: IP

Chair/Co-Chair: Randy Fish (Synopsys)

In a complex SoC today 20%+ of the die may be consumed by IP that does not contribute directly to the intended mission mode function of the design. Test, debug, monitoring, POR, system controllers, … all play a critical role and are becoming more available on the commercial market. Larger and mature companies have a long and deep history of developing in-house solutions. Many of these "unloved" IPs are now broadening their impact into the full lifecycle of the design including in-field use. Here how a complex AI chip from Esperanto uses Unloved IP as well as perspectives from two leading suppliers, Synopsys and Siemens.

Session Organizer: Randy Fish, Synopsys,

Speakers: Bill Orner, Allen Baum, Esperanto; Adam Cron, Synopsys; Hanan Moller, Andy Gothard, Siemens EDA

MONDAY DESIGNER, IP, AND EMBEDDED SYSTEMS POSTER GLADIATORS PRESENTATION

Thank You to Our Sponsor SIEMENS methodics by Perforce

Time: 4:30 pm – 5:30 pm
Room: DAC Pavilion

ENHANCED ANALYTICS AND REPORTING FOR TRIAGE AND SIGN-OFF TIMING

Richard Taggart, Kerim Kalafala, Nathaniel Hieter, Chris Cavitt, Charles Gates, Tom Guzowski, Harry Reindel, Charles Schmitter, IBM, Poughkeepsie, NY; SheshaShayee Raghunathan, IBM, Bangalore, India

SHIFT-LEFT POST-SILICON VERIFICATION WITH SPEED AND ACCURACY

Jitendra Aggarwal, Arm Ltd., Austin, TX

ENHANCED HYPERSCALING OF DATA CENTERS USING IN-CHIP MONITORING & SENSING FABRICS

Stephen Crosher, Synopsys, Plymouth, United Kingdom; Ramsay Allen, Synopsys, Devon, United Kingdom

A LOW COST, SCALABLE AND PREDICTABLE GATE LEVEL SIMULATION METHODOLOGY FOR GIGA-SCALE SOCS

Satish Kumar Rompicharla, Nilay R. Desai, Anil K. Jonnalagadda, Intel Corporation, Bangalore, India; Kundan Kumar, Intel Corporation, Santa Clara, CA

ROUTABILITY IMPROVEMENT METHODOLOGY USING MULTIPLE STANDARD CELLS WITH VARIOUS PIN LOCATION

Sua Lee, Joonyoung Shin, Hyung-Ock Kim, Sangdo Park, Jooyeon Kwon, Yeongyeong Shin, Yongcheul Kim, Sangyun Kim

A SCALABLE MULTICORE RISC-V GPGPU ACCELERATOR FOR HIGH-END FPGAS

Blaise Pascal Tine, Fares Elsabbagh

ABSTRACTION – AN EFFICIENT METHODOLOGY FOR RTL & LOW-POWER SIGNOFF IN SOC DESIGN

Rohit Sinha, Intel Corporation

TOWARDS MEASURING LAYOUT PATTERN COVERAGE: A MACHINE LEARNING APPROACH

Hui Fu, Intel Corporation

MONDAY DESIGNER, IP AND EMBEDDED SYSTEMS TRACK POSTERS

Thank You to Our Sponsor SIEMENS methodics by Perforce

Time: 5:00 pm – 6:00 pm
Room: Exhibit Hall Level 2
Event Type: Designer, IP and Embedded Systems Track Poster Networking Reception

ACCELERATING ADVANCED NODE RAMP UP AND ROBUST DESIGN ENABLEMENT FOR LEADING EDGE SOC DESIGNERS

*Dipto Thakurta, Pegah Hassanzadeh, Intel Corporation, Hillsboro, OR; **Joe Kwan**, Siemens EDA, Fremont, CA; Aliaa Kabeel, Sarah Rizk, Kareem Madkour, Marwa Shafee,Mostafa Alaa, Michael Beshara, Mohamed Ismail, Siemens EDA, Cairo, Egypt; Yuyang Sun, Siemens EDA, Bedminister, NJ; Jiechang Hou, Siemens EDA, Wilsonville, OR*

ACCELERATING STANDARD CELLS VARIATION-AWARE CHARACTERIZATION METHODOLOGY WITH MACHINE LEARNING TECHNIQUES

*Jean-Arnaud Francois, Etienne Maurin,Bastien Aghetti, STMicroelectronics, Crolles, France; Rajnish Garg, Honey Garg, STMicroelectronics, Greater Noida, India; Austin Shirley, Siemens EDA, Saskatoon, Canada; **Wei-Lii Tan**, Siemens EDA, Fremont, CA*

ACCURATE AND EFFICIENT HIGH-PERFORMANCE MEMORY MODELING FOR FULL-CHIP POWER NOISE ANALYSIS

***Arif Mirza**, NVIDIA, Austin, TX; Girish Deshpande, Santosh Santosh, NVIDIA, Santa Clara, CA; Karthik Srinivasan, Rithunraj Krishna, Ansys, San Jose, CA*

AMS VERIFICATION OF HBMPHY: CHALLENGES & SOLUTIONS – 12NM PROCESS NODE

*Vijaykumar Sankaran, Cadence Design Systems, Inc., Bengaluru, India; **Santosh Mahadeo Narawade**, Shrikant Dhongadi, openfive, Bengaluru, India*

BEYOND LINT

***Cedric Walravens**, ICsense, Leuven, Belgium*

DUAL FEATURE VECTOR HETERO GRAPH NEURAL NETWORK (DFV-GNN) BASED POST-LAYOUT PARASITIC ESTIMATION

***Sungwon Kim**, Intel Corporation, Portland, OR; Hui Fu, Intel Corporation, Austin, TX*

EARLY LAYOUT AREA AND PLS ESTIMATION BY DESIGNERS

*Akshita Bansal, Atul Bhargava, STMicroelectronics, Greater Noida, India; **Jonathan Longrigg**, Paul Clewes, Pulsic, Newcastle upon Tyne, United Kingdom; Christian Symmons, Pulsic, Bristol, United Kingdom*

END-TO-END SOLUTION FOR STRUCTURED IMPLEMENTATION OF HIGH-SPEED DATA BUSES

*Shubham Agarwal, **Subhadarshini Behera**, Dheeraj Tuteja, Shishir Saran Rai, Intel Technology India Pvt. Ltd., Bangalore, India*

INNOVATIVE TECHNIQUES TO ACCELERATE ERROR HANDLING VERIFICATION OF COMPLEX SYSTEMS

***Bhushan Parikh**, Peter Graniello, Neha Rajendra, Intel Corporation, Chandler, AZ*

MEMORY PERIPHERAL STANDARD CELL ARCHITECTURE OPTIMIZATION USING DTCO UNDER STRONG AREA RESTRICTION

***Seyong Ahn**, Joohan Kim, SungHwan Cho, SeungHyuk Kwon, Youngmin Kim, Younsik Park, Hyuckjoon Kwon, Jung Yun Choi, Samsung Electronics, Hwaseong-si, South Korea*

MODERNIZING A NATIONWIDE INDOOR/OUTDOOR PACKAGE SORTING SYSTEM

***Dale Hackathorn**, Comark, Milford, MA*

MULTI-CORE SYSTEM VERIFICATION USING UVM PORTABLE STIMULUS

*Gaurav Gupta, Arjun Singh, NXP Semiconductors Inc., Noida, India; Maninder Kumar, NXP Semiconductors Inc., Delhi, India; Ajay Sharma, NXP Semiconductors Inc., Novi, MI; **Vaibhav Kumar**, NXP Semiconductors Inc., Austin, TX*

PI SIGNOFF METHODS USED IN A 5NM INFO DESIGN

*Ping Ding,Junjie Chen,Keqing Ouyang, Sanechips Technology Co., Ltd, ShenZhen, China; Chang Zhao, Xin Yao, Yao Liu, **Sooyong Kim**, Ansys, Shanghai, China*

RESOLUTION OF VERIFICATION BOTTLENECK BY FUNCTIONAL COVERAGE AUTOMATION

*Shikhadevi Katharia, Kiran Malvi, Neil More, **Priyanka Gharat**, Silicon Interfaces, Mumbai, India*

RISC-V PROCESSOR VERIFICATION METHODOLOGY WITH DYNAMIC TESTBENCH FOR ASYNCHRONOUS EVENTS

*Simon Davidmann, Lee Moore, **Man Wai (Manny) Wright**, Imperas Software Ltd., Thame, United Kingdom*

SHIFT LEFT: NOVER POWER ANALYSIS METHOD FOR LARGE-SCALE AI PROCESSORS

*Ling Sun, Shixuan Que, Iluvatar, Shanghai, China; **Arindam Mitra**, Ansys*

UPDATING RISC-V MICROARCHITECTURE IN THE FIELD THROUGH MENTA CO-EXTENDED CORES AND CODASIP STUDIO

***Imen Baili**, MENTA S.A.S, Valbonne, France; **Zdeněk Přikryl**, Codasip, Brno, Czech Republic*

VERIFICATION METHODOLOGY FOR HIGH RESOLUTION HIGH SPEED CMOS IMAGE SENSOR SOC - LEVERAGING INNOVATIONS IN EDA TOOLS

*Abhinav Agarwal, Forza Silicon (Ametek Inc.), Pasadena, CA; **Sumit Vishwakarma**, Siemens EDA, Fremont, CA*

KEYNOTE: GPUS, MACHINE LEARNING, AND EDA

Bill Dally, NVIDIA, Stanford, CA

9:00 am – 9:45 am
Room: 3008

GPU-accelerated computing and machine learning (ML) have revolutionized computer graphics, computer vision, speech recognition, and natural language processing. We expect ML and GPU-accelerated computing will also transform EDA software and as a result, chip design workflows. Recent research shows that orders of magnitudes of speedups are possible with accelerated computing platforms and that the combination of GPUs and ML can enable automation on tasks previously seen as intractable or too difficult to automate. This talk will cover near-term applications of GPUs and ML to EDA tools and chip design as well as a long term vision of what is possible. The talk will also cover advances in GPUs and ML-hardware that are enabling this revolution.

Bill Dally joined NVIDIA in January 2009 as chief scientist, after spending 12 years at Stanford University, where he was chairman of the computer science department. Dally and his Stanford team developed the system architecture, network architecture, signaling, routing and synchronization technology that is found in most large parallel computers today. Dally was previously at the Massachusetts Institute of Technology from 1986 to 1997, where he and his team built the J-Machine and the M-Machine, experimental parallel computer systems that pioneered the separation of mechanism from programming models and demonstrated very low overhead synchronization and communication mechanisms. From 1983 to 1986, he was at California Institute of Technology (CalTech), where he designed the MOSSIM Simulation Engine and the Torus Routing chip, which pioneered "wormhole" routing and virtual-channel flow control. He is a member of the National Academy of Engineering, a Fellow of the American Academy of Arts & Sciences, a Fellow of the IEEE and the ACM, and has received the ACM Eckert-Mauchly Award, the IEEE Seymour Cray Award, and the ACM Maurice Wilkes award. He has published over 250 papers, holds over 120 issued patents, and is an author of four textbooks. Dally received a bachelor's degree in Electrical Engineering from Virginia Tech, a master's in Electrical Engineering from Stanford University and a Ph.D. in Computer Science from CalTech. He was a cofounder of Velio Communications and Stream Processors.

THE STATE OF EDA: A VIEW FROM WALL STREET

Time: 10:15 am – 11:15 am
Room: DAC Pavilion
Event Type: Analyst Review
Topic Area(s):

We will examine the financial performance and structure of the EDA industry from 2010 through 2020, as well as the material technical trends and requirements that have affected EDA business performance and strategies. In addition, we will examine the progression of semiconductor R&D spending. Lastly, we will examine how the market value of the publicly-held EDA companies has evolved and provide our EDA industry projections for 2021 through 2024.

Presenter: Jay Vleeschhouwer, Griffin Securities, New York City, NY

LEARN TO DESIGN BETTER NOC

Time: 10:30 am – 11:30 am
Room: 3016
Event Type: Research Session
Topic Area(s): EDA, In-Package and On-Chip Communication and Networks-on-Chip

Chair/Co-Chair: To be announced

Machine Learning (ML) plays an enabling role in NoC/NoI architecture design and optimization. The papers in this session highlight various opportunities to demonstrate the interplay between ML and manycore architectures. In fact, they focus on two broad classes: one is ML-enabled architecture design and the other is NoC architecture for ML accelerator.

TOPOLOGY AGNOSTIC VIRTUAL CHANNEL ASSIGNMENT AND PROTOCOL LEVEL DEADLOCK AVOIDANCE IN A NETWORK-ON-CHIP

***Anup Gangwar**, Arm Ltd., Austin, TX; Ravishankar Sreedharan, Ambica Prasad, Nitin Kumar Agarwal, Sri Harsha Gade, Arm Ltd., Bangalore, India*

ADELE: AN ADAPTIVE CONGESTION-AND-ENERGY-AWARE ELEVATOR SELECTION FOR PARTIALLY CONNECTED 3D NOCS

***Ebadollah Taheri**, Ryan Kim, Mahdi Nikdast, Colorado State University, Fort Collins, CO*

DEEP LEARN YOUR YIELD

Time: 11:30 am – 12:00 pm (Combined Session)
Room: 3016
Event Type: Research Session
Topic Area(s): EDA, Physical Design and Verification, Lithography and DFM

Chair/Co-Chair: David Z. Pan (The University of Texas at Austin); Co-chair to be announced

Wondering how to improve your manufacturability and yield at sub-5nm? These four papers bring the best of deep learning technologies and creative approaches to transfer learn layout pattern generations, attack data imbalance, insert SRAFs and accelerate dummy fill computation.

A TWO-STAGE NEURAL NETWORK CLASSIFIER FOR DATA IMBALANCED PROBLEM WITH APPLICATION TO HOTSPOT DETECTION

*Bingshu Wang, Lanfan Jiang, Wenxing Zhu, Longkun Guo, Fuzhou University, Fuzhou, China; **Jianli Chen**, Fudan University, Shanghai, China; Yao-Wen Chang, National Taiwan University, Taipei, Taiwan*

LOCKS, CLONES AND HAMMERS: TRUSTING YOUR CHIP IN A VULNERABLE WORLD

Time: 10:30 am – 11:30 am (Combined Session)
Room: 3014
Event Type: Research Session
Topic Area(s): Hardware Security: Attack and Defense, Security

Chair/Co-Chair: To be announced

The session presents reliability attacks in hardware design and proposes new methodologies for trustworthy fabrication. Get more insights into the Rowhammer vulnerability and its state-of-the-art variants by delving into a quantitative analytical model of capacitive-coupling weaknesses in DRAM. Learn about a new logic locking methodology which leverages high-level synthesis to protect IPs while mitigating attacks and minimizing area overhead and key size. Recent advances in Delay-PUFs are further analyzed to expose new modelling attacks that break previous security claims. Finally, a technique to fortify RTL locking techniques with scan-based functional mode isolation helps protect your keys along with your IP.

HLOCK: LOCKING IPS AT THE HIGH-LEVEL LANGUAGE

***Md Rafid Muttaki**, Roshanak Mohammadivojdan, Mark Tehranipoor, Farimah Farahmandi, University of Florida, Gainesville, FL*

FORTIFYING RTL LOCKING AGAINST ORACLE-LESS (UNTRUSTED FOUNDRY) AND ORACLE-GUIDED ATTACKS

***Nimisha Limaye**, Animesh B. Chowdhury, Siddharth Garg, Ramesh Karri, New York University, New York City, NY; Christian Pilato, Politecnico di Milano, Milan, Italy; Mohammed Nabeel, Ozgur Sinanoglu, New York University Abu Dhabi, Abu Dhabi, United Arab Emirates*

SHIPP - SECURITY HARDENING FOR INTELLECTUAL PROPERTY PROTECTION

Time: 11:30 am – 12:00 pm (Combined Session)
Room: 3014
Event Type: Research Session
Topic Area(s): Hardware Security: Primitives, Architecture, Design & Test, Security

Chair/Co-Chair: Jeyavijayan Rajendran (Texas A&M University) Co-Chair to be announced

This session covers the topic of intellectual property protection through piracy detection and secure design flow using high level synthesis tools and emerging devices. The presenters will discuss state of the art graph neural network-based piracy detection schemes, the implementation of side-channel attack resilient domain-oriented masking using high-level-synthesis to improve design time, and the security of hardware IP using emerging spin-based devices that utilize reconfigurable IP blocks. In addition, the use of architectural features for resource binding will be discussed as a means to enhance SAT resilience.

A RESOURCE BINDING APPROACH TO LOGIC OBFUSCATION*

***Michael Zuzak**, Yuntao Liu, Ankur Srivastava, University of Maryland, College Park, College Park, MD*

TRANSFORMING EMERGING TECHNOLOGIES IN THE POST-MOORE ERA

Time: 10:30 am – 11:30 am
Room: 3018
Event Type: Research Session
Topic Area(s): Design, Emerging Device Technologies

Chair/Co-Chair: Aatmesh Shrivastava (Northeastern University), Dinesh Patil (Facebook)

The impending end of Moore's Law shifts the focus of technology competitions from applications back to developing new devices. In this session, we study some transformative devices including memristors, nanomagnets, superconducting materials, and nanophotonics. These enabling technologies, which are still in their nascent stage, start to emerge as the candidate to replace CMOS devices in the post-Moore era. The four papers cover some compelling innovations in logic circuits design, computing architectures, and synthesis tools that are critical to the adoption of these technologies.

SECURE LOGIC LOCKING WITH STRAIN-PROTECTED NANOMAGNET LOGIC

***Naimul Hassan**, **Alexander J. Edwards**, Mustafa Munawar Shihab, Varun Venkat,Peng Zhou, Xuan Hu, Shamik Kundu, Abraham Peedikayil Kuruvila, Kanad Basu, Yiorgos Makris, Joseph S. Friedman, The University of Texas at Dallas, Richardson, TX; Dhritiman Bhattacharya, Jayasimha Atulasimha, Virginia Commonwealth University, Richmond, VA*

QSEQ: FULL ALGORITHMIC AND TOOL SUPPORT FOR SYNTHESIZING SEQUENTIAL CIRCUITS IN SUPERCONDUCTING SFQ TECHNOLOGY

***Ghasem Pasandi**, Massoud Pedram, University of Southern California, Los Angeles, CA*

NEW FRONTIERS IN FORMAL AND STATIC VERIFICATION

Thank You to Our Sponsor SIEMENS

Time: 10:30 am – 11:30 am (Combined Session)
Room: 2010/2012
Event Type: Designer, IP and Embedded Systems Track Presentations
Topic Area(s): Front-End Design

Chair/Co-Chair: Maheshwar Chandrasekar (Synopsys)

In this essential session, there will be talks that focus on new explorations of formal techniques and tools by industry giants and research lab. A new approach to use formal analysis to ensure automotive SoC's adhere to safety standards will be presented. Other presentations focus on architectural analysis, design partitioning and completeness for formal sign-off. Finally, a couple of presentations focus on static verification techniques for reset/power domains and constraint based clock-domain crossing sign-off that circumvent error-prone waiver mechanism.

OPTIMIZING FAULT SIMULATIONS WITH FORMAL ANALYSIS FOR ASIL COMPLIANCE

***Vaibhav Kumar**, NXP Semiconductors Inc., Austin, TX; Jiri Prevratil, Tareq Altakrouri, Synopsys, Plano, TX*

CONSTRAINTS BASED CDC SIGN-OFF METHODOLOGY

*Sharan Mohan, Rambabu Singampalli, Pinkesh Shah, Western Digital, Bangalore, India; **Varun Sharma**, Real Intent Inc, Sunnyvale, CA*

LABREPLAY: EFFICIENT REPLAY OF POST-SILICON DEBUG FOR HIGH PERFORMANCE MICROPROCESSOR DESIGNS

***Arun Joseph**, Spandana Rachamalla, Shiladitya Ghosh, Shashidhar Reddy, Pradeep Joy, Sampath Baddam, IBM, Bangalore, India; Samuel Kirchhoff, Wolfgang Roesner, IBM, Austin, TX; Joachim Fenkes, IBM, Böblingen, Germany*

ENSURING COMPLETENESS OF FORMAL VERIFICATION WITH GAPFREE: ARE WE DONE YET?

***Ratish Punnoose**, Sandia National Labs, Livermore, CA*

SOLIDIFYING YOUR SOC BEYOND DESIGN

Thank You to Our Sponsor PERFORCE

Time: 10:30 am – 11:30 am
Room: 2008
Event Type: Designer, IP and Embedded Systems Track Presentations
Topic Area(s): IP

Chair/Co-Chair: Chirag Dhruv, (AMD)

Does a solid design in itself guarantee solid end product? With SOC Design methodologies well understood, often times teams face challenges in terms of having robust Silicon due to power/performance, test coverage and reliability related issues. In this session, experts will talk about some of the key factors that can be considered during design phase of the Chip to solidify the Silicon. We will look at techniques used by some of the experienced engineers to improve effects of aging and reduce variability challenges, ways to improve power and performance of your designs and key considerations while integrating Mixed-Signal IPs.

INNOVATIVE IN-SITU SLACK MONITOR (IS2M) DESIGN FOR DYNAMIC DETECTION OF VOLTAGE TEMPERATURE AGEING CHANGE.

***Rohit Goel**, Rajnish Garg, Anand Mishra, STMicroelectronics, Greater Noida, India; Florian Cacho, Damien Riquet, Pascal Urard, STMicroelectronics, Crolles, France*

MITIGATING VARIABILITY CHALLENGES OF IPS FOR ROBUST DESIGN

***Atul Bhargava**, Rachit Sharma, Rajnish Garg, Rohit Kumar Gupta, STMicroelectronics, Noida, India; Mike Sheinin, Siemens EDA, Saskatoon, Canada; Nebabie Kebebew, Siemens EDA, Fremont, CA*

TECH TALK: CHARTING THE PATH TO 3NM & MORE THAN MOORE

Time: 11:30 am – 12:30 pm
Room: DAC Pavilion
Event Type: Tech Talk

For more than fifty years, the trend known as Moore's Law has astutely predicted a doubling of transistor count every twenty-four months. As 3nm technology moves into production, process engineers are feverishly working to uphold Moore's Law by further miniaturizing the next generation of semiconductor technology. Meanwhile, a second trend referred to as "More than Moore" was coined in 2010 to reflect the integration of diverse functions and subsystems in 2D SoCs and 2.5D and 3D packages. Today, the trends of Moore's Law and "More than Moore" synergize to produce ever higher value systems.

Working together, advances in both process technology and electronic design automation (EDA) have driven fundamental evolutions behind these two important semiconductor trends. This talk will examine the amazing and innovative developments in EDA over the years, culminating in the era of 3DIC and Machine Learning-based EDA to chart the path to 3nm and More than Moore.

Speaker(s): Michael Jackson, Cadence Design Systems, Inc., Mountain View, CA

SKY TALK: ACCELERATOR ARCHITECTURES AND MACHINE LEARNING - AI HARDWARE

Time: 1:00 pm – 1:45 pm
Room: DAC Pavilion
Event Type: SKY Talk

Over the past decade, Deep Neural Network (DNN) workloads have dramatically increased the computational requirements of AI Training and Inference systems – significantly outpacing the performance gains obtained traditionally using Moore's law of silicon scaling. New computer architectures, powered by low precision arithmetic engines (FP16 for training and INT8 for Inference), have laid the foundation for high performance AI systems – however, there remains an insatiable desire for AI compute with much higher power-efficiency and performance. In this talk, I'll outline some of the exciting innovations as well as key technical challenges – that can enable systems with aggressively scaled precision for inference and training, while fully preserving model fidelity. I'll also highlight some key complementary trends, including 3D stacking, sparsity and analog computing, that can enable dramatic growth in the AI system capabilities over the next decade.

Speaker(s): Kailash Gopalakrishnan, IBM Research, New York City, NY

INTELLIGENT SOFTWARE AND SYSTEM ARCHITECTURES FOR SMART MEMORIES

Time: 1:30 pm - 2:00 pm (Combined Session)
Room: 3014
Event Type: Research Session
Topic Area(s): Embedded Systems, Near-Memory and In-Memory Computing

Chair/Co-Chair: Co-Chair to be announced

Compute-in-Memory (CIM) platforms rely heavily on reliable and efficient software stacks as well as finely tuned system architectures to leverage their true potential. This session pushes state of the art in this exciting area from developing new CIM architectures to efficiently attain really large attention spans in transformer networks, developing smart memory placement algorithms for heterogenous memories, removing synchronization bottlenecks, and speeding up LU Factorization and deploying PIM to enable ultra-fast mRNA Quantification.

MAT: PROCESSING IN-MEMORY ACCELERATION FOR LONG-SEQUENCE ATTENTION

***Minxuan Zhou**, Yunhui Guo, Weihong Xu, Tajana Rosing, University of California, San Diego, La Jolla, CA; Bin Li, Kevin Eliceiri, University of Wisconsin-Madison, Madison, WI*

FAST, COOL AND ERROR TOLERANT COMPUTE-IN-MEMORY

Time: 2:00 pm – 2:30 pm (Combined Session)
Room: 3014
Event Type: Research Session
Topic Area(s): Embedded Systems, Near-Memory and In-Memory Computing

Chair/Co-Chair: Co-Chair to be announced

Compute-in-Memory (CIM) offers us a promising path to escape traditional Von-Neumann Memory Bottlenecks. This session helps push state of the art in this new paradigm by introducing ultra-low-power 3D-Nand compute substrates for AI, pioneering the deployment of ECC codes for error and variation tolerant CIM, developing high-throughput near-memory accelerators for graph workloads, and enabling ultra-fast max-min searches in DRAMs.

EFFICIENT ERROR-CORRECTING-CODE MECHANISM FOR HIGH-THROUGHPUT MEMRISTIVE PROCESSING-IN-MEMORY

***Orian Leitersdorf**, Ben Perach, Ronny Ronen, Shahar Kvatinsky, Technion, Israel Institute of Technology, Haifa, Israel*

NOVEL STRATEGIES FOR I/O SYSTEMS AND DEVICES MANAGEMENT

Time: 2:30 pm – 3:00 pm (Combined Session)
Room: 3014
Event Type: Research Session
Topic Area(s): Embedded Systems, Embedded Memory, Storage and Networking

Chair/Co-Chair: Co-Chair to be announced

This session describes new strategies based on machine learning and cross-layer approaches to improve the performance and energy levels of new I/O devices, as well as addressing the robustness of novel technologies. The first two papers of the session explore a new update strategy against crashes in magnetic recording devices, and the use of reinforcement learning for persistent caches. The last two papers look at new management approaches for mobile memory systems.

OPENMEM: HARDWARE/SOFTWARE COOPERATIVE MANAGEMENT FOR MOBILE MEMORY SYSTEM

*Fei Wen, Mian Qin, **Paul Gratz**, Narasimha Reddy, Texas A&M University, College Station, TX*

SMARTER COMPUTE ENGINES FOR GREENER ML

Time: 1:30 pm – 2:35 pm (Combined Session)
Room: 3018
Event Type: Research Session
Topic Area(s): Design, AI/ML System Design

Chair/Co-Chair: Weiwen Jiang (University of Notre Dame), Co-Chair to be announced

This world is always seeking better hardware accelerators to improve machine learning computing performance. This session presents four research works focusing on optimizing computer hardware to improve machine learning execution performance. Efficient hardware accelerators incorporated with innovative optimizations are presented in this session to accelerate widely-used machine learning networks, such as 2D and 3D convolutional neural networks as well as reinforcement learning, with less energy consumption.

DATAFLOW MIRRORING: ARCHITECTURAL SUPPORT FOR HIGHLY EFFICIENT FINE-GRAINED SPATIAL MULTITASKING ON SYSTOLIC-ARRAY NPUS

*Jounghoo Lee, **Jinwoo Choi**, Jaeyeon Kim, Jinho Lee, Youngsok Kim, Yonsei University, Seoul, South Korea*

RASA: EFFICIENT REGISTER-AWARE SYSTOLIC ARRAY MATRIX ENGINE FOR CPU

***Geonhwa Jeong**, Eric Qin, Ananda Samajdar, Hyesoon Kim, Tushar Krishna, Georgia Institute of Technology, Atlanta, GA; Christopher J. Hughes, Intel Corporation, Santa Clara, CA; Sreenivas Subramoney, Intel Corporation, Bangalore, India*

FIXAR: A FIXED-POINT DEEP REINFORCEMENT LEARNING PLATFORM WITH QUANTIZATION-AWARE TRAINING AND ADAPTIVE PARALLELISM

***Je Yang**, Seongmin Hong, Joo-Young Kim, Korea Advanced Institute of Science and Technology, Daejeon, South Korea*

BEYOND SUPERVISED LEARNING: APPROACHES FOR EFFICIENT AND RELIABLE INTELLIGENCE

Time: 2:35 pm – 3:00 pm (Combined Session)
Room: 3018
Event Type: Research Session
Topic Area(s): Design, AI/ML System Design

Chair/Co-Chair: Priyadarshini Panda (Yale University), Sumit K. Mandal (University of Wisconsin-Madison)

As AI is entering into all aspects of our lives, issues such as scalability, privacy, and reliability become predominant in addition to performance. There exists an increasing interest in non-traditional methods to address the efficiency/complexity dilemma encountered in supervised learning. This session presents four diverse approaches along with federated learning, Hyper-dimensional computing, reinforcement learning, and verifiable deep learning.

A3C-S: AUTOMATED AGENT ACCELERATOR CO-SEARCH TOWARDS EFFICIENT DEEP REINFORCEMENT LEARNING

*Yonggan Fu, **Yongan Zhang**, Chaojian Li, Zhongzhi Yu, Yingyan Lin, Rice University, Houston, TX*

SPECULATIONS ON ROUTES TO BOOST POWER AND ENERGY EFFICIENCY

Time: 1:30 pm – 3:00 pm
Room: 3016
Event Type: Research Session
Topic Area(s): EDA, Cross-Layer Power Analysis and Low-Power Design

Chair/Co-Chair: Elaheh Bozorgzadeh (University of California, Irvine); Andreas Burg, to be announced

This session describes four methods of designing and managing digital systems to improve their power, energy, and thermal properties. It opens with a lightweight machine learning technique to improve the boostability of multicore systems, considering power, performance, and temperature. The next presentation describes control of runtime dynamic concurrency throttling and frequency boosting parameters to improve OpenMP energy-delay products. The third presentation describes a design space exploration technique using hybrid static/dynamic speculation; it considers most-significant input bits, depth-of-carry histories, and local thread identifiers to improve accuracy. The session closes with an impedance-driven design space exploration tool for board-level power networks.

SMARTBOOST: LIGHTWEIGHT ML-DRIVEN BOOSTING FOR THERMALLY-CONSTRAINED MANY-CORE PROCESSORS

***Martin Rapp**, Mohammed Bakr Sikal, Heba Khdr, Jörg Henkel, Karlsruhe Institute of Technology, Karlsruhe, Germany*

ST2GPU: AN ENERGY-EFFICIENT GPU DESIGN WITH SPATIO-TEMPORAL SHARED-THREAD SPECULATIVE ADDERS

***Vijay Kandiah**, Nikos Hardavellas, Northwestern University, Evanston, IL; Ali Murat Gok, Argonne National Laboratory, Lemont, IL; Georgios Tziantzioulis, Princeton University, Princeton, NJ*

SYNERGICALLY REBALANCING PARALLEL EXECUTION VIA DCT AND TURBO BOOSTING

*Sandro Matheus Marques, Thiarles Soares Medeiros, Marcelo Caggiani Luizelli, **Arthur Francisco Lorenzon**, Fábio Diniz Rossi, Farroupilha Federal Institute, Alegrete, Brazil; Antonio Carlos Schneider Beck, Federal University of Rio Grande do Sul, Porto Alegre, Brazil*

SPROUT – SMART POWER ROUTING TOOL FOR BOARD-LEVEL EXPLORATION AND PROTOTYPING

***Rassul Bairamkulov**, Eby G. Friedman, University of Rochester, Rochester, NY; Abinash Roy, Mali Nagarajan, Vaishnav Srinivas, Qualcomm CDMA Technologies Inc., San Diego, CA*

IS YOUR PRODUCT SECURE? - AN IP DRIVEN APPROACH TO PRODUCT SECURITY

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Time: 1:30 pm – 2:30 pm
Room: 2008
Event Type: Designer, IP and Embedded Systems Track Presentations
Topic Area(s): IP

Chair/Co-Chair: Raymond Nijssen (Achronix)

EMBEDDED SECURITY OPTIMIZED WITH EFPGA

***Imen Baili**, MENTA S.A.S, Valbonne, Sophia-Antipolis, France; Michel Le Rolland, Secure-IC, Rennes, France*

POWER MANAGEMENT VERIFICATION OF [COMPANY] [SOC NAME] GPU

***David Akselrod**, AMD, Markham, Canada*

SMART DIGITAL SENSORS AGAINST TAMPERING

***Sylvain Guilley**, Michel Le Rolland, Secure-IC, Rennes, France*

HOW SYSTEM COMPANIES ARE RE-SHAPING REQUIREMENTS FOR EDA

Time: 2:00 pm – 2:45 pm
Room: DAC Pavilion
Event Type: DAC Pavilion Panels

As predicted by Hennessy/Patterson in 2018, the electronics industry is entering an era of domain-specific architectures and domain-specific languages that enable hyperscale computing at never-before-seen complexity, advanced edge processing, and a new breed of consumer devices. As a result, industry verticals like automotive, consumer, mobile, networking, and data center compute are re-shaping to new vertical integration and specialization levels. For example, consumer devices will deliver new user experiences at form factors and power envelopes that were hard to imagine just years ago and will exist in a hyperconnected, always-on world. In addition, hyper-convergence for infrastructure in data centers re-balances memory, storage, network, and computing at never before seen pace. This panel will discuss the resulting new sets of EDA and System Analysis requirements, including new innovative approaches for 3DIC integration, Low-Power/Thermal and Electromagnetic Analysis, and enablement for workload-optimized server and AI/ML chips and systems across data centers, networks, edges, and consumer devices. The panel will also discuss the changes in the overall supply chain for data-center silicon and system development.

FANTASTIC SOCS AND WHERE TO FIND THEM!

Time: 3:30 pm – 5:30 pm
Room: 3016
Event Type: Research Session
Topic Area(s): EDA, System-on-Chip Design Methodology

Chair/Co-Chair: Peipei Zhou (University of Pittsburgh), Co-Chair to be announced

With the increasing complexity of systems-on-chip (SoCs), developing efficient SoC design-space exploration methodologies has become challenging. This session presents six papers with novel contributions in the development of HDL framework for SoCs and improvement in SoC performance for acceleration. The first two papers focus on the behavioral design of SoCs and improve their performance for DNN acceleration. The third and fourth papers present co-exploration solutions and structural compilers for SoC-based accelerators. Finally, the last two papers propose new automated-design frameworks for hardware.

UPTPU: IMPROVING ENERGY EFFICIENCY OF A TENSOR PROCESSING UNIT THROUGH UNDERUTILIZATION BASED POWER-GATING

*Pramesh Pandey, Noel Daniel Gundi, **Sanghamitra Roy**, Koushik Chakraborty, Utah State University, Logan, UT*

DANCE: DIFFERENTIABLE ACCELERATOR/NETWORK CO-EXPLORATION

*Kanghyun Choi, Yonsei University, Seoul, South Korea; **Deokki Hong**, Hojae Yoon, Youngsok Kim, Jinho Lee, Yonsei University, Seoul, South Korea; Joonsang Yu, Seoul National University, Seoul, South Korea*

NEW REGULAR EXPRESSIONS ON OLD ACCELERATORS

***Jackson Woodruff**, Michael F. P. O'Boyle, University of Edinburgh, Edinburgh, United Kingdom*

PROPERTY-DRIVEN AUTOMATIC GENERATION OF REDUCED-ISA HARDWARE

***Nathaniel L. Bleier**, Rakesh Kumar, University of Illinois at Urbana-Champaign, Champaign, IL; John Sartori, University of Minnesota, Minneapolis, MN*

BHDL: A LUCID, EXPRESSIVE, AND EMBEDDED PROGRAMMING LANGUAGE AND SYSTEM FOR PCB DESIGNS

***Hebi Li**, Youbiao He, Qi Xiao, Jin Tian, Forrest Sheng Bao, Iowa State University, Ames, IA*

FROM BRAINS TO BITS

Time: 3:30 pm – 4:00 pm (Combined Session)
Room: 3018
Event Type: Research Session
Topic Area(s): Design, Emerging Models of Computation

Chair/Co-Chair: Siddharth Joshi (University of Notre Dame); Shaolan Li (Georgia Institute of Technology)

This session presents six papers that explore advanced algorithms and hardware design to develop the next-generation of brain-inspired intelligent systems. While the first paper discusses neuromorphic hardware-algorithm co-design, the second paper demonstrates algorithm-mapping to neuro-inspired hardware. The next two papers address robustness and resiliency in machine-learning systems. The fifth paper discusses neural processing for event cameras and the last paper of this session presents a methodology to attain robustness against adversarial attacks in hyper-dimensional computing.

SCALABLE PITCH-CONSTRAINED NEURAL PROCESSING UNIT FOR 3D INTEGRATION WITH EVENT-BASED IMAGERS

***Maxence Bouvier**, Alexandre Valentian, Gilles Sicard, CEA, Grenoble, France*

INTELLIGENT EDGE-CLOUD COMPUTING ARCHITECTURES FOR CPS

Time: 4:00 pm – 4:30 pm (Combined Session)
Room: 3018
Event Type: Research Session
Topic Area(s): Design, Design of Cyber-physical Systems and IoT

Chair/Co-Chair: to be announced

This session presents techniques for collaborative, efficient, and adaptive design of CPS and IoT systems. Several papers in the session address the key challenge of collaborative edge-cloud execution of machine learning workloads. Innovative techniques such as multi-objective neural architecture search, complexity-aware selection of inference-location, and bandwidth-saving approaches such as adaptive frame clustering and operating on compressed video streams are proposed. The session also features papers that propose design frameworks to automatically learn neural network controllers and a novel priority assignment approach for CAN bus messages.

COCKTAIL: LEARN A BETTER NEURAL NETWORK CONTROLLER FROM MULTIPLE EXPERTS VIA ADAPTIVE MIXING AND ROBUST DISTILLATION

***Yixuan Wang**, Chao Huang, Zhilu Wang, Shichao Xu, Zhaoran Wang, Qi Zhu, Northwestern University, Evanston, IL*

THAT QUANTUM SESSION EVERYONE IS TALKING ABOUT

Time: 4:30 pm – 5:00 pm (Combined Session)
Room: 3018
Event Type: Research Session
Topic Area(s): Design, Quantum Computing

Chair/Co-Chair: to be announced

Quantum noise is a major roadblock towards its applicability. Furthermore, there is a strong need to accelerate the quantum simulations and explore the application domains of quantum computing. This session addresses these challenges via novel approaches to design and simulate quantum circuits, develop various error mitigation/correction techniques and explore applications in machine learning.

QUANTUM SPECTRAL CLUSTERING OF MIXED GRAPHS

***Daniel Volya**, Prabhat Mishra, University of Florida, Gainesville, FL*

WHEN THEY GO HIGH – WE GO LOW (IN COMPUTATION)

Time: 4:30 pm – 5:00 pm
Room: 3014
Event Type: Research Session
Topic Area(s): Design, Approximate Computing for AI/ML

Chair/Co-Chair: Aayush Ankit (Microsoft), Co-Chair to be announced

Low computational complexity improves hardware efficiency. To that end, this session reports cutting-edge developments in the domain of Approximate Computing for AI Hardware-Software codesign. Along with novel algorithmic techniques addressing pruning and reduced precision, the session dives deeper into cross-layer optimization and approximate arithmetic for different types of deep neural network accelerators ranging from embedded FPGA systems to in-memory computing.

SOFTERMAX: HARDWARE/SOFTWARE CO-DESIGN OF AN EFFICIENT SOFTMAX FOR TRANSFORMERS

***Jacob R. Stevens**, Anand Raghunathan, Purdue University, West Lafayette, IN; Rangharajan Venkatesan, Steve Dai, NVIDIA, Santa Clara, CA; Brucek Khailany, NVIDIA, Austin, TX*

CONTROL VARIATE APPROXIMATION FOR DNN ACCELERATORS

*Georgios Zervakis, Karlsruhe Institute of Technology, Karlsruhe, Germany; Ourania Spantidi, **Iraklis Anagnostopoulos**, Southern Illinois University, Carbondale, IL; Hussam Amrouch, University of Stuttgart, Stuttgart, Germany; Jörg Henkel, Karlsruhe Institute of Technology, Karlsruhe, Germany*

COSAIM: COUNTER-BASED STOCHASTIC-BEHAVING APPROXIMATE INTEGER MULTIPLIER FOR DEEP NEURAL NETWORKS

***Shuyuan Yu**, Yibo Liu, Sheldon Tan, University of California, Riverside, Riverside, CA*

EXCHANGING EDA DATA FOR AI/ML USING STANDARD API

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Time: 3:30 pm – 5:00 pm
Room: 2010/2012
Event Type: Designer, IP and Embedded Systems Track Presentations
Topic Area(s): Machine Learning/AI

Chair/Co-Chair: Leigh Anne Clevenger (Silicon Integration Initiative, Inc.)

Session Organizers: Leigh Anne Clevenger, Silicon Integration Initiative, Inc., Albany, NY; Kerim Kalafala, IBM, Poughkeepsie, NY

Recent industry surveys show that current status quo involving siloed development on proprietary APIs results in significant difficulties in collaborating on AI/ML in the field of EDA. Key issues are: 1) lack of a standard means of exchanging derived data between partners and 2) the concomitant duplication of efforts due to proprietary hurdles. In this special session, experts representing chip design, EDA vendors, and academia provide perspectives on the need for a common API to present derived data for AI/ML pertaining to IC design. This session includes a discussion of existing data formats, applications that use these data types, and of how advances in AI/ML are driving needs which extend beyond capabilities of existing APIs. The topic of IP protection will be a particular focus, including perspectives on what mechanisms need to be in place for data sharing, and various levels of security required depending on the application domain.

Speakers: Kerim Kalafala, IBM, Poughkeepsie, NY ; Lakshmanan Balasubramanian, Texas Instruments (India) Pvt. Ltd., Bengaluru, India Firas Mohammed, Silvaco, Grenoble, France Andrew Kahng, University of California, San Diego, San Diego, CA

TUESDAY DESIGNER, IP, AND EMBEDDED SYSTEMS POSTER GLADIATORS PRESENTATION

Thank You to Our Sponsor SIEMENS methodics by Perforce

Time: 4:30 pm – 5:30 pm
Room: DAC Pavilion

HYBRID EMULATION METHODOLOGY FOR SSD DESIGN

Byunghoon Lee, Kyungsu Kang, Sangho Park, SunGil Lee, Seunghan Lee, Byeongwook Bae, Jungyun Choi, JaeWoo Im, Samsung Electronics, Hwaseong, South Korea

DEEP DATA FOR FASTER SILICON BRING-UP, CHARACTERIZATION, AND QUALIFICATION WITH HIGHER CONFIDENCE

Evelyn Landman, Nir Sever, proteanTecs, Haifa, Israel; Alex Burlak, proteanTecs, Bridgewater, Israel

END-TO-END SOLUTION FOR STRUCTURED IMPLEMENTATION OF HIGH-SPEED DATA BUSES

Shubham Agarwal, Subhadarshini Behera, Dheeraj Tuteja, Shishir Saran Rai, Intel Technology India Pvt. Ltd., Bangalore, India

EXPEDITING DATA CONVERTER LAYOUTS USING DESIGN PLANNING & ANALYSIS (DPA) AUTOMATION

Atul Bhargava, Monika Lilani, STMicroelectronics, Greater Noida, India; Colin Thomson, Cadence Design Systems, Inc., Edinburgh, United Kingdom; Vishesh Kumar, Cadence Design Systems, Inc., Noida, India

ALGORITHM TO RTL: A FASTER PATH TO IMPLEMENTATION

Russell Klein, Siemens EDA, Wilsonville, OR; Anoop Saha, Siemens EDA, Fremont, CA

INNOVATIVE TECHNIQUES TO ACCELERATE ERROR HANDLING VERIFICATION OF COMPLEX SYSTEMS

Bhushan Parikh, Peter Graniello, Neha Rajendra, Intel Corporation, Chandler, AZ

A FLEXIBLE SAR-ADC IP FOR MULTIPLE TECHNODES

Torsten Reich, Benjamin Prautsch, Marcel Jotschke, Fraunhofer IIS/EAS, Dresden, Germany

ROBUST TIMING ANALYSIS AND OPTIMIZATION UNDER PARAMETRIC ON-CHIP PROCESS VARIATION

Jaeyoung Lim, Moon-Su Kim, Jegil Moon, Yun Heo, Ilryong Kim, Samsung Electronics, Hwaseong, South Korea; Wenwen Chai, Li Ding, Synopsys, Mountain View, CA

TUESDAY DESIGNER, IP AND EMBEDDED SYSTEMS TRACK POSTERS

Time: 5:00 pm – 6:00 pm
Room: Exhibit Hall Level 2
Event Type: Designer, IP and Embedded Systems Track Poster Networking Reception

ABSTRACTION – AN EFFICIENT METHODOLOGY FOR RTL & LOW-POWER SIGNOFF IN SOC DESIGN ROHIT SINHA, INTEL CORPORATION ANALOG IN MEMORY COMPUTING OPTIMIZATION WITH TOPS/W METHODOLOGY

***She-Hwa Yen**, Applied Materials, Santa Clara, CA*

ANDES ACE FEATURE EXTENDED ON MENTA EFPGA FOR RISC-V CORES ISA RECONFIGURABILITY IN THE FIELD

***Imen Baili**, MENTA S.A.S, Valbonne, France; YiChiang Chang, Andes Technology, Hsinchu, Taiwan*

AN AUTOMATED APPROACH TO PRE-EMPT CLOCK-DIVERGENCE & ACHIEVE PREDICTABLE TIMING CLOSURE

***Divya Yogi**, Rathish Chandran, Intel Technology India Pvt. Ltd., Bangalore, India*

AUTOMATED GENERATION OF CURRENT CONTROLLED OSCILLATOR (CCO) LAYOUT USING TEMPLATE REUSE FLOW

***Rajeev Singh**, Vijay Singh Khati, Atul Bhargava, Akshita Bansal, STMicroelectronics, Greater Noida, India; Aneesh Shastry, Vishesh Kumar, Cadence Design Systems, Inc., Noida, India*

CONTROLLED OSCILLATOR (CCO) LAYOUT USING TEMPLATE REUSE FLOW

Rajeev Singh, Vijay Singh Khati, Atula Bhargava, Akshita Bansal, Aneesh R. Shastry, Vishesh Kumar, Cadence Design Systems, Inc., Noida, India

CONSTRAINTS BASED CDC SIGN-OFF METHODOLOGY

*Sharan Mohan, Rambabu Singampalli, Pinkesh Shah, Western Digital, Bangalore, India; **Varun Sharma**, Real Intent Inc., Sunnyvale, CA*

DEEP DATA FOR FASTER SILICON BRING-UP, CHARACTERIZATION, AND QUALIFICATION WITH HIGHER CONFIDENCE

*Evelyn Landman, Nir Sever, **Uzi Baruch**, proteanTecs, Haifa, Israel; Alex Burlak, proteanTecs, Bridgewater, NJ*

DUAL FEATURE VECTOR HETERO GRAPH NEURAL NETWORK (DFV-GNN) BASED POST-LAYOUT PARASITIC ESTIMATION

*Sungwon Kim, Intel Corporation, Portland, OR; **Hui Fu**, Intel Corporation, Austin, TX*

EFFICIENT IMPEDANCE DISCONTINUITY OPTIMIZATION TECHNIQUE FOR HIGH SPEED INTERFACES

***Jiyoung Park**, Sumant Srikant, Seungki Nam, Sungwook Moon, Samsung Electronics, Hwasung, South Korea*

EXTENDED POWER CONNECTIVITY SOLUTION FOR CPF BASED LOW POWER SIMULATION

***Lakshmanan Balasubramanian**, Abhinav Parashar, Sooraj Sekhar, Texas Instruments (India) Pvt. Ltd., Bengaluru, India; Vivek Gandhi, Samsung Semiconductor India, Bengaluru, India*

FORMAL VERIFICATION OF SAFETY MECHANISMS | INFINEON TECHNOLOGIES

***Keerthikumara Devarajegowda**, Infineon Technologies AG, Neubiberg, Germany*

A HIGHLY REUSABLE GENERIC UVM FOR SOFT PROCESSORS

***Khaled Mohamed**, Ayub Khan, Siemens EDA, Fremont, CA; Kholoud Mahmoud Ahmed, Randa Ahmed, Yasser Ibrahim, Waleed Taie, Mostafa Ayman, Karim Ayman, Hassan Mostafa, Cairo University, Cairo, Egypt*

NOVEL CHIP-PACKAGE-SYSTEM POWER NOISE ANALYSIS WITH RTL POWER PROFILING

Bin Xiao, Ying Hui Shu, Li Guo Feng, Yue Feng Chen, Yu Chen, ZTE Co., Shenzhen, China; Zhongming Hou, Ansys, Shenzhen, China; Arindam Mitra, Ansys

ON THE ENERGY EFFICIENCY OF MACHINE LEARNING FRAMEWORKS

***Nagu Dhanwada**, IBM Systems, Poughkeepsie, NY; Kartik Acharya, IBM Systems, Atlanta, GA; Lourie Goodall, IBM Systems, Tucson, AZ; Yves Santos, IBM Systems, Houston, TX; Vaidyanathan Srinivasan, IBM Systems, Bangalore, India; Karthik Swaminathan, IBM Research, Yorktown Heights, NY*

"OPENOPU", A COMPLETE SOLUTION FOR HETEROGENEOUS COMPUTING

***Mingyu Wang**, Zeyu Wang, University of California, Los Angeles, Los Angeles, CA*

ROUTABILITY IMPROVEMENT METHODOLOGY USING MULTIPLE STANDARD CELLS WITH VARIOUS PIN LOCATION

Jooyeon Kwon, Yongcheul Kim, Sangdo Park, Yeongyeong Shin, Joonyoung Shin, Sua Lee, Hyung-Ock Kim, Sangyun Kim, Samsung Electronics, Hwaseong-si, South Korea

A SCALABLE MULTICORE RISC-V GPGPU ACCELERATOR FOR HIGH-END FPGAS

Blaise Pascal Tine, Fares Elsabbagh, Georgia Institute of Technology, Atlanta, GA

A SINGLE SOLUTION FOR SCANNING, TRACKING INVENTORY, TRANSACTIONS, AND RECHARGING

***Edward Garcia**, Comark, Milford, MA*

TOWARDS MEASURING LAYOUT PATTERN COVERAGE: A MACHINE LEARNING APPROACH

***Hui Fu**, Intel Corporation*

TUESDAY WORK-IN-PROGRESS POSTERS

Time: 6:00 pm – 7:00 pm
Room: Level 2 Foyer
Event Type: Networking Reception, Work-in-Progress Poster

AMBROSIA: REDUCTION IN DATA TRANSFER FROM SENSOR TO SERVER FOR INCREASED LIFETIME OF IOT SENSOR NODES

***Shikhar Suryavansh**, Somali Chaterji, Purdue University, West Lafayette, IN; Abu Benna, Beaconchain, Calgary, Canada; Chris Guest, LightBug, Bristol, United Kingdom*

CONTEXT-AWARE AND CODR TASK HANDLING IN RESOURCE-CONSTRAINED ROBOTS WITH VIRTUALIZATION

***Ramyad Hadidi**, Nima Shoghi Ghalehshahi, Bahar Asgari, Hyesoon Kim, Georgia Institute of Technology, Atlanta, GA*

CODR: COMPUTATION AND DATA REUSE AWARE CNN ACCELERATOR

***Alireza Khadem**, Haojie Ye, Trevor Mudge, University of Michigan, Ann Arbor, MI*

DESIGN CONTEXT AWARE ELECTROMIGRATION ANALYSIS METHODOLOGY TO OVERCOME BEOL INTERCONNECT SCALING INDUCED RELIABILITY RISK FOR ADVANCED PROCESS TECHNOLOGY

***Kwangseok Choi**, Jinseok Kim, Dongyoun Yi, Minseok Kang, Yongho Lee, Byunghyun Lee, Samsung Electronics, Hwaseong-si, South Korea*

DETECTING SECURITY AND PRIVACY THREATS IN HOME IOT NETWORKS THROUGH TRAFFIC PROFILING

***Malin P. Prematilake**, Vijay Raghunathan, Purdue University, West Lafayette, IN*

EDGENAI: DISTRIBUTED INFERENCE WITH LOCAL EDGE DEVICES AND MINIMUM LATENCY

***Maedeh Hemmat**, Azadeh Davoodi, Yu Hen Hu, University of Wisconsin-Madison, Madison, WI*

ENERGY HARVESTING AWARE MULTI-HOP ROUTING AND ENERGY ALLOCATION IN DISTRIBUTED IOT SYSTEM BASED ON MULTI-AGENT REINFORCEMENT LEARNING

***Wen Zhang**, Longzhuang Li, Dulal Kar,Chen Pan, Texas A&M University at Corpus Christi, Corpus Christi, TX; Tao Liu, Lawrence Technological University, Southfield, MI; Mimi Xie, The University of Texas at San Antonio, San Antonio, TX*

GUIDING GLOBAL PLACEMENT WITH REINFORCEMENT LEARNING

Robert Kirby,Rajarshi Roy, Saad Godil, Bryan Catanzaro, NVIDIA, Santa Clara, CA; Kolby Nottingham, University of California, Irvine, Irvine, CA

HAMMERFILTER: ROBUST PROTECTION AND LOW HARDWARE OVERHEAD METHOD FOR ROW-HAMMERING

***Kwangrae Kim**, Junsu Kim, Ki-Seok Chung, Hanyang University, Seoul, South Korea; Jeonghyun Woo, University of Illinois at Urbana-Champaign, Champaign, IL*

A HIGH EFFICIENCY POWER OBFUSCATION SWITCHED CAPACITOR DC-DC CONVERTER ARCHITECTURE

***Nikita Mirchandani**, Majid Sabbagh, Yunsi Fei, Aatmesh Shrivastava, Northeastern University, Boston, MA*

AN IN-MEMORY ANALOG COMPUTING CO-PROCESSOR FOR ENERGY-EFFICIENT CNN INFERENCE ON MOBILE DEVICES

***Mohammed Elbtity**, Brendan Reidy, Ramtin Zand, University of South Carolina, Columbia, SC; Abhishek Singh, Xiaochen Guo, Lehigh University, Bethlehem, PA*

LEARNING QUANTUM CIRCUIT ERRORS BASED ON ERROR PROPAGATION

*Nikita Acharya, **Vedika Saravanan**, Samah Saeed, CUNY City College, New York City, NY*

NOVEL STATIC TIMING ANALYSIS CONSIDERING DYNAMIC VOLTAGE DROP

*Jongyoon Jung, Chul Rim, Hyung-Ock Kim, Sangyun Kim, Samsung Electronics, Hwaseong-si, South Korea; **Andrew Hoover**, Samsung Electronics, Austin, TX*

OPTIMIZING TEMPORAL CONVOLUTIONAL NETWORKS FOR ULTRA-LOW-POWER EDGE-BASED TIME SERIES ANALYTICS

*Alessio Burrello, Francesco Conti, Marcello Zanghieri, Luca Benini, University of Bologna, Torino, Italy; Alberto Dequino, **Daniele Jahier Pagliari**, Enrico Macii, Massimo Poncino, Politecnico of Turin, Torino, Italy*

PROCRASTINATING CFI FOR HARD REAL-TIME SYSTEMS

***Tanmaya Mishra**, Thidapat Chantem, Ryan Gerdes, Virginia Polytechnic Institute and State University, Arlington, VA*

RISA: A SYSTOLIC ARRAY DESIGN REINFORCED WITH EMBEDDED TENSOR MANAGEMENT AND ACCELERATED DEPTHWISE CONVOLUTIONS

***Hyungmin Cho**, Sungkyunkwan University, Suwon, South Korea*

RVFPLIB: A FAST AND COMPACT OPEN-SOURCE FLOATING-POINT EMULATION LIBRARY FOR TINY RISC-V PROCESSORS

***Matteo Perotti**, Stefan Mach, Luca Bertaccini, Luca Benini, ETH Zürich, Zürich, Switzerland; Giuseppe Tagliavini, University of Bologna, Bologna, Italy*

SIMPLECHISEL: A HARDWARE DESIGN LANGUAGE FOR COMPONENT-LEVEL HETEROGENEOUS DESIGNS

***Shibo Chen**, University of Michigan, Ann Arbor, MI; Shibo Chen, Yonathan Fisseha, Jean-Baptiste Jeannin, Todd Austin, University of Michigan, Ann Arbor, MI*

TAPEOUT OF A RISC-V CRYPTO CHIP WITH HARDWARE TROJANS: A CASE-STUDY ON TROJAN DESIGN AND PRE-

SILICON DETECTABILITY

***Alexander Hepp**, Georg Sigl, Technische Universität Munich, Munich, Germany*

TOWARDS DEPLOYING PSS TO EARLY DESIGN SPACE EXPLORATION

***Frederik Kautz**, Christian Sauer, Cadence Design Systems, Inc., Munich, Germany; Holger Blume, Leibniz Universität Hannover, Hannover, Germany*

ZEM: ZERO-CYCLE BIT-MASKING MODULE FOR DEEP LEARNING REFRESH-LESS DRAM

*Duy-Thanh Nguyen, **Minh-Son Le**, Ik-Joon Chang, Kyung Hee University, Yongin, South Korea; Nhut-Minh Ho, Weng-Fai Wong, National University of Singapore, Singapore, Singapore*

MORE THAN MOORE BUT MORE SECURE? ON THE SECURITY CHALLENGES AND OPPORTUNITIES OF EMERGING TECHNOLOGIES

Time: 10:30 am – 12:00 pm
Room: 3020
Event Type: Special Session
Topic Area(s): Design, IP, Security

Chair/Co-Chair: Jeyavijayan Rajendran (Texas A&M University)

Session Organizer: Jeyavijayan Rajendran, Texas A&M University, College Station, TX

While CMOS logic is widely used for reliable and highly efficient systems, there are applications that call for devices in non-CMOS or non-traditional CMOS technologies. On the one hand, these novel device technologies need to be re-evaluated with respect to potential threats and attacks, and how these can be faced with existing and novel security solutions and methods. On the other hand, these emerging devices bring opportunities for building the secure systems of the future. In this paper, we will give an overview of three important device technologies and their security challenges and opportunities, namely memristors, thin-film transistors on plastic substrates, and CMOS logic in fully depleted silicon on insulator (FD-SOI) technology.

SECURITY BEYOND CMOS: OPPORTUNITIES AND CHALLENGES OF EMERGING DEVICES

Rosario Cammarota, Intel Corporation, San Diego, CA; Lejla Batina, Radboud University, Nijmegen, Netherlands; Nele Mentens, Leibniz Universität Hannover, Hannover, Germany ;Ahmad-Reza Sadeghi, Shaza Zeitouni, Technische Universität Darmstadt, Darmstadt, Germany ;Johanna Sepulveda, Airbus Defence and Space, Munich, Germany

ACCELERATING FULLY HOMOMORPHIC ENCRYPTION WITH PROCESSING IN MEMORY

Tajana Rosing, University of California, San Diego, La Jolla, CA

SECURITY PRIMITIVES WITH EMERGING MEMORIES

Giorgio Di Natale, Elena Ioana Vatajelu, TIMA Laboratory, Grenoble, France

KEYNOTE – JOE COSTELLO

Time: 8:45 am – 9:45 am
Room: 3008
Event Type: Visionary Talk

Mr. Costello is considered to have founded the EDA industry when in the late 1980s he became President of Cadence Design Systems, Inc. and drove annual revenues to over $1B—the first EDA company to achieve that milestone. In 2004, he was awarded the Phil Kaufman Award by the Electronic System Design Alliance in recognition of his business contributions that helped grow the EDA industry. After leaving Cadence, Joe has led numerous startups to successful exits such as Enlighted, Orb Networks, think3, and Altius. He received his BS in Physics from the Harvey Mudd College and also has a master's degree in Physics from both Yale University and UC Berkeley.

EXPLOIT YOUR MODULES FOR COMPLETE VERIFICATION

Time: 10:30 am – 11:30 am (Combined Session)
Room: 3016
Event Type: Research Session
Topic Area(s): EDA, Design Verification and Validation

Chair/Co-Chair: Pierluigi Nuzzo (University of Southern California), Co-Chair to be announced

This session presents innovations that can boost effectiveness, specificity, automation, and confidence in module-level verification. It contributes an efficient test-generation algorithm for dynamic verification of DRAMs based on deep reinforcement learning and a method based on graybox fuzzing for effective and rapid test generation targeting specific module instances in large RTL designs. The session then proceeds with a tool for automatically constructing formal testbenches using SystemVerilog assertions to aid verification of the control logic governing the interactions between design modules. Finally, it offers a system for efficiently certifying the correctness of first-order logic proofs in satisfiability modulo theories solvers.

AUTOSVA: DEMOCRATIZING FORMAL VERIFICATION OF RTL MODULE INTERACTIONS

***Marcelo Orenes-Vera**, Aninda Manocha, David Wentzlaff, Margaret Martonosi, Princeton University, Princeton, NJ*

THEORY-SPECIFIC PROOF STEPS WITNESSING CORRECTNESS OF SMT EXECUTIONS

*Rodrigo Otoni, Martin Blicha, Patrick Eugster, **Antti Hyvärinen**, Natasha Sharygina, Università della Svizzera italiana, Lugano, Switzerland*

VERIFICATION IS RUNNING: WHAT ARE THE NEXT STOPS?

Time: 11:30 am – 12:00 pm (Combined Session)
Room: 3016
Event Type: Research Session
Topic Area(s): EDA, Design Verification and Validation

Chair/Co-Chair: Jin Yang (Intel Corporation), Co-Chair to be announced

This session features advances in verification and testing to address increasing system complexity, security and emerging technologies.

It first proposes abstractions and mechanisms to detect bugs and vulnerabilities at system-level.

To this aim, trace notation for ISA definition is proposed for capture processor behaviors, while efficient extraction of reset-controlled events and concolic testing are used for detecting security vulnerabilities in SoC with asynchronous partial reset.

The session also addresses emerging directions in the verification of control systems based on neural networks and equivalence checking of quantum circuits. This is achieved by synthesizing barrier certificates of closed-loop systems controlled by neural networks and by employing tensor network contraction for computing the fidelity between an ideal quantum circuit and its noisy implementations.

ISA MODELING WITH TRACE NOTATION FOR CONTEXT FREE PROPERTY GENERATION

Keerthikumara Devarajegowda, *Endri Kaja, Sebastian Prebeck, Wolfgang Ecker, Infineon Technologies AG, Munich, Germany*

SCALING THE DATA WALL: NOVEL HETEROGENEOUS ARCHITECTURES FOR EMERGING DATA-INTENSIVE APPLICATIONS

Time: 10:30 am – 12:00 pm
Room: 3018
Event Type: Research Session
Topic Area(s): Design, SoC, Heterogeneous, and Reconfigurable Architectures

Chair/Co-Chair: Jack Wadden (University of Michigan), Co-Chair to be announced

With increasing acceleration of computing, data movement has become the major bottleneck in novel/upcoming applications in machine learning, graph analytics, stream processing etc. This session covers novel approaches for accelerating data movement across the design stack ranging from emerging technology to heterogeneous packaging, and domain-specific architectures. In particular, the papers in this session look towards application-driven insights to drive some of the underlying hardware design decisions in memory system design, reconfigurable architectures, photonic interconnections, chiplet-based designs, and 3D ICs.

HETEROGENEOUS MONOLITHIC 3D ICS: EDA SOLUTIONS, AND POWER, PERFORMANCE, COST TRADEOFFS

Sai Surya Kiran Pentapati, *Sung Kyu Lim, Georgia Institute of Technology, Atlanta, GA*

SCALING DEEP-LEARNING INFERENCE WITH CHIPLET-BASED ARCHITECTURE AND PHOTONIC INTERCONNECTS

Yuan Li, *Ahmed Louri, George Washington University, Washington, DC; Avinash Karanth, Ohio University, Athens, OH*

COSPARSE: A SOFTWARE AND HARDWARE RECONFIGURABLE SPMV FRAMEWORK FOR GRAPH ANALYTICS

Siying Feng, *Subhankar Pal, Xin He, Dong-hyeon Park, Trevor Mudge, Ronald Dreslinski, University of Michigan, Ann Arbor, MI; Jiawen Sun, Kuba Kaszyk, Magnus Morton, Murray Cole, Michael O'Boyle, University of Edinburgh, Edinburgh, United Kingdom*

GNNERATOR: A HARDWARE/SOFTWARE FRAMEWORK FOR ACCELERATING GRAPH NEURAL NETWORKS

Jacob R. Stevens, *Anand Raghunathan, Purdue University, West Lafayette, IN; Dipankar Das, Sasikanth Avancha, Bharat Kaul, Intel Corporation, Bangalore, India*

AN APPROXIMATE WORLD FROM NEURONS TO GENOMES

Time: 10:30 am – 12:00 pm
Room: 3014
Event Type: Research Session
Topic Area(s): Design, Approximate Computing for AI/ML

Chair/Co-Chair: Ahmedullah Aziz (University of Tennessee Knoxville)

The session features recent advancements in applying approximate computing techniques to different computing paradigms pertaining to Artificial Intelligence and Machine Learning, including hyperdimensional systems, spiking neural networks, probabilistic programming, and compressed video analytics. The techniques proposed include new encoding schemes, fixed-point quantization approaches, training methodologies, and compiler frameworks. The techniques have demonstrated significant improvement in both energy consumption and performance across various end-applications.

STATHEROS: COMPILER FOR EFFICIENT LOW-PRECISION PROBABILISTIC PROGRAMMING

***Jacob Laurel**, Rem Yang, Atharva Sehgal, Shubham Ugare, Sasa Misailovic, University of Illinois at Urbana-Champaign, Urbana-Champaign, IL*

TCL: AN ANN-TO-SNN CONVERSION WITH TRAINABLE CLIPPING LAYERS

***Nguyen-Dong Ho**, Ik-Joon Chang, Kyung Hee University, Yongin, South Korea*

SCALING UP HBM EFFICIENCY OF TOP-K SPMV FOR APPROXIMATE EMBEDDING SIMILARITY ON FPGAS

***Alberto Parravicini**, Luca Cellamare, Marco Siracusa, Marco Santambrogio, Politecnico di Milano, Milano, Italy*

EXACT NEURAL NETWORKS FROM INEXACT MULTIPLIERS VIA FIBONACCI WEIGHT ENCODING

***William Andrew Simon**, Valérian Rey, Alexandre Levisse, Giovanni Ansaloni, David Atienza, École polytechnique fédérale de Lausanne, Lausanne, Switzerland; Marina Zapater, Haute Ecole d'Ingénierie et de Gestion du Canton de Vaud, Yverdon-les-Bains, France*

A-EYE ON THE CUTTING EDGE OF IOT

Time: 2:10 pm – 2:30 pm (Combined Session)
Room: 3018
Event Type: Research Session
Topic Area(s): Embedded Systems, Embedded System Design Methodologies

Chair/Co-Chair: Steve Kommrusch (Colorado State University), Co-Chair to be announced

This session covers cutting edge research to integrate artificial intelligence (AI) across edge, smart building, and medical IoT devices. The first two papers focus on latency and sparsity optimizations in edge computing devices. The third paper focuses on prioritizing user comfort and energy efficiency in smart building environments. The last paper presents a timely approach to detect ventricular arrhythmias with low power medical devices, to help deliver in-time defibrillation.

MYML: USER-DRIVEN MACHINE LEARNING

***Vidushi Goyal**, Valeria Bertacco, Reetuparna Das, University of Michigan, Ann Arbor, MI*

TUNE IN TO THE CLOCKS!

Thank You to Our Sponsor PERFORCE

Time: 10:30 am – 11:30 am
Room: 2008
Event Type: Designer, IP and Embedded Systems Track Presentations
Topic Area(s): Back-End Design

Chair/Co-Chair: Janam Trivedi (Facebook)

Clock design continues to be an important aspect of the overall chip design. In this session, you would come across some novel techniques used to resolve challenges in clock design during chip development.

USING CLOCK SKEW TO FIX HOLD: A PATH-DEPTH BASED USEFUL-SKEW APPROACH TO REDUCE HOLD BUFFER INSERTION

***Eliot Gerstner**, Cadence Design Systems, Inc., Saratoga, NY*

CLOCKING METHODS WITH FOCUS ON PCIE GEN4

***Patricia Fong**, Bertram Bradley, Shivani Pandya, Marvell Semiconductor, Santa Clara, CA*

ECO PATCH GENERATION & STITCHING TO FACILITATE CONCURRENT ECOS IN HIGH PERFORMANCE PROCESSOR DESIGNS

*Abhilash Belagur, George Antony, Ashish Jaitly, Naiju Karim, IBM, Bangalore, India; **Joel Earl**, IBM, Rochester, NY*

UVM: WHERE THE WILD THINGS ARE

Thank You to Our Sponsor SIEMENS

Time: 10:30 am – 12:00 pm
Room: 2010/2012
Event Type: Designer, IP and Embedded Systems Track Panels
Topic Area(s): Front-End Design

Chair/Co-Chair: Tom Fitzpatrick (Siemens EDA)

Session Organizers: Tom Fitzpatrick, Siemens EDA, Marlborough, MA

This panel will focus on specific enhancements being planned or considered to be added for the next revision of UVM IEEE 1800.2.

Moderator: Dennis Brophy, Siemens EDA, Wilsonville, OR

Panelists: Mark Glasser, Cerebras, Soquel, CA; Cliff Cummings, Paradigm Works, Provo, UT Hillel Miller, Synopsys, Austin, TX; Jamsheed Agahi, Semifore, Palo Alto, CA

TECHTALK: THE AI HYPE CYCLE IS OVER. NOW WHAT?

Time: 11:30 am – 12:30 pm
Room: DAC Pavilion
Event Type: Tech Talk

The expectations around AI and ML have been enormous, which fueled investment and innovation as companies scrambled for scalable approaches to building and deploying AI and ML solutions. Experimentation, in both hardware and software, has been the order of the day:

- Ramping up the core technology to improve accuracy and take on more use cases.
- Experimenting with the technology (models and processors) to understand what was possible, what worked, what didn't and why.

The exuberance of the moment, however, created some unintended consequences. Take, for example, a fully parameterized, complex Transformer network. In an analysis by Northeastern University, the 300 million parameter model took 300 tons of carbon to train. Since then, accuracy and efficiency have improved gradually.

Today, as the shouting dies down, the biggest trend - one that is having profound effects in helping teams innovate - is around hardware. The days of general-purpose hardware anchoring AI and ML are quickly giving way to specialized compute that allows engineers to not only tune their solutions for accuracy and efficiency but deploy their solutions more effectively across the compute spectrum. Industry veteran Steve Roddy, head of AI and ML product for Arm, will describe how a new era of democratized design is accelerating innovation in AI and design teams who embrace are speeding ahead of the pack.

Speaker: Steve Roddy, Arm Ltd., Austin, TX

LUNCH AND LEARN: PYTHON FOR SCIENTIFIC COMPUTING AND DEEP LEARNING (PRE-REGISTRATION REQUIRED)

Time: 12:15 pm – 1:15 pm
Room: 3001
Event Type: Lunch and Learn

As well as being a general-purpose programming and scripting language, Python has become one of the most popular languages for scientific computing and more recently for deep learning. Python is everywhere, and Python is cool.

Python is easy to learn, and Python programs are very readable, even by people who don't know Python. There are Python libraries available for doing pretty much anything.

In this tutorial you will learn enough to start using Python as a scripting language and you will become sufficiently familiar with Python to start making sense of the emerging libraries and frameworks used for deep learning, such as TensorFlow and Keras. This tutorial will show you some of the cool things you can do with Python right out-of-the-box!

You can learn more about the Python language and about Deep Learning in the morning and afternoon sessions on 'Thursday is Training Day'.

SKY TALK: CROSS-DISCIPLINARY INNOVATIONS REQUIRED FOR THE FUTURE OF COMPUTING

Time: 1:00 pm – 1:45 pm
Room: DAC Pavilion
Event Type: SKY Talk

With traditional drivers of compute performance a thing of the past, innovative engineers are tapping into new vectors of improvement to meet the world's demand for computation. Like never before, the future of computing will be owned by those who can optimize across the previously siloed domains of silicon design, processor architecture, package technology and software algorithms to deliver performance gains with new capabilities. These approaches will derive performance and power efficiency through tailoring of the architecture to particular workloads and market segments, leveraging the much greater performance/Watt and performance/area of accelerated solutions. Designing and verifying multiple tailored solutions for markets where a less efficient general purpose design formerly sufficed can be accomplished through modular architectures using 2.5D and 3D packaging approaches. Delivering on modular solutions for high volume markets requires simultaneously optimizing across packaging, silicon, interconnect technologies where in the past, silicon design was sufficient. This talk will cover these trends with the vectors of innovation required to deliver these next generation compute platforms.

Speaker: Sam Naffziger, AMD, Fort Collins, CO

KEEP YOUR SECRETS SAFE: SIDE-CHANNEL ATTACKS AND ASSESSMENT TECHNIQUES

Time: 1:30 pm – 2:10 pm (Combined Session)
Room: 3018
Event Type: Research Session
Topic Area(s): Hardware Security: Attack and Defense, Security

Chair/Co-Chair: To be announced

Side-channel attacks (SCA) have become an important challenge in the design of protected devices. This session focuses on side-channel attack techniques and methodologies to analyze cryptographic hardware implementations. The first half of the session explores SCA attacks on NIST's Round-3 post-quantum digital signature standard finalist FALCON and modern processors using the micro-architectural state held by predictors. The third paper presents a novel methodology to perform cross-device profiling of power and EM attacks with the help of meta transfer learning. The session further explores a pre-silicon SCA resistance assessment at the RTL stage to offer significant speed-up on security evaluations.

FALCON DOWN: BREAKING THE FALCON POST-QUANTUM SIGNATURE SCHEME THROUGH SIDE-CHANNEL ATTACKS

***Emre Karabulut**, Aydin Aysu, North Carolina State University, Raleigh, NC*

PSC-TG: RTL POWER SIDE-CHANNEL LEAKAGE ASSESSMENT WITH TEST PATTERN GENERATION

***Tao Zhang**, Jungmin Park, Mark Tehranipoor, Farimah Farahmandi, University of Florida, Gainesville, FL*

PANDA OR GIBBON AND BACK: ATTACKING AND DEFENDING MODERN MACHINE LEARNING SYSTEMS

Time: 1:30 pm – 3:00 pm (Combined Session)
Room: 3014
Event Type: Research Session
Topic Area(s): Hardware Security: Attack and Defense, Security

Chair/Co-Chair: To be announced

Machine learning, particularly deep neural networks, have been adopted in diverse applications for classification and object detection with exceptional performance. However, the research community has developed powerful attacks on models. The papers in this session include both novel attacks and defenses for machine learning models. One paper presents an adversarial attack against models that process 3D point clouds, typically found in autonomous systems; the second presents a model inversion attack on hyper-dimensional models, which leads to compromise of the training data; the other two papers illustrate how recently proposed in-memory computing systems have built-in defense mechanisms against adversarial attacks.

ON THE INTRINSIC ROBUSTNESS OF NVM CROSSBARS AGAINST ADVERSARIAL ATTACKS

***Deboleena Roy**, Indranil Chakraborty, Timur Ibrayev, Kaushik Roy, Purdue University, West Lafayette, IN*

3D-ADV: BLACK-BOX PHYSICAL ADVERSARIAL ATTACKS AGAINST DEEP LEARNING MODELS THROUGH 3D SENSORS

***Kaichen Yang**, Yier Jin, University of Florida, Gainesville, FL; Xuan-Yi Lin, Tsung-Yi Ho, National Tsing Hua University, Hsinchu, Taiwan; Yixin Sun, Huazhong University of Science and Technology, Wuhan, China*

LEVERAGING VARIABILITY AND AGGRESSIVE QUANTIZATION OF IN-MEMORY COMPUTING FOR ROBUSTNESS IMPROVEMENT OF DEEP NEURAL NETWORK HARDWARE AGAINST ADVERSARIAL INPUT AND WEIGHT ATTACKS

***Sai Kiran Cherupally**, Adnan Rakin, Shihui Yin, Deliang Fan, Jae-sun Seo, Arizona State University, Tempe, AZ; Mingoo Seok, Columbia University, New York, NY*

SMARTER SOFTWARE FRAMEWORKS FOR EASIER ML DEVELOPMENT

Time: 1:30 pm – 2:35 pm (Combined Session)
Room: 3016
Event Type: Research Session
Topic Area(s): Design, AI/ML System Design

Chair/Co-Chair: To be announced

It is always painful and difficult for software engineers with little ML background to craft a high performance and efficient ML system. This session presents a collection of novel software frameworks for improving the productivity of ML practitioners by assisting the development of high-performance ML accelerators, novel ML algorithms, and emerging ML applications.

INSTANTNET: AUTOMATED GENERATION AND DEPLOYMENT OF INSTANTANEOUSLY SWITCHABLE-PRECISION NETWORKS

***Yonggan Fu**, Zhongzhi Yu, Yongan Zhang, Chaojian Li, Mingchao Jiang, Yingyan Lin, Rice University, Houston, TX; Yifan Jiang, Zhangyang Wang, The University of Texas at Austin, Austin, TX; Yongyuan Liang, Sun Yat-sen University, Beijing, China*

GEMMINI: ENABLING SYSTEMATIC DEEP-LEARNING ARCHITECTURE EVALUATION VIA FULL-STACK INTEGRATION*

***Hasan N. Genc**, Seah Kim, Alon Amid, Ameer Haj-Ali, Vighnesh Iyer, Pranav Prakash, Jerry Zhao, Daniel Grubb, Harrison Liew, Howard Mao, Albert Ou, Colin Schmidt, Samuel Steffl, John Wright, Ion Stoica, Krste Asanovic, Borivoje Nikolic, Yakun Sophia Shao, University of California, Berkeley, Berkeley, CA; Jonathan Ragan-Kelley, Massachusetts Institute of Technology, Cambridge, MA*

HARDWARE ACCELERATORS FOR CODEC AVATAR DECODING

***Xiaofan Zhang**, Deming Chen, University of Illinois at Urbana-Champaign, Urbana-Champaign, IL; Dawei Wang, Shugao Ma, Yuecheng Li, Facebook Reality Lab, Pittsburgh, PA; Pierce Chuang, Facebook Reality Lab, Menlo Park, CA*

LEARNING TO ACCELERATE CIRCUIT TIMING ANALYSIS

Time: 2:35 pm – 3:00 pm (Combined Session)
Room: 3016
Event Type: Research Session
Topic Area(s): EDA, Digital Design, Timing and Simulation

Chair/Co-Chair: Murthy Palla (Synopsys), Co-Chair to be announced

This session presents advanced methods for circuit timing analysis and optimization. The first two papers use new algorithms, data structures, and machine-level optimizations for improving the efficiency of common path pessimism removal (CPPR) problem and path-based timing analysis. The last two papers use machine learning techniques for learning resistor networks from linear measurements and for gate sizing.

RL-SIZER: VLSI GATE SIZING FOR TIMING OPTIMIZATION USING DEEP REINFORCEMENT LEARNING

***Yi-Chen Lu**, Sung Kyu Lim, Georgia Institute of Technology, Atlanta, GA; Siddhartha Nath, Vishal Khandelwal, Synopsys, Mountain View, CA*

UVM IS 10 YEARS OLD: WHAT'S NEXT?

Thank You to Our Sponsor SIEMENS

Time: 1:30 pm – 3:00 pm
Room: 2010/2012
Event Type: Designer, IP and Embedded Systems Track Presentations
Topic Area(s): Front-End Design

Chair/Co-Chair: Dennis Brophy (Siemens EDA)

Session Organizer: Tom Fitzpatrick, Siemens EDA

The Universal Verification Methodology (UVM) is now 10 years old. In the past decade, the UVM ecosystem has grown to dominance of our industry, but what about the next 10 years? Verification looks very different today than it did 10 years ago. We are now facing a substantial amount of software content as an integral piece of the overall SoC functionality, and SoC size and complexity is outstripping simulators' ability to randomly generate the right stimulus sequences to cover all of the corner cases where bugs lie. There is also the need to be able to staff verification teams to take advantage of UVM as the next generation of verification engineers comes of age. How do we keep UVM relevant and build on its success such that we can continue to rely on the great work done so far as verification itself progresses along with ever-growing SoC complexitly?

Presenter(s): John Aynsley, Doulos, Hampshire, United Kingdom; Ray Salemi, Siemens EDA, Boston, MA; Jason Sprott, Verilab, Edinburgh, United Kingdom

IDENTIFYING SECURITY WEAKNESSES IN ELECTRONIC DESIGNS USING A STANDARDIZED METHODOLOGY

Thank You to Our Sponsor PERFORCE

Time: 1:30 pm – 3:00 pm
Room: 2008
Event Type: Designer, IP and Embedded Systems Track Presentations
Topic Area(s): IP

Chair/Co-Chair: John Hallman (Tortuga Logic); Jason Oberg (onespin)

Session Organizers: Mike Borza, Synopsys, Ottawa, Canada; Jason Fung, Intel Corporation, Hillsboro, OH; Vishal Moondhra, perforce, Santa Clara, CA; Anders Nordstrom, Tortuga Logic, Ottawa, Canada; Jason Oberg, Tortugalogic, San Jose, CA

According to the National Vulnerability Database, there has been an exponential growth in hardware vulnerabilities over the last few years. These exploits are becoming more widespread, dangerous, and costly than ever and are coming from multiple attack vectors. With many being remotely exploitable such the widely publicized Spectre and Meltdown attacks, the impact of an attack can be enormous.

In this 90-minute Tutorial we will address the concerns mentioned above by focusing on the following topics, along with some demonstrations:

- Intro to Accellera's Security Annotation for Electronic Design Integration (SA-EDI)
- MITRE's Hardware Common Weakness Enumerations
- Hardware Assurance Database and Sharing
- Demonstrations that showcase the SA-EDI with Weakness Enumerations:
- OneSpin/Perforce
- Tortuga Logic

Speakers: John Hallman, Onespin Solutions, San Jose, CA; Anders Nordstrom, Jason Oberg, Tortugalogic, Ottawa, Canada; Jason Fung, Intel Corporation, Portland, OR John Hallman, Onespin Solutions, Melbourne, FL Mike Borza, Synopsys, Ottawa, Canada Jeremy Bellay, Battelle, Columbus, OH

DESIGN AND VERIFICATION ENGINEER 2.0-A NEW GENERATION OR A PIPE DREAM?

Time: 2:00 pm – 2:45 pm
Room: DAC Pavilion
Event Type: DAC Pavilion Panels
Topic Area(s):

Session Organizer: John Blyler, DesignNews, Portland, OR

The tremendous advances in Integrated Circuit (IC) Design that have spawned amazing innovation have also increased the complexity of Design Verification (DV).

DV today takes up more than half the time and cost of designing an IC. Additionally, DV requires a significant amount of engineering talent, simply put, there just aren't enough DV engineers being produced to meet this demand.

To address the future challenges of verification, DV engineers must reinvent themselves and evolve into the DV Engineer 2.0. In this panel we will debate if ML/AI and Software 2.0 – the move toward a more abstracted way of designing electronics chips and systems – will play a role in helping the Design and Verification Engineer 2.0 to take on the challenge of reducing the cost and time of design and verification, while challenging the traditional Software 1.0 stack. Our debate will include the following areas:

- Deep Neural Network (DNN) Models and Software 2.0
- Functional Verification and Coverage improvement using ML
- Formal Verification
- Language models
- Machine Learning Model Deployment in Production
- How EDA companies need to evolve to meet these new challengers

With the proliferation of Software 2.0 and Machine Learning, will the Design and Verification Engineer 2.0 be twice as productive as they are today? Will they acquire the skill sets to model complex algorithms using Machine Learning Models and challenge traditional software 1.0 from EDA companies? We'll offer a multitude of expert perspectives.

Moderator: Duaine Pryor, Siemens EDA, Menlo Park, CA

Speakers: Sandeep Srinivasan, VerifAI Inc., San Francisco, CA; Aman Joshi, Western Digital, Palo Alto, CA; Sashi Obilisetty, Synopsys, Santa Clara, CA

HANDLING SOC VERIFICATION: CHANGING THE PARADIGM IN VERIFICATION APPROACHES

Time: 3:00 pm – 3:45 pm
Room: DAC Pavilion
Event Type: DAC Pavilion Panels
Topic Area(s):

Organizer: Balachandran Rajendran, Dell EMC, Seattle, WA

Modern SoC complexity is driving a new verification frontier. The verification of an SoC has always been a departure from the more standardized techniques employed in large block or sub-system, both in terms of test requirements as well as sheer complexity and size. However, new issues such as safety, security, processor instruction flexibility layered on top of advanced applications including 5G, AI, Quantum Computing, etc. have driven the need for different thinking.

Simulators, emulators and formal-based apps are essential tools in the verification teams' armament. But what is the most effective way to augment the core capabilities to deliver these intensely complex chips on time? For example, do we invest in accelerating test content production through techniques such as Portable Stimulus. Or should the focus be on additional and advanced static verification methods.

Moderator Brian Bailey, technology editor/EDA for Semiconductor Engineering, will lead two well-known, senior engineers who are responsible for next generation verification flow development. They will consider and discuss next generation needs and the directions they can take. Two vendor CEOs will attempt to address those needs and explain why their method is the most effective use of time and budget.

Come and witness an animated and lively discussion as we watch an open and frank conversation, often held behind closed doors in many semiconductor and electronic systems companies.

Moderator: Brian Bailey, Semiconductor Engineering, Beaverton, OR; Speakers: Mike Chin, Intel Corporation, Concord, CA; David Kelf, Breker Verification Systems, San Jose, CA; Jason Xing, Empyrean Technology, San Jose, CA; Adnan Hamid, Breker Verification Systems, Fremont, CA

SECURITY-AWARE COMPUTER AIDED ELECTRONIC DESIGN

Time: 3:30 pm – 5:00 pm
Room: 3002
Event Type: Special Session
Topic Area(s): Security

Chair/Co-Chair: Ujjwal Guin (Auburn University)

Session Organizer: Ujjwal Guin, Auburn University, Auburn, AL

Due to the lack of standard tools, methods, or solutions currently in practice, there is an urgent need for developing chip-level security solutions. The primary reason for the lack of security features in a chip has resulted from the economic hurdles and technical trade-offs often associated with chip design. This special session will highlight these concerns and opportunities. The first presentation will be an overview of the benefits of the security-aware CAD flows and discuss the attack surfaces such as side-channel attacks, reverse engineering, supply chain attacks, and malicious hardware attacks that need to be addressed. The second talk will focus on Security-Aware Computer-Aided Electronic Design Tools. The third talk will focus on Independent Verification & Validation (IV&V) of Security-Aware CAD tools. The final talk will discuss the Integration of IC Design Changes into a BlockChain for Traceability in the Electronic CAD Flow.

VISION OF AUTOMATING THE IMPLEMENTATION OF SECURITY INTO SILICON

***Serge Leef**, DARPA, Washington, DC*

END-TO-END SECURE SOC LIFECYCLE MANAGEMENT

*Mike Borza, Synopsys, Ottawa, Canada; Fahim Rahman, University of Florida, Gainesville, FL; Md Sami Ul Islam Sami, Farimah Farahmandi, **Mark Tehranipoor**, University of Florida, Gainesville, FL; Adam Cron, Synopsys, Hilton Head Island, SC*

INDEPENDENT VERIFICATION AND VALIDATION OF SECURITY-AWARE EDA TOOLS AND IP

*Benjamin Tan, New York University, New York City, NY; **Warren Savage**, Yuntao Liu, Michael Zuzak, Abhishek Chakraborty, Ankur Srivastava, Omid Aramoon, Qian Xu, Gang Qu, University of Maryland, College Park, MD; Siddharth Garg, Ramesh Karri, New York University, New York City, NY Adam Porter, Jeno Szep, Fraunhofer USA, College Park, MD*

LOGIC SYNTHESIS GOT EVEN BETTER. CAN YOU BELIEVE IT? MACHINE LEARNING TO THE RESCUE

Time: 3:30 pm – 5:00 pm
Room: 3016
Event Type: Research Session
Topic Area(s): EDA, RTL/Logic Level and High-level Synthesis

Chair/Co-Chair: Christian Pilato (Politecnico di Milano)

The use of machine learning in EDA is deeply impacting the field. In this session we show how machine learning (ML) techniques are used to improve logic synthesis. The first paper uses reinforcement learning to design parallel prefix circuits such as adders and priority encoders that are fundamental in high-performance circuits, while the second paper uses ML to develop a novel technology mapping algorithm. The third paper proposes a framework to generate hardware accelerators for tensor algebra application. The next paper applies FPGA-based synthesis methods to ASIC synthesis. Finally, the last two papers present methods to efficient simulate complex problems. In particular the tight integration between the circuit simulation and a Boolean satisfiability solver, and a cycle-accurate simulation models with RTL models.

PREFIXRL: OPTIMIZATION OF PARALLEL PREFIX CIRCUITS USING DEEP REINFORCEMENT LEARNING

***Rajarshi Roy**, Jonathan Raiman, Neel Kant, Ilyas Elkin, Robert Kirby, Michael Siu, Stuart Oberman, Saad Godil, Bryan Catanzaro, NVIDIA, Santa Clara, CA*

SLAP: A SUPERVISED LEARNING APPROACH FOR PRIORITY CUTS TECHNOLOGY MAPPING

***Walter Lau Neto**, Yingjie Li, Cunxi Yu, Pierre-Emmanuel Gaillardon, University of Utah, Salt Lake City, UT; Matheus Trevisan Moreira, Chronos Tech, San Diego, CA; Luca Amaru, Synopsys, Sunnyvale, CA*

LUT-BASED OPTIMIZATION FOR ASIC DESIGN FLOW

***Luca Amaru**, Vinicius Possani, Eleonora Testa, Felipe Marranghello, Christopher Casares, Jiong Luo, Patrick Vuillod, Synopsys, Sunnyvale, CA; Alan Mishchenko, University of California, Berkeley, Berkeley, CA; Giovanni De Micheli, École polytechnique fédérale de Lausanne, Lausanne, Switzerland*

UMOC: UNIFIED MODULAR ORDERING CONSTRAINTS TO UNIFY CYCLE- AND REGISTER-TRANSFER-LEVEL MODELING

*Shunning Jiang, **Yanghui Ou**, Peitian Pan, Christopher Batten, Cornell University, Ithaca, NY*

RELIABILITY FROM FAB TO MISSION

Time: 3:30 pm – 5:00 pm
Room: 3018
Event Type: Research Session
Topic Area(s): EDA, Manufacturing Test and Reliability

Chair/Co-Chair: Liu Cheng (Chinese Academy of Sciences, University of Chinese Academy of Sciences), Co-Chair to be announced

As CMOS scaling continues deeper into the nanometer scale and new device technologies proliferate to enhance performance, reliability of products through their lifetime is an increasing concern. This session presents analysis and mitigation methods to prevent and detect wearout based failures for a variety of technologies, ranging from analog, digital, and mixed signal devices to memristors.

REVERSIBLE GATING ARCHITECTURE FOR RARE FAILURE DETECTION OF ANALOG AND MIXED-SIGNAL CIRCUITS

*Myung Seok Shim, Texas A&M University, College Station, TX; **Hanbin Hu**, Peng Li, University of California, Santa Barbara, Santa Barbara, CA*

LOW-COST LITHOGRAPHY HOTSPOT DETECTION WITH ACTIVE ENTROPY SAMPLING AND MODEL CALIBRATION

***Yifeng Xiao**, Jianli Chen, Jun Yu, Fudan University, Shanghai, China; Miaodi Su, Fuzhou University, Fuzhou, China; Haoyu Yang, Bei Yu, The Chinese University of Hong Kong, Hong Kong, Hong Kong*

A NEW, COMPUTATIONALLY EFFICIENT "BLECH CRITERION" FOR IMMORTALITY IN GENERAL INTERCONNECTS

***Mohammad Abdullah Al Shohel**, Vidya A. Chhabria, Sachin S. Sapatnekar, University of Minnesota, Minneapolis, MN*

EMGRAPH: FAST LEARNING-BASED ELECTROMIGRATION ANALYSIS FOR MULTI-SEGMENT INTERCONNECT USING GRAPH CONVOLUTION NETWORKS

***Wentian Jin**, Liang Chen, Sheriff Sadiqbatcha, Shaoyi Peng,Sheldon X.-D. Tan, University of California, Riverside, Riverside, CA*

SECURITY TECHNIQUES ACROSS THE BOARD (STAB)

Time: 3:30 pm – 5:05 pm (Combined Session)
Room: 3014
Event Type: Research Session
Topic Area(s): Embedded and Cross-Layer Security, Security

Chair/Co-Chair: Aydin Aysu (North Carolina State University), Co-Chair to be announced

This session presents security defenses and attacks across a range of abstraction layers. The first two papers present machine learning techniques to hardware-based malware detection. The first paper's approach estimates and reduces uncertainty in the detection process and the second paper presents a collaborative federated learning approach. The next two papers investigate side-channel attacks, proposing an architecture to obfuscate timing side-channels and presenting a new interruption-based side-channel attack against a secure enclave. The next paper presents a Network-on-Chip architecture to defend cloud services. The final paper presents a method to detect confidentiality vulnerabilities in mixed hardware/firmware systems using formal verification.

TOWARDS IMPROVING THE TRUSTWORTHINESS OF HARDWARE BASED MALWARE DETECTOR USING ONLINE UNCERTAINTY ESTIMATION

***Harshit Kumar**, Nikhil Chawla, Saibal Mukhopadhyay, Georgia Institute of Technology, Atlanta, GA*

DISTRIBUTED MEMORY GUARD: ENABLING SECURE ENCLAVE COMPUTING IN NOC-BASED ARCHITECTURES

*Ghada Dessouky, Pouya Mahmoody, Ahmad-Reza Sadeghi, Emmanuel Stapf, Shaza Zeitouni, Technische Universität Darmstadt, Darmstadt, Germany; **Mihailo Isakov**, Michel A. Kinsy, Miguel Mark, Texas A&M University, College Station, TX*

A FORMAL APPROACH TO CONFIDENTIALITY VERIFICATION IN SOCS AT THE REGISTER TRANSFER LEVEL

***Johannes Müller**, Mohammad Rahmani Fadiheh, Anna Lena Duque Antón, Dominik Stoffel, Wolfgang Kunz, Technische Universität Kaiserslautern, Kaiserslautern, Germany; Thomas Eisenbarth, Universität zu Lübeck, Lübeck, Germany*

EMBEDDED RECIPES FOR SECURE AND BUG-FREE SOUPS

Time: 5:05 pm – 5:30 pm (Combined Session)
Room: 3014
Event Type: Research Session
Topic Area(s): Embedded and Cross-Layer Security, Security

Chair/Co-Chair: Jiafeng Xie (Villanova University)

This session considers building trust in embedded systems, which have become pervasive but also increasingly more complex. The emerging eco-system of embedded devices resembles a delicious soup with several ingredients which at the same time is threatened by a variety of bugs and security attacks - bugs love swimming in fancy soups and the bowl is large! The papers in the session include secure methodologies for memory safety, application-specific attacks and defenses, trusted executions, and legacy code protection.

DIALED: DATA INTEGRITY ATTESTATION FOR LOW-END EMBEDDED DEVICES

*Ivan De Oliveira Nunes, **Sashidhar Jakkamsetti**, Gene Tsudik, University of California, Irvine, Irvine, CA*

WEDNESDAY DESIGNER, IP AND EMBEDDED SYSTEMS TRACK POSTERS

Time: 5:00 pm – 6:00 pm
Room: Exhibit Hall Level 2
Event Type: Designer, IP and Embedded Systems Track Poster Networking Reception

ALGORITHM TO RTL: A FASTER PATH TO IMPLEMENTATION

Russell Klein, Siemens EDA, Wilsonville, OR; Anoop Saha, Siemens EDA, Fremont, CA

ATTAINING CONSISTENT RTL QUALITY AND IMPROVING DEVELOPMENT CYCLES WITH GIT CONTINUOUS INTEGRATION TOOLS

***Michael Craren**, General Dynamics Mission Systems, Dedham, MA; Brinda Vokkarane, Siemens EDA, Boston, MA; Chris Giles, Siemens EDA, Longmont, CO*

EFFICIENT HIGH-SIGMA VERIFICATION OF STANDARD CELL LIBRARIES

***Andrew Evans**, Adesh Namekumar, Arm Ltd., Austin, TX; Ajay Chopra, Arm Ltd., Bangalore, India; Mike Sheinin, Siemens EDA, Saskatoon, Canada; Nebabie Kebebew, Siemens EDA, Fremont, CA*

ENHANCED HYPERSCALING OF DATA CENTERS USING IN-CHIP MONITORING & SENSING FABRICS

*Stephen Crosher, Synopsys, Plymouth, United Kingdom; Ramsay Allen, Synopsys, Devon, United Kingdom; **Firooz Massoudi**, Synopsys*

EXPEDITING DATA CONVERTER LAYOUTS USING DESIGN PLANNING & ANALYSIS (DPA) AUTOMATION

*Atul Bhargava, Monika Lilani, STMicroelectronics, Greater Noida, India; **Colin Thomson**, Cadence Design Systems, Inc., Edinburgh, United Kingdom; Vishesh Kumar, Cadence Design Systems, Inc., Noida, India; **Marc Swinnen**, Ansys*

FAST AND ACCURATE DVD AWARE TIMING ANALYSIS

*Minseok Kang, Seonghun Jeong, Yongho Lee, Samsung Electronics, Hwaseong, South Korea; Vinayakam Subramanian, Krishnakanth Gilakamsetti, Ansys, Bangalore, India; Jonghyun Lim, Ansys, Seoul, South Korea; **Marc Swinnen**, Ansys*

FAST TRACKING A FEDERAL AUTHENTICATION SOLUTION FOR SECURE FACILITIES

***Edward Garcia**, Comark, Milford, MA*

HYBRID EMULATION METHODOLOGY FOR SSD DESIGN

Byeongwook Bae, Seunghan Lee, Sangho Park, JaeWoo Im, Jungyun Choi, Kyungsu Kang, Byunghoon Lee, SungGil Lee, Samsung Electronics, Hwaseong, South Korea

A LOW COST, SCALABLE AND PREDICTABLE GATE LEVEL SIMULATION METHODOLOGY FOR GIGA-SCALE SOCS

*Satish Kumar Rompicharla, Nilay R. Desai, Anil K. Jonnalagadda, **Miklesh Naicker**, Intel, Bangalore, India*

MACHINE LEARNING ASSISTED DESIGN RULE DEBUG AND RULE RANKING AUTOMATION

***Hui Fu**, Intel Corporation, Austin, TX*

MODERNIZING PUBLIC INFRASTRUCTURE WITH INTERACTIVE DEVICES

***Ken Gray**, Comark, Milford, MA*

MULTI-PHYSICS SIMULATION TECHNIQUES TOWARD ELECTROMAGNETIC SIDE-CHANNEL ATTACK ASSESSMENTS ON IC CHIP ASSEMBLY

*Kazuki Monta, Makoto Nagata, Kobe University, Kobe, Japan; **Lang Lin**, Jimin Wen, Deqi Zhu, Calvin Chow, Norman Chang, Ansys, San Jose, CA*

OPTIMIZING HOLD ECO USING ML TECHNIQUES

***Akarsh Agrawal**, Mangesh Deshmukh, Divya Yogi, Intel Technology India Pvt. Ltd., Bengaluru, India*

PIONEERING LOW POWER MODELING AND VERIFICATION TECHNIQUE FOR CUSTOM BLOCKS

***Archanna Srinivasan**, Intel Corporation, San Jose, CA; Mei War Kan, Intel Corporation, Georgetown, Malaysia*

PREDICTING TIMING BOTTLENECKS IN PLACE & ROUTE USING MACHINE LEARNING

*Harn Hua Ng, **Hichem Belhadj**, Plunify, Singapore, Singapore*

PRIORITY SYNTHESIS IN PHYSICAL SYNTHESIS

*Nancy Y. Zhou, IBM Systems, Austin, TX; **Lakshmi Reddy**, IBM Research, Yorktown Heights, NY; Alex Suess, Cindy Washburn, Josiah Hamilton, IBM Systems, Poughkeepsie, NY; Jeffrey Brownscheidle, IBM Systems, Seattle, WA*

RETHINKING NEW PRODUCT INTRODUCTION TO BETTER ALIGN TO CLIENT NEEDS

***Dale Hackathorn**, Comark, Milford, MA*

ROOT-CAUSE ANALYSIS OF UNDEFINED SLACK USING TIMING/NETLIST DATA MODEL

Shesha Raghunathan, Anshul ., Prashansha Gupta, IBM, Bengaluru, India

SHIFT-LEFT POST-SILICON VERIFICATION WITH SPEED AND ACCURACY

*Jitendra Aggarwal, **Oscar Monroy**, Arm Ltd., Austin, TX*

A SPRING MODEL APPROACH FOR TIMING BUDGET APPORTIONMENT

***Tsz-mei Ko**, IBM, Poughkeepsie, NY*

STRESS TESTING TO SURVIVE AN INDUSTRIAL GAS TURBINE

***Timothy McNamara**, Comark, Milford, MA*

USING CLOCK SKEW TO FIX HOLD: A PATH-DEPTH BASED USEFUL-SKEW APPROACH TO REDUCE HOLD BUFFER INSERTION

***Eliot Gerstne**, Cadence Design Systems, Inc., Saratoga, NY*

WEDNESDAY LATE BREAKING RESULTS POSTERS

Time: 6:00 pm – 7:00 pm
Room: Level 2 Foyer
Event Type: Late Breaking Results Poster, Networking Reception

ATTENTION IN GRAPH2SEQ NEURAL NETWORKS TOWARDS PUSH-BUTTON ANALOG IC PLACEMENT

António Gusmão, Nuno Horta, Nuno Lourenço, ***Ricardo Martins****, Instituto Nacional de Telecomunicações, Lisboa, Portugal*

AN EFFECTIVE LEGALIZATION ALGORITHM FOR HETEROGENEOUS FPGAS WITH COMPLEX CONSTRAINTS

Zhipeng Huang*, Fuzhou University, Fuzhou, China; Haokai Sun, East China Normal University, Shanghai, China; Huimin Wang, Jun Yu, Jianli Chen, Fudan University, Shanghai, China; Ziran Zhu, Southeast University, Nanjing, China*

HETEROGENEOUS CIRCUIT LAYOUT CENTERLINE EXTRACTION FOR MASK VERIFICATION

Xiqiong Bai*, Peng Zou, Fuzhou University, Fuzhou, China; Ziran Zhu, Southeast University, Nanjing, China; Lichong Sun, Huawei Technologies Company Ltd., Hangzhou, China; Jianli Chen, Fudan University, Shanghai, China*

INCREMENTAL 3D GLOBAL ROUTING CONSIDERING CELL MOVEMENT

Peng Zou*, Chenyue Ma, Jun Yu, Jianli Chen, Fudan University, Shanghai, China; Zhifeng Lin, Fuzhou University, Fuzhou, China*

NOVEL DISCRETE DYNAMIC FILLED FUNCTION ALGORITHM FOR ACYCLIC GRAPH PARTITIONING

Jianli Chen*, Jun Yu, Fudan University, Shanghai, China; Jiarui Chen, Fuzhou University, Fuzhou, China; Xiao Shi, Southeast University, Los Angeles, CA; Lichong Sun, Huawei Technologies Company Ltd., Hangzhou, China*

PARALLELIZING NET ROUTING WITH CGANS

Dmitry Utyamishev*, Inna P.-Vaisband, University of Illinois at Chicago, Chicago, IL*

PHYSICAL ADVERSARIAL ATTACKS OF DIFFRACTIVE DEEP NEURAL NETWORKS

Yingjie Li*, Cunxi Yu, University of Utah, Salt Lake City, UT*

WEDNESDAY WORK-IN-PROGRESS POSTERS

Time: 6:00 pm – 7:00 pm
Room: Level 2 Foyer
Event Type: Networking Reception, Work-in-Progress Poster

ARGOS: AN ADAPTIVE AND REGION-SCALE KNOWLEDGE DISTILLATION FOR OBJECT RECOGNITION SYSTEMS

***Mohammad Bajestani**, Rahul Santhosh Kumar Varma, Carole-Jean Wu, Yezhou Yang, Arizona State University, Tempe, AZ*

A COORDINATED GPU OVERDRIVE FAULT ATTACK ON NEURAL NETWORKS

Majid Sabbagh, Yunsi Fei, David Kaeli, Northeastern University, Boston, MA

DETERMINING THE MULTIPLICATIVE COMPLEXITY OF BOOLEAN FUNCTIONS USING SAT

***Mathias Soeken**, Microsoft, Zurich, Switzerland*

AN EFFICIENT CELL CAPACITOR COMPACT MODELING AND APPLICATION FOR HIGH-SPEED DRAM DESIGN

***Jae Nyeong Kim**, Beomsang Yoo, Sanghoon Lee, Dongsoo Kang, Juwon Lim, Dooyoung Kim, Jangwoo Ryu, Yoochang Sung, Jeongyeol Kim, Samsung Electronics, Hwasung-si, South Korea*

EFFICIENT REAL-TIME OBJECT DETECTION WITH ADAPTIVE IMAGE SCALING AND CROPPING

***Siwoo Chung**, Woosung Kang, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea; Hoon Sung Chwa, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea; Youngmoon Lee, Hanyang University, Ansan, South Korea; Kilho Lee, Soongsil University, Seoul, South Korea; Kang G. Shin, University of Michigan, Ann Arbor, MI*

FASCINET: FULLY AUTOMATED SINGLE-BOARD COMPUTER GENERATOR USING A NEURAL NETWORK BASED DATASHEET SCRUBBER

***Morteza Fayazi**, Zachary Colter, Zineb Benameur-El Youbi, Tutu Ajayi, Ronald Dreslinski, University of Michigan, Ann Arbor, MI*

FINDING OPTIMAL IMPLEMENTATIONS OF NON-NATIVE CNOT GATES USING SAT

*Luca Müller, Philipp Niemann, DFKI GmbH, Breman, Germany; **Rolf Drechsler**, University of Bremen, Bremen, Germany*

GAMES, DOLLARS, SPLITS: A GAME-THEORETIC ANALYSIS OF SPLIT MANUFACTURING

***Vasudev Gohil**, Mark Tressler, Kevin Sipple, Satwik Patnaik, Jeyavijayan Rajendran, Texas A&M University, College Station, TX*

GLITCH AND LEVEL DETECTION ALGORITHMS FOR ANALOG MIXED-SIGNAL VERIFICATION COVERAGE MANAGEMENT

***Sayandeep Sanyal**, Aritra Hazra, Pallab Dasgupta, Indian Institute of Technology Kharagpur, Kharagpur, India; Scott Morrison, Texas Instruments, Dallas, TX; Sudhakar Surendran, Lakshmanan Balasubramanian, Texas Instruments (India) Pvt. Ltd., Banga*

IO PERFORMANCE MODELING FOR COMMUNICATION WORKLOADS

Asad Khan, Ahmed Abousamra, Mohammad Majharul Islam, Kenneth O'Neal, Marc Millier, Raid Ayoub, Intel Corporation, Hillsboro, OR

ON THE IMPACT OF ELECTRICAL MASKING AND TIMING ANALYSIS ON SOFT ERROR RATE ESTIMATION IN DEEP SUBMICRON TECHNOLOGIES

***Georgios-Ioannis Paliaroutis**, Pelopidas Tsoumanis, Nestor Evmorfopoulos, Georgios Stamoulis, University of Thessaly, Volos, Greece*

PARAMETER APPROXIMATION IN CNNS FOR IMPROVED INFERENCE ON FPGA

***Vahideh Akhlaghi**, Hamed Omidvar, Massimo Franceschetti, Rajesh K. Gupta, University of California, San Diego, La Jolla, CA*

A ROBUST DNN ACCELERATOR WITH DATA-PATH FAULT DETECTION AND MITIGATION

***Stéphane Burel**, Adrian Evans, Lorena Anghel, CEA LIST, Grenoble, France*

ROHNAS-WHEN ROBUSTNESS MEETS HW-AWARE NAS: A NEURAL ARCHITECTURE SEARCH FRAMEWORK WITH CONJOINT OPTIMIZATION FOR ADVERSARIAL ROBUSTNESS AND HARDWARE EFFICIENCY OF CONVOLUTIONAL AND CAPSULE NETWORKS

*Alberto Marchisio, Vienna University of Technology, Vienna, Austria; **Vojtech Mrazek**, Brno University of Technology, Brno, Czech Republic; Andrea Massa, Beatrice Bussolino, Maurizio Martina, Politecnico di Torino, Turin, Italy; Muhammad Shafique, New York University, Abu Dhabi, UAE*

RTL REGRESSION TEST SELECTION USING MACHINE LEARNING

*Ganapathy Parthasarathy, **Saurav Nanda**, Sridhar Rajakumar, Synopsys, Mountain View, CA; Aabid Rushdi, Parivesh Choudhary, Malan Evans, Hansika Gunasekara, Synopsys, Colombo, Sri Lanka*

SONICFFT: A SYSTEM ARCHITECTURE FOR ULTRASONIC-BASED FFT ACCELERATION

***Mohamed M. Sabry Aly**, Darayus Adil Patel, Nanyang Technological University, Singapore, Singapore; Viet Phuong Bui, A*STAR Institute of High Performance Computing, Singapore, Singapore*

SPECMCTS: ACCELERATING MONTE CARLO TREE SEARCH USING SPECULATIVE TREE TRAVERSAL

*Hyungmin Cho, **Juhwan Kim**, Byeongmin Kang, Sungkyunkwan University, Suwon, South Korea*

STIMULUS TRUNCATION METHOD FOR ENERGY EFFICIENT MEMRISTOR BASED NEUROMORPHIC COMPUTING

*Zhiheng Liao, Jingyan Fu, North Dakota State University, Fargo, ND; **Caiwen Ding**, University of Connecticut, Storrs, CT; Jinhui Wang, University of South Alabama, Mobile, AL*

TATAMI: DYNAMIC CGRA RECONFIGURATION FOR MULTI-CORE GENERAL PURPOSE PROCESSING

***Jinho Lee**, Trevor E. Carlson, National University of Singapore, Singapore, Singapore*

KEYNOTE – KURT KEUTZER: AI, MACHINE LEARNING, DEEP LEARNING: WHERE ARE THE REAL OPPORTUNITIES FOR THE EDA INDUSTRY?

Time: 8:45 am – 9:45 am
Room: TBD
Event Type: Visionary Talk

Kurt Keutzer is a Professor of the Graduate School in EECS at University of California, Berkeley, where he is also a member of the Berkeley AI Research (BAIR) Lab and co-director of the Berkeley Deep Drive research consortium. His research covers all aspects of making Deep Learning efficient. His "Squeeze" family of Deep Neural Nets were among the first neural nets suitable for mobile and IOT applications. His collaboration on the LARS and LAMB algorithms reduced the training time of ImageNet and BERT to minutes. Previously, Kurt was CTO at Synopsys, and his contributions to Electronic Design Automation were recognized at the 50th Design Automation Conference where he was noted as a Top 10 most-cited author, author of a Top 10 cited paper, and one of only three people to win four Best Paper Awards in the fifty-year history of that conference. As an entrepreneur Kurt has been an investor and advisor to over 30 startups. His most recent exits have been DeepScale (where he was co-founder), acquired by Tesla, and BabbleLabs (investor and advisor), acquired by Cisco. He was the first investor in Coverity, and he was among the first group of investors in Tensilica, and, more recently, Covariant.

ACCELERATING EDA ALGORITHMS WITH GPUS AND MACHINE LEARNING

Time: 10:30 am – 12:00 pm
Room: 3020
Event Type: Special Session
Topic Area(s): EDA, Machine Learning/AI

Chair/Co-Chair: David Z. Pan (The University of Texas at Austin)

Session Organizer: Brucek Khailany, NVIDIA, Austin, TX; David Pan, The University of Texas at Austin, Austin, TX

Recent advancements in GPU accelerated computing platforms and machine learning (ML) based optimization techniques have led to exciting recent research progress with large speedups on many EDA algorithms fundamental to semiconductor design flows. In this session, we highlight ongoing research deploying GPUs and ML to mask synthesis, IC design automation, and PCB design at commercial EDA vendors and semiconductor design and manufacturing companies. Research into mask synthesis techniques shows the potential for GPUs to accelerate inverse lithography and for running training and inference of ML models for process modeling. In PCB layout editing, GPU-accelerated path rendering techniques can scale to millions of rendered objects with interactive responsiveness. In IC physical design, GPU-accelerated reinforcement learning for DRC fixing combined with traditional EDA optimization techniques can automate standard cell layout generation. The combination of GPUs and ML can enable large speedups and automate key EDA tasks previously seen as intractable.

MASK SYNTHESIS IN THE ERA OF GPU COMPUTING AND DEEP LEARNING

***Danping Peng**, TSMC, San Francisco, CA*

ACCELERATING PCB LAYOUT EDITOR USING MODERN GPU ARCHITECTURE FOR COMPLEX DESIGNS

***Patrick Bernard**, Anton Kryukov, Cadence Design Systems, inc.*

AIVENGERS: EMERGING AI ALGORITHMS TO THE RESCUE

Time: 11:00 am – 11:30 am (Combined Session)
Room: 3014
Event Type: Research Session
Topic Area(s): Design, AI/ML System Design

Chair/Co-Chair: To be announced

Deep learning technology is evolving quickly. Recent years have seen the emergence of new deep learning methods, including transformers, graph and temporal convolutions, and federated learning for AI at scale. This session presents hardware methods and optimization for these emerging deep learning algorithms.

PRUNING IN TIME (PIT): A LIGHT-WEIGHT NETWORK ARCHITECTURE OPTIMIZER FOR TEMPORAL CONVOLUTIONAL NETWORKS

*Matteo Risso, Daniele Jahier Pagliari, Enrico Macii, Massimo Poncino, Politecnico of Turin, Torino, Italy; **Alessio Burrello**, Francesco Conti, Lorenzo Lamberti, Luca Benini, University of Bologna, Bologna, Italy*

NEW TRENDS IN MEMORY ARCHITECTURE DESIGNS FOR I/O SYSTEMS

Time: 2:40 am – 3:00 pm (Combined Session)
Room: 3014
Event Type: Research Session
Topic Area(s): Embedded Systems, Embedded Memory, Storage and Networking

Chair/Co-Chair: Chenchen Liu (University of Maryland, Baltimore County), Co-Chair to be announced

This session describes new architectures and designs for embedded memory and storage devices. The first two papers address the dynamic adjustment of the new RAM-based designs for a reduced refresh rate against an excessive timing margin for the worst-case temperature, as well as looking at cross-layer optimizations. The last two papers look at new possible architectural designs of solid-state drives and memories with alternative technologies.

KV-SSD: WHAT IS IT GOOD FOR?

***Manoj P. Saha**, Adnan Maruf,Janki Bhimani, Florida International University, Miami, FL; Bryan S. Kim, Syracuse University, Miami, FL*

CRITICAL DESIGN FOR TIMING CRITICAL SYSTEMS

Time: 10:30 am – 11:00 am (Combined Session)
Room: 3016
Event Type: Research Session
Topic Area(s): Embedded Systems, Time-Critical System Design

Chair/Co-Chair: To be announced

Increasing storage and I/O requirements as well as emerging parallelism in real-time embedded systems poses challenges pertaining to timing properties and performance at the same time. The papers presented in this session address concerns of real-time storage on flash, I/O virtualization with guaranteed real-time performance, distributed training of DNNs, data transfer optimization, and timing analysis for parallel real-time tasks.

DYNAMIC CHIP CLUSTERING AND TASK ALLOCATION FOR REAL-TIME FLASH

***Gyeongtaek Kim**, Sungjin Lee, Hoon Sung Chwa, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea*

SPACE: SECURITY OF POST-QUANTUM AND ACCELERATOR-BASED CRYPTOGRAPHIC ENGINES

Time: 11:00 am – 12:00 pm (Combined Session)
Room: 3016
Event Type: Research Session
Topic Area(s): Hardware Security: Primitives, Architecture, Design & Test, Security

Chair/Co-Chair: Ujjwal Guin (Auburn University), Co-Chair to be announced

The security of post-quantum and accelerator rich cryptographic platforms requires novel techniques and methodologies that extend across the computing stack. From novel neural network models to highly optimized architectures for post-quantum crypto, this session covers an array of methods that can be applied to enhance the security of critical next generation systems. In addition, architectural techniques that validate the integrity of data and enhance the properties of branch predictors are discussed that provide additional security assurances in accelerator rich systems.

EFFICIENT IMPLEMENTATION OF FINITE FIELD ARITHMETIC FOR BINARY RING-LWE POST-QUANTUM CRYPTOGRAPHY THROUGH A NOVEL LOOKUP-TABLE-LIKE METHOD

***Jiafeng Xie**, Pengzhou He, Villanova University, Villanova, PA; Wujie Wen, Lehigh University, Bethlehem, PA*

CUCKOONSAI: AN EFFICIENT MEMORY AUTHENTICATION USING AMALGAM OF CUCKOO FILTERS AND INTEGRITY TREES

***Omais Shafi**, Ismi Abidi Indian Institute of Technology Dehli, New Delhi, India*

TINYML – TINY IN SIZE, BIG IN IMPACT!

Time: 1:30 pm – 3:00 pm
Room: 3002
Event Type: Special Session
Topic Area(s): Embedded Systems, Machine Learning/AI

Chair/Co-Chair: Theocharis Theocharides (University of Cyprus)

Session Organizer: Theocharis Theocharides, University of Cyprus, Nicosia, Cyprus

tinyML encapsulates and nurtures the fast-growing branch of ultra-low power machine learning technologies and approaches dealing with machine intelligence at the very edge of the cloud. These integrated "tiny" machine learning applications require "full-stack" solutions including machine learning architectures, techniques, tools, and approaches capable of performing on-device analytics. A variety of sensing modalities are used with extreme energy efficiency, to enable machine intelligence right at the boundary of the physical and digital worlds. We see a new world with trillions of distributed intelligent devices enabled by energy efficient machine learning technologies that sense, analyze, and autonomously act together to create a healthier and more sustainable environment for all! This special session provides a birds eye view of the current state of the art through an overview talk and two industrial perspectives from leaders of this exciting paradigm, identifying the challenges and opportunities surrounding this rapidly growing area.

THE CURRENT STATE OF TINYML - OPPORTUNITIES, CHALLENGES AND THE ROAD AHEAD

Boris Murmann, Stanford University, Stanford, CA; Theocharis Theocharides, University of Cyprus, Nicosia, Cyprus ***Muhammad Shafique****, New York University Abu Dhabi, Abu Dhabi, United Arab Emirates Vijay Janapa Reddi, Harvard University, Cambridge, MA*

TINYML ON EMBEDDED MICROPROCESSORS AND THE BROAD AVENUE OF OPPORTUNITIES

Ian Bratt*, Arm Ltd., Austin, TX*

ALWAYS-ON MODULES DEMONSTRATE THAT TINYML IS ALREADY HERE!

Evgeni Gousev*, Qualcomm, San Francisco, CA*

AUTOMATING AUTONOMY: FROM GPU TO TRAFFIC CONTROL

Time: 1:30 pm – 3:00 pm
Room: 3016
Event Type: Research Session
Topic Area(s): Autonomous Systems

Chair/Co-Chair: Wanli Chang (University of York, Hunan University)

This session features a range of exciting results for the design and analysis of autonomous systems. At the application level, several papers address key challenges of real-time performance, fault tolerance, and distributed control of autonomous vehicles. On the software side, two papers present novel state-sensitive fuzzing techniques and a robot runtime that can exploit environment heterogeneity to significantly improve performance and resource usage. Finally, at the hardware level, one paper tackles the outstanding problem of memory protection in GPUs.

GGUARD: ENABLING LEAKAGE-RESILIENT MEMORY ISOLATION IN GPU-ACCELERATED AUTONOMOUS EMBEDDED SYSTEMS

Yaswanth Yadlapalli*, Husheng Zhou,Cong Liu, The University of Texas at Dallas, Richardson, TX; Yuqun Zhang, Southern University of Science and Technology, Shenzhen, China*

ROBORUN: A ROBOT RUNTIME TO EXPLOIT SPATIAL HETEROGENEITY

Behzad Boroujerdian*, The University of Texas at Austin, New York City, NY; Radhika Ghosal, Jon Cruz, Brian Plancher, Vijay Janapa Reddi, Harvard University, Cambridge, MA*

NEURAL PRUNING SEARCH FOR REAL-TIME OBJECT DETECTION OF AUTONOMOUS VEHICLES

Pu Zhao*, Geng Yuan, Yuxuan Cai, Yanzhi Wang, Xue Lin, Northeastern University, Boston, MA; Wei Niu,Bin Ren, College of William and Mary, Williamsburg, VA; Qi Liu, Wujie Wen, Lehigh University, Bethlehem, PA*

ANALYZING AND IMPROVING FAULT TOLERANCE OF LEARNING-BASED NAVIGATION SYSTEMS

Zishen Wan*, Georgia Institute of Technology, Atlanta, GA; Malik Aqeel Anwar, Arijit Raychowdhury, Georgia Institute of Technology, Atlanta, GA; Yu-Shun Hsiao, Tianyu Jia, Vijay Janapa Reddi, Harvard University, Cambridge, MA*

A MELANGE OF MACHINE LEARNING FRAMEWORKS FOR OPTIMIZATION

Time: 1:30 pm – 2:15 pm (Combined Session)
Room: 3014
Event Type: Research Session
Topic Area(s): Design, AI/ML System Design

Chair/Co-Chair: Narayan Srinivasa (Intel Corporation), Co-Chair to be announced

The landscape of machine learning systems is evolving very fast, and many optimizations are needed across algorithm, compiler, and hardware accelerator designs. In this session, we highlight frameworks for machine learning system optimization covering four topics: memory-efficient graph neural network design, neural hardware-compiler co-design, energy-efficient unsupervised spiking neural network framework, and Bayesian neural network hardware accelerator.

EVOLVED NEURAL-HARDWARE-COMPILER CO-DESIGN

***Yujun Lin**, Song Han, Massachusetts Institute of Technology, Cambridge, MA; Mengtian Yang, Shanghai Jiao Tong University, Shanghai, China*

HIGH-PERFORMANCE FPGA-BASED ACCELERATOR FOR BAYESIAN NEURAL NETWORKS

*Hongxiang Fan, Wayne Luk, Imperial College London, London, United Kingdom; **Martin Ferianc**, Miguel Rodrigues, University College London, London, United Kingdom; Hongyu Zhou, Central South University, Changsha, China; Xinyu Niu, Corerain, Shenzhen, China*

LET THERE BE LIGHT: EMERGING TECHNOLOGY FOR INTELLIGENT SYSTEMS

Time: 1:30 pm - 2:40 pm (Combined Session)
Room: 3014
Event Type: Research Session
Topic Area(s): Design, AI/ML System Design

Chair/Co-Chair: To be announced

Modern artificial intelligence (AI) methods have high computing and memory costs. This session focuses on the use of emerging technologies, from silicon photonics to in-memory computing, to mitigate these costs and move us towards more efficient hardware implementations for AI.

TOWARDS RESILIENT DEPLOYMENT OF IN-MEMORY NEURAL NETWORKS WITH HIGH THROUGHPUT

***Baogang Zhang**, Rickard Ewetz, University of Central Florida, Orlando, FL*

CROSSLIGHT: A CROSS-LAYER OPTIMIZED SILICON PHOTONIC NEURAL NETWORK ACCELERATOR

***Febin Sunny**, Asif Mirza, Mahdi Nikdast, Sudeep Pasricha, Colorado State University, Fort Collins, CO*
add presentation

LOW-COST AND EFFECTIVE FAULT-TOLERANCE ENHANCEMENT TECHNIQUES FOR EMERGING MEMORIES-BASED DEEP NEURAL NETWORKS

***Thai Hoang Nguyen**, Jaehyuk Choi, Sungkyunkwan University, Suwon, South Korea; Imran Muhammad, National University of Sciences and Technology, Islamabad, Pakistan; Joon-Sung Yang, Yonsei University, Seoul, South Korea*

RECONFIGURABILITY ACROSS THE SPECTRUM: FROM ICS TO INTELLIGENCE

Time: 3:30 pm – 5:00 pm
Room: 3016
Event Type: Research Session
Topic Area(s): Design, SoC, Heterogeneous, and Reconfigurable Architectures

Chair/Co-Chair: Daniel Morris (Facebook)

Reconfigurability has become essential, for efficient processing at all layers of the compute stack. This session presents novel architectures for integrating thousands of cores on a single wafer, as well as interconnect technologies for 3D integration. Moreover, architectures for emerging AI paradigms such as hyper-dimensional computing and graph neural networks are presented. Finally, ultra-fast reconfiguration techniques for CGRAs and for virtualizing FPGAs are discussed.

DESIGNING A 2048-CHIPLET, 14336-CORE WAFERSCALE PROCESSOR

***Saptadeep Pal**, Irina Alam, Haris Suhail, Shi Bu, Subramanian S. Iyer, Puneet Gupta, University of California, Los Angeles, Los Angeles, CA; Jingyang Liu, Nicholas Cebry, Rakesh Kumar, University of Illinois at Urbana Champaign, Urbana-Champaign, IL*

MICRO-BUMPING, HYBRID BONDING, OR MONOLITHIC? A PPA STUDY FOR HETEROGENEOUS 3D IC OPTIONS

***Jinwoo Kim**, Lingjun Zhu, Hakki Mert Torun,Madhavan Swaminathan, Sung Kyu Lim, Georgia Institute of Technology, Atlanta, GA*

ULTRA-FAST CGRA SCHEDULING TO ENABLE RUN TIME, PROGRAMMABLE CGRAS

***Jinho Lee**, Trevor E. Carlson, National University of Singapore, Singapore, Singapore*

REINFORCED: ANALOG CIRCUIT SIZING AND LAYOUT

Time: 5:00 pm – 5:30 pm
Room: 3014
Event Type: Research Session
Topic Area(s): EDA, Analog Design, Simulation, Verification and Test

Chair/Co-Chair: Meghna Mankalale (Synopsys), Co-Chair to be announced

This session starts with four inspiring papers to boost the analog and mixed-signal circuit sizing and optimization process with various flavors of reinforcement learning and Bayesian optimization, as for instance using deep neural network, localized and trust-based modeling and exploration, and exploiting design knowledge. The last two papers present exciting ideas on unsupervised symmetry constraint extraction and interactive analog layout editing with legalization.

DNN-OPT: AN RL INSPIRED OPTIMIZATION FOR ANALOG CIRCUIT SIZING USING DEEP NEURAL NETWORKS*

***Ahmet F. Budak**, David Pan, Nan Sun, The University of Texas at Austin, Austin, TX; Prateek Bhansali, Chandramouli V. Kashyap, Intel Corporation, Hillsboro, OR; Bo Liu, University of Glasgow, Glasgow, United Kingdom*

PRIORITIZED REINFORCEMENT LEARNING FOR ANALOG CIRCUIT OPTIMIZATION WITH DESIGN KNOWLEDGE

***Karthik Somayaji Suryanarayana**, Hanbin Hu, Peng Li, University of California, Santa Barbara, Santa Barbara, CA*

UNIVERSAL SYMMETRY CONSTRAINT EXTRACTION FOR ANALOG AND MIXED-SIGNAL CIRCUITS WITH GRAPH NEURAL NETWORKS

***Hao Chen**, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, David Z. Pan, The University of Texas at Austin, Austin, TX*

INTERACTIVE ANALOG LAYOUT EDITING WITH INSTANT PLACEMENT LEGALIZATION

*Xiaohan Gao, Yibo Lin, Peking University, Beijing, China; **Mingjie Liu**, David Z. Pan,The University of Texas at Austin, Austin, TX*

2021: A SPACE ODYSSEY IN PLACE AND ROUTE

Topic Area(s): EDA, Physical Design and Verification, Lithography and DFM

New applications and design rules constantly challenge placement and routing, more so at sub-5nm nodes seen in 2021. Learn about novel place and route algorithms and methodologies across ASIC and FPGAs here. These carefully selected works will take you on a journey managing time and space in place and route!

VLSI STRUCTURE-AWARE PLACEMENT FOR CONVOLUTIONAL NEURAL NETWORK ACCELERATOR UNITS

Yun Chou, Jhih-Wei Hsu, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan; Tung-Chieh Chen, Maxeda Technology, Hsinchu, Taiwan

ULTRAFAST CPU/GPU KERNELS FOR DENSITY ACCUMULATION IN PLACEMENT

Zizheng Guo, Jing Mai, Yibo Lin, Peking University, Beijing, China

PERFORMANCE-DRIVEN SIMULTANEOUS PARTITIONING AND ROUTING FOR MULTI-FPGA SYSTEMS

Jun-Jie Wang, Ming-Hung Chen, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

ANONYMOUS: CONSTRUCTING RECTILINEAR MINIMUM STEINER TREE VIA REINFORCEMENT LEARNING

Jinwei Liu, Gengjie Chen, Evangeline F.Y. Young, The Chinese University of Hong Kong, Hong Kong, Hong Kong

A COMPLETE PCB ROUTING METHODOLOGY WITH CONCURRENT HIERARCHICAL ROUTING

Shih-Ting Lin, Hung-Hsiao Wang, Chia-Yu Kuo, Yih-Lang Li, National Chiao Tung University, Hsinchu, Taiwan; Yolo Chen, Wistron NeWeb Corporation, Hsinchu, Taiwan

SIMULTANEOUS PRE- AND FREE-ASSIGNMENT ROUTING FOR MULTIPLE REDISTRIBUTION LAYERS WITH IRREGULAR VIAS

Yu-Jie Cai, Yang Hsu, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

A-EYE ON THE CUTTING EDGE OF IOT

Topic Area(s): Embedded Systems, Embedded System Design Methodologies

This session covers cutting edge research to integrate artificial intelligence (AI) across edge, smart building, and medical IoT devices. The first two papers focus on latency and sparsity optimizations in edge computing devices. The third paper focuses on prioritizing user comfort and energy efficiency in smart building environments. The last paper presents a timely approach to detect ventricular arrhythmias with low power medical devices, to help deliver in-time defibrillation.

ZEROBN: LEARNING COMPACT NEURAL NETWORKS FOR LATENCY-CRITICAL EDGE SYSTEMS

Shuo Huai, Weichen Liu, Nanyang Technological University, Singapore, Singapore; Lei Zhang, Di Liu, HP-NTU Digital Manufacturing Corporate Lab, Singapore, Singapore; Ravi Subramaniam, Hewlett Packard Enterprise, Palo Alto, CA

EIMPROVE – OPTIMIZING ENERGY AND COMFORT IN BUILDINGS BASED ON FORMAL SEMANTICS AND REINFORCEMENT LEARNING

Sagar Verma, Supriya Agrawal, Venkatesh R, Ulka Shrotri Aabriti Dutta, Tata Consultancy Services Ltd., Pune, India; Srinarayana Nagarathinam, Rajesh Jayaprakash, Tata Consultancy Services Ltd., Chennai, India

ENABLING ON-DEVICE MODEL PERSONALIZATION FOR VENTRICULAR ARRHYTHMIAS DETECTION BY GENERATIVE ADVERSARIAL NETWORKS

Zhenge Jia, Jingtong Hu, University of Pittsburgh, Pittsburgh, PA; Feng Hong, Lichuan Ping, Singular Medical Co., Ltd., Suzhou, China; Yiyu Shi, University of Notre Dame, South Bend, IN

AIVENGERS: EMERGING AI ALGORITHMS TO THE RESCUE

Topic Area(s): Design, AI/ML System Design

Deep learning technology is evolving quickly. Recent years have seen the emergence of new deep learning methods, including transformers, graph and temporal convolutions, and federated learning for AI at scale. This session presents hardware methods and optimization for these emerging deep learning algorithms.

DANCING ALONG BATTERY: ENABLING TRANSFORMER WITH RUN-TIME RECONFIGURABILITY ON MOBILE DEVICES

Yuhong Song, Panjie Qi, Qingfeng Zhuge, Edwin Hsing-Mean Sha, East China Normal University, Shanghai, China; Weiwen Jiang, Yiyu Shi, University of Notre Dame, South Bend, IN; Bingbing Li, Caiwen Ding, University of Connecticut, Mansfield, CT; Sakyasingha Dasgupta, Edgecortix Inc, Tokyo, Japan

BLOCKGNN: TOWARDS EFFICIENT GNN ACCELERATION USING BLOCK-CIRCULANT WEIGHT MATRICES

Zhe Zhou, Bizhao Shi, Guangyu Sun, Guojie Luo, Zhe Zhang, Yijin Guan, Peking University, Beijing, China

HELIOS: HETEROGENEITY-AWARE FEDERATED LEARNING WITH DYNAMICALLY BALANCED COLLABORATION

Zirui Xu, Fuxun Yu, Xiang Chen, George Mason University, Fairfax, VA; Jinjun Xiong, IBM Thomas J. Watson Research Center, Yorktown Heights, NY

AN APPROXIMATE WORLD FROM NEURONS TO GENOMES

Topic Area(s): Design, Approximate Computing for AI/ML

The session features recent advancements in applying approximate computing techniques to different computing paradigms pertaining to Artificial Intelligence and Machine Learning, including hyperdimensional systems, spiking neural networks, probabilistic programming, and compressed video analytics. The techniques proposed include new encoding schemes, fixed-point quantization approaches, training methodologies, and compiler frameworks. The techniques have demonstrated significant improvement in both energy consumption and performance across various end-applications.

COGNITIVE CORRELATIVE ENCODING FOR GENOME SEQUENCE MATCHING IN HYPERDIMENSIONAL SYSTEM

Prathyush Poduval, Indian Institute of Science, Bengaluru, India; Zhuowen Zou, Elaheh Sadredini, Mohsen Imani, University of California, Irvine, Irvine, CA; Xunzhao Yin, Zhejiang University, Hangzhou, China

PIXELSIEVE: TOWARDS EFFICIENT ACTIVITY ANALYSIS FROM COMPRESSED VIDEO STREAMS

Yongchen Wang,Ying Wang, Huawei Li, Xiaowei Li, Chinese Academy of Sciences, Beijing, China

AUTOMATING AUTONOMY: FROM GPU TO TRAFFIC CONTROL

Topic Area(s): Autonomous Systems

This session features a range of exciting results for the design and analysis of autonomous systems. At the application level, several papers address key challenges of real-time performance, fault tolerance, and distributed control of autonomous vehicles. On the software side, two papers present novel state-sensitive fuzzing techniques and a robot runtime that can exploit environment heterogeneity to significantly improve performance and resource usage. Finally, at the hardware level, one paper tackles the outstanding problem of memory protection in GPUs.

GGUARD: ENABLING LEAKAGE-RESILIENT MEMORY ISOLATION IN GPU-ACCELERATED AUTONOMOUS EMBEDDED SYSTEMS

Yaswanth Yadlapalli, Husheng Zhou,Cong Liu, The University of Texas at Dallas, Richardson, TX; Yuqun Zhang, Southern University of Science and Technology, Shenzhen, China

ROBORUN: A ROBOT RUNTIME TO EXPLOIT SPATIAL HETEROGENEITY

Behzad Boroujerdian, The University of Texas at Austin, New York City, NY; Radhika Ghosal, Jon Cruz, Brian Plancher, Vijay Janapa Reddi, Harvard University, Cambridge, MA

NEURAL PRUNING SEARCH FOR REAL-TIME OBJECT DETECTION OF AUTONOMOUS VEHICLES

Pu Zhao, Geng Yuan, Yuxuan Cai, Yanzhi Wang, Xue Lin, Northeastern University, Boston, MA; Wei Niu,Bin Ren, College of William and Mary, Williamsburg, VA; Qi Liu, Wujie Wen, Lehigh University, Bethlehem, PA

ANALYZING AND IMPROVING FAULT TOLERANCE OF LEARNING-BASED NAVIGATION SYSTEMS

Zishen Wan, Georgia Institute of Technology, Atlanta, GA; Malik Aqeel Anwar, Arijit Raychowdhury, Georgia Institute of Technology, Atlanta, GA; Yu-Shun Hsiao, Tianyu Jia, Vijay Janapa Reddi, Harvard University, Cambridge, MA

BEYOND SUPERVISED LEARNING: APPROACHES FOR EFFICIENT AND RELIABLE INTELLIGENCE

Topic Area(s): Design, AI/ML System Design

As AI is entering into all aspects of our lives, issues such as scalability, privacy, and reliability become predominant in addition to performance. There exists an increasing interest in non-traditional methods to address the efficiency/complexity dilemma encountered in supervised learning. This session presents four diverse approaches along with federated learning, Hyper-dimensional computing, reinforcement learning, and verifiable deep learning.

HADFL: HETEROGENEITY-AWARE DECENTRALIZED FEDERATED LEARNING FRAMEWORK

Jing Cao, Zirui Lian, Weihong Liu, Zongwei Zhu, Cheng Ji, Nanjing University of Science and Technology, Nanjing, China

REGHD: ROBUST AND EFFICIENT REGRESSION IN HYPER-DIMENSIONAL LEARNING SYSTEM

Alejandro Hérnandez-Cano, Universidad Nacional Autónoma de México, Mexico City, Mexico; Zhuowen Zou, Mohsen Imani, University of California, Irvine, Irvine, CA; Cheng Zhuo, Xunzhao Yin, Zhejiang University, Hangzhou, China

AID: ATTESTING THE INTEGRITY OF DEEP NEURAL NETWORKS

Omid Aramoon, Gang Qu, University of Maryland, College Park, MD; Pin-Yu Chen, IBM research, Yorktown Heights, NY

BIG DATA INTO SMALL DEVICES

Topic Area(s): Embedded Systems, Embedded Software

Big data is moving to edge devices. Papers in this session show how to make tensor graphs and contrastive learning feasible on small devices. Also, an efficient representation and processing of random forests is shown. Together with an efficient sparse matrix vector multiplication.

ON THE EFFICIENCY OF SPARSE-TILED TENSOR GRAPH PROCESSING FOR LOW MEMORY USAGE

Antonio Cipolletta, Andrea Calimera, Politecnico di Torino, Torino, Italy

ECO-FELLER: MINIMIZING THE ENERGY CONSUMPTION OF RANDOM FOREST ALGORITHM BY AN ECO-PRUNING STRATEGY OVER MLC NVRAM

Yu-Pei Liang, Tsan-sheng Hsu, Academia Sinica, Taipei, Taiwan; Yung-Han Hsu, Wei-Kuan Shih, National Tsing Hua University, Hsinchu, Taiwan; Tseng-Yi Chen, Shuo-Han Chen, National Taipei University of Technology, Taipei, Taiwan; Hsin-Wen Wei, Tamkang University, Taipei, Taiwan

ENABLING ON-DEVICE SELF-SUPERVISED CONTRASTIVE LEARNING WITH SELECTIVE DATA CONTRAST

Yawen Wu, Zhepeng Wang, Jingtong Hu, University of Pittsburgh, Pittsburgh, PA; Dewen Zeng, Yiyu Shi, University of Notre Dame, South Bend, IN

SPV8: PURSUING OPTIMAL VECTORIZATION AND REGULAR COMPUTATION PATTERN IN SPMV

Chenyang Li, Tian Xia, Wenzhe Zhao, Nanning Zheng, Pengju Ren, Xi'an Jiaotong University, Xi'an, China

CRITICAL DESIGN FOR TIMING CRITICAL SYSTEMS

Topic Area(s): Embedded Systems, Time-Critical System Design

Increasing storage and I/O requirements as well as emerging parallelism in real-time embedded systems poses challenges pertaining to timing properties and performance at the same time. The papers presented in this session address concerns of real-time storage on flash, I/O virtualization with guaranteed real-time performance, distributed training of DNNs, data transfer optimization, and timing analysis for parallel real-time tasks.

I/O-GUARD: HARDWARE/SOFTWARE CO-DESIGN FOR I/O VIRTUALIZATION WITH GUARANTEED REAL-TIME PERFORMANCE

Zhe Jiang, Yunfeng Ma, Neil Audsley, University of York, York, United Kingdom; Kecheng Yang, Texas State University, San Marcos, TX; Nathan Fisher, Zheng Dong, Wayne State University, Detroit, MI

TRAINING ACCELERATION FOR DEEP NEURAL NETWORKS: A HYBRID PARALLELIZATION STRATEGY

Zihao Zeng, Chubo Liu, Zhuo Tang, Kenli Li, Hunan University, Changsha, China; Wanli Chang, University of York, York, United Kingdom

OPTIMAL MEMORY ALLOCATION AND SCHEDULING FOR DMA DATA TRANSFERS UNDER THE LET PARADIGM

Paolo Pazzaglia, University of Saarland, Saarbrücken, Germany; Daniel Casini, Alessandro Biondi, Marco Di Natale, Scuola Superiore Sant'Anna, Pisa, Italy

A FINER-GRAINED BLOCKING ANALYSIS FOR PARALLEL REAL-TIME TASKS WITH SPIN-LOCKS

Zewei Chen, Maolin Yang, Hang Lei, Yong Liao, University of Electronic Science and Technology of China, Chengdu, China; Lei Qiao, Beijing Institute of Control Engineering, Beijing, China

DEEP LEARN YOUR YIELD

Topic Area(s): EDA, Physical Design and Verification, Lithography and DFM

Wondering how to improve your manufacturability and yield at sub-5nm? These four papers bring the best of deep learning technologies and creative approaches to transfer learn layout pattern generations, attack data imbalance, insert SRAFs and accelerate dummy fill computation.

ATTENTIONAL TRANSFER IS ALL YOU NEED: TECHNOLOGY-AWARE LAYOUT PATTERN GENERATION

Xiaopeng Zhang, Haoyu Yang, Evangeline F.Y. Young, The Chinese University of Hong Kong, Hong Kong, Hong Kong

SUBRESOLUTION ASSIST FEATURE INSERTION BY VARIATIONAL ADVERSARIAL ACTIVE LEARNING AND CLUSTERING WITH DATA POINT RETRIEVAL

Sean Shang-En Tseng, Iris Hui-Ru Jiang, National Taiwan University, Taipei, Taiwan; James P. Shiely, Synopsys, Hillsboro, OR

NEURFILL: MIGRATING FULL-CHIP CMP SIMULATORS TO NEURAL NETWORKS FOR MODEL-BASED DUMMY FILLING SYNTHESIS

Junzhe Cai, Changhao Yan, Xuan Zeng, Fudan University, Shanghai, China; Yuzhe Ma, Bei Yu, The Chinese University of Hong Kong, Hong Kong, Hong Kong; Dian Zhou, The University of Texas at Dallas, Dallas, TX

DESIGNERS RELAX: GENERATING ANALOG WITH A CLICK

Topic Area(s): Design, Digital and Analog Circuits

Automating the analysis and design of analog circuits has remained a key challenge in EDA . This session features three papers, each representing continued advances in the area. The first presents a neural network approach to model functionality of analog and mixed-signal circuits. An EDA tool flow for phase-locked loop design automation is presented in the second paper. The final paper presents a Bayesian optimization approach to operational amplifier design.

CIRCUIT CONNECTIVITY INSPIRED NEURAL NETWORK FOR ANALOG MIXED-SIGNAL FUNCTIONAL MODELING

Mohsen Hassanpourghadi, Shiyu Su, Rezwan A. Rasul, Juzheng Liu, Qiaochu Zhang, Mike Shuo-Wei Chen, University of Southern California, Los Angeles, CA

AN AUTOMATED AND PROCESS-PORTABLE GENERATOR FOR PHASE-LOCKED LOOP

Zhongkai Wang, Minsoo Choi, John Wright, University of California, Zhaokai Liu, Nathan Narevsky, Colin Schmidt, Ayan Biwas, Borivoje Nikolic, Elad Alon, University of California, Berkeley, Berkeley, CA; Eric Chang, Blue Cheetah Analog Design, San Francisco, CA; Woorham Bae, Ayar Labs, Inc., Berkeley, CA

AUTOMATED COMPENSATION SCHEME DESIGN FOR OPERATIONAL AMPLIFIER VIA BAYESIAN OPTIMIZATION

Jialin Lu, Liangbo Lei, Fan Yang, Changhao Yan, Xuan Zeng, Fudan University, Shanghai, China

DIRTY TRICKS ON EMBEDDED SYSTEMS

Topic Area(s): Embedded Systems, Embedded Software

In embedded systems, efficiency is of paramount importance. In this session, several dimensions are explored: from the impact of data width on energy consumption to the distribution of the computation over connected devices based on user interaction. Also, it is shown how to unleashing the power of CPU-iGPU and to improve code safety by concolic testing.

TOWARDS RELIABLE SPATIAL MEMORY SAFETY FOR EMBEDDED SOFTWARE BY COMBINING CHECKED C WITH CONCOLIC TESTING

Sören Tempel, Vladimir Herdt, Rolf Drechsler, University of Bremen, Bremen, Germany

ARCHITECTURE-AWARE PRECISION TUNING WITH MULTIPLE NUMBER REPRESENTATION SYSTEMS*

Daniele Cattaneo,Michele Chiari, Nicola Fossati, Giovanni Agosta, Politecnico di Milano, Milan, Italy; Stefano Cherubin, Codeplay Software Ltd., Edinburgh, United Kingdom

PRUID: PRACTICAL USER INTERFACE DISTRIBUTION FOR MULTI-SURFACE COMPUTING

Menglong Cui, Mingsong Lv, Qingqiang He,Caiqi Zhang,Nan Guan, The Hong Kong Polytechnic University, Hong Kong, Hong Kong; Chuancai Gu, Tao Yang, Huawei Technologies Company Ltd., Hangzhou, China

A FRAMEWORK FOR OPTIMIZING CPU-IGPU COMMUNICATION ON EMBEDDED PLATFORMS

Francesco Lumpp, Nicola Bombieri, University of Verona, Verona, Italy; Hiren Patel, University of Waterloo, Waterloo, Canada

EMBEDDED RECIPES FOR SECURE AND BUG-FREE SOUPS

Topic Area(s): Embedded and Cross-Layer Security, Security

This session considers building trust in embedded systems, which have become pervasive but also increasingly more complex. The emerging eco-system of embedded devices resembles a delicious soup with several ingredients which at the same time is threatened by a variety of bugs and security attacks – bugs love swimming in fancy soups and the bowl is large! The papers in the session include secure methodologies for memory safety, application-specific attacks and defenses, trusted executions, and legacy code protection.

SHORE: HARDWARE/SOFTWARE METHOD FOR MEMORY SAFETY ACCELERATION ON RISC-V

Kenny Dow, Tuo Li, William Miles, Sri Parameswaran, University of New South Wales, Sydney, Australia

DEEPSTRIKE: REMOTELY-GUIDED FAULT INJECTION ATTACKS ON DNN ACCELERATOR IN CLOUD-FPGA

Yukui Luo,Cheng Gongye, Yunsi Fei, Xiaolin Xu, Northeastern University, Boston, MA

SGX-FPGA: TRUSTED EXECUTION ENVIRONMENT FOR CPU-FPGA HETEROGENEOUS ARCHITECTURE

Ke Xia, Sheng Wei, Rutgers University, Piscataway, NJ; Yukui Luo, Northeastern University ,Xiaolin Xu, Northeastern University, Boston, MA

ROLOAD: SECURING SENSITIVE OPERATIONS WITH POINTEE INTEGRITY

Wende Tan, Yuan Li,Chao Zhang, Xingman Chen, Songtao Yang, Ying Liu, Jianping Wu, Tsinghua University, Beijing, China

REWRITE TO REINFORCE: REWRITING THE BINARY TO APPLY COUNTERMEASURES AGAINST FAULT INJECTION

Pantea Kiaei, Patrick Schaumont, Worcester Polytechnic Institute, Worcester, MA; Cees-Bart Breunesse, Jasper van Woudenberg, Riscure, San Francisco, CA; Mohsen Ahmadi, Arizona State University, Woodland Hills, AZ

EXPLOIT YOUR MODULES FOR COMPLETE VERIFICATION

Topic Area(s): EDA, Design Verification and Validation

This session presents innovations that can boost effectiveness, specificity, automation, and confidence in module-level verification. It contributes an efficient test-generation algorithm for dynamic verification of DRAMs based on deep reinforcement learning and a method based on graybox fuzzing for effective and rapid test generation targeting specific module instances in large RTL designs. The session then proceeds with a tool for automatically constructing formal testbenches using SystemVerilog assertions to aid verification of the control logic governing the interactions between design modules. Finally, it offers a system for efficiently certifying the correctness of first-order logic proofs in satisfiability modulo theories solvers.

APPLICATION OF DEEP REINFORCEMENT LEARNING TO DYNAMIC VERIFICATION OF DRAM DESIGNS

Hyojin Choi, In Huh, Seungju Kim, Jeonghoon Ko, Changwook Jeong, Hyeonsik Son, Kiwon Kwon, Joonwan Chai, Younsik Park, Jaehoon Jeong, Dae Sin Kim, Jung Yun Choi, Samsung Electronics, Hwaseong-si, South Korea

DIRECTFUZZ: AUTOMATED TEST GENERATION FOR RTL DESIGNS USING DIRECTED GRAYBOX FUZZING

Sadullah Canakci, Leila Delshadtehrani, Furkan Eris, Manuel Egele, Ajay Joshi, Boston University, Boston, MA; Michael Bedford Taylor, University of Washington, Seattle, WA

FANTASTIC SOCS AND WHERE TO FIND THEM!

Topic Area(s): EDA, System-on-Chip Design Methodology

With the increasing complexity of systems-on-chip (SoCs), developing efficient SoC design-space exploration methodologies has become challenging. This session presents six papers with novel contributions in the development of HDL framework for SoCs and improvement in SoC performance for acceleration. The first two papers focus on the behavioral design of SoCs and improve their performance for DNN acceleration. The third and fourth papers present co-exploration solutions and structural compilers for SoC-based accelerators. Finally, the last two papers propose new automated-design frameworks for hardware.

ENABLING THE DESIGN OF BEHAVIORAL SYSTEMS-ON-CHIP

Santosh Shetty, Benjamin Carrion Schaefer, The University of Texas at Dallas, Richardson, TX

FAST, COOL AND ERROR TOLERANT COMPUTE-IN-MEMORY

Topic Area(s): Embedded Systems, Near-Memory and In-Memory Computing

Compute-in-Memory (CIM) offers us a promising path to escape traditional Von-Neumann Memory Bottlenecks. This session helps push state of the art in this new paradigm by introducing ultra-low-power 3D-Nand compute substrates for AI, pioneering the deployment of ECC codes for error and variation tolerant CIM, developing high-throughput near-memory accelerators for graph workloads, and enabling ultra-fast max-min searches in DRAMs.

A COMPUTE-IN-MEMORY ARCHITECTURE COMPATIBLE WITH 3D NAND FLASH THAT PARALLELLY ACTIVATES MULTI-LAYERS

Liang Zhao, Chu Yan, Fan Yang, Shifan Gao Yi Zhao, Zhejiang University, Hangzhou, China; Gabriel Rosca, Dan Manea, Zhichao Lu, Hefei Reliance Memory Ltd., Hefei, China

GCIM: A NEAR-DATA PROCESSING ACCELERATOR FOR GRAPH CONSTRUCTION

Lei He, Ying Wang, Cheng Liu, Shengwen Liang, Huawei Li, Xiaowei Li, Chinese Academy of Sciences, Beijing, China

MAX-PIM: FAST AND EFFICIENT MAX/MIN SEARCHING IN DRAM

Fan Zhang, Shaahin Angizi, Deliang Fan, Arizona State University, Tempe, AZ

FROM BRAINS TO BITS

Topic Area(s): Design, Emerging Models of Computation

This session presents six papers that explore advanced algorithms and hardware design to develop the next-generation of brain-inspired intelligent systems. While the first paper discusses neuromorphic hardware-algorithm co-design, the second paper demonstrates algorithm-mapping to neuro-inspired hardware. The next two papers address robustness and resiliency in machine-learning systems. The fifth paper discusses neural processing for event cameras and the last paper of this session presents a methodology to attain robustness against adversarial attacks in hyper-dimensional computing.

NEUROMORPHIC ALGORITHM-HARDWARE CODESIGN FOR TEMPORAL PATTERN LEARNING

Haowen Fang, Zaidao Mei, Qinru Qiu, Syracuse University, Syracuse, NY; Brady Taylor, Ziru Li,Hai (Helen) Li, Duke University, Durham, NC

IN-HARDWARE LEARNING OF MULTILAYER SPIKING NEURAL NETWORKS ON A NEUROMORPHIC PROCESSOR

Amar Shrestha, Haowen Fang, Daniel Patrick Rider, Zaidao Mei, Qinru Qiu, Syracuse University, Syracuse, NY

NOISE-ROBUST DEEP SPIKING NEURAL NETWORKS WITH TEMPORAL INFORMATION

Seongsik Park, Dongjin Lee, Sungroh Yoon, Seoul National University, Seoul, South Korea

SPARKXD: A FRAMEWORK FOR RESILIENT AND ENERGY-EFFICIENT SPIKING NEURAL NETWORK INFERENCE USING APPROXIMATE DRAM

Rachmad Vidya Wicaksana Putra, Muhammad Abdullah Hanif, Technische Universität Wien, Vienna, Austria; Muhammad Shafique, New York University Abu Dhabi, Abu Dhabi, United Arab Emirates

HDTEST: DIFFERENTIAL FUZZ TESTING OF BRAIN-INSPIRED HYPERDIMENSIONAL COMPUTING

Dongning Ma, Xun Jiao, Villanova University, Villanova, PA; Jianmin Guo, Yu Jiang, Tsinghua University, Beijing, China

Access Full Virtual Program:
https://58dac.digitellinc.com/dac/

INTELLIGENT EDGE-CLOUD COMPUTING ARCHITECTURES FOR CPS

Topic Area(s): Design, Design of Cyber-physical Systems and IoT

This session presents techniques for collaborative, efficient, and adaptive design of CPS and IoT systems. Several papers in the session address the key challenge of collaborative edge-cloud execution of machine learning workloads. Innovative techniques such as multi-objective neural architecture search, complexity-aware selection of inference-location, and bandwidth-saving approaches such as adaptive frame clustering and operating on compressed video streams are proposed. The session also features papers that propose design frameworks to automatically learn neural network controllers and a novel priority assignment approach for CAN bus messages.

LENS: LAYER DISTRIBUTION ENABLED NEURAL ARCHITECTURE SEARCH IN EDGE-CLOUD HIERARCHIES

Mohanad Odema, Nafiul Rashid, Berken Utku Demirel, Mohammad Al Faruque, University of California, Irvine, Irvine, CA

APPEALNET: AN EFFICIENT AND HIGHLY-ACCURATE EDGE/CLOUD COLLABORATIVE ARCHITECTURE FOR DNN INFERENCE

Min Li, Yu Li, Ye Tian,Qiang Xu, The Chinese University of Hong Kong, Hong Kong, Hong Kong; Li Jiang, Shanghai Jiao Tong University, Shanghai, China

AN INTELLIGENT VIDEO PROCESSING ARCHITECTURE FOR EDGE-CLOUD VIDEO STREAMING

Chengsi Gao, Ying Wang, Weiwei Chen, Lei Zhang, Chinese Academy of Sciences, Beijing, China

PETRI: REDUCING BANDWIDTH REQUIREMENT IN SMART SURVEILLANCE BY EDGE-CLOUD COLLABORATIVE ADAPTIVE FRAME CLUSTERING AND PIPELINED BIDIRECTIONAL TRACKING

Ruoyang Liu, Lu Zhang, Jingyu Wang, Huazhong Yang, Yongpan Liu, Tsinghua University, Beijing, China

OBFUSCATED PRIORITY ASSIGNMENT TO CAN-FD MESSAGES WITH DEPENDENCIES: A SWAPPING-BASED AND AFFIX-MATCHING APPROACH

Guoqi Xie, Yawen Zhang, Renfa Li, Hunan University, Changsha, China; Debayan Roy, Technische Universität Munich, Changsha, Germany; Wanli Chang, University of York, York, United Kingdom

INTELLIGENT SOFTWARE AND SYSTEM ARCHITECTURES FOR SMART MEMORIES

Topic Area(s): Embedded Systems, Near-Memory and In-Memory Computing

Compute-in-Memory (CIM) platforms rely heavily on reliable and efficient software stacks as well as finely tuned system architectures to leverage their true potential. This session pushes state of the art in this exciting area from developing new CIM architectures to efficiently attain really large attention spans in transformer networks, developing smart memory placement algorithms for heterogenous memories, removing synchronization bottlenecks, and speeding up LU Factorization and deploying PIM to enable ultra-fast mRNA Quantification.

JPDHEAP: A JVM HEAP DESIGN FOR PM-DRAM MEMORIES

Litong You, Yuting Chen, Linpeng Huang, Shanghai Jiao Tong University, Shanghai, China; Tianxiao Gu, Jianmei Guo, Sanhong Li, Alibaba Group, Shanghai, China; Shengan Zheng, Tsinghua University, Shanghai, China

SFLU: SYNCHRONIZATION-FREE SPARSE LU FACTORIZATION FOR FAST CIRCUIT SIMULATION ON GPUS

Jianqi Zhao, Yao Wen, Yuchen Luo, Zhou Jin, Weifeng Liu, China University of Petroleum, Beijing, China; Zhenya Zhou, Empyrean Software Inc, San Jose, CA

PIM-QUANTIFIER: A PROCESSING-IN-MEMORY PLATFORM FOR MRNA QUANTIFICATION

Fan Zhang, Shaahin Angizi, Deliang Fan, Arizona State University, Tempe, AZ; Naima Ahmed Fahmi, Wei Zhang, University of Central Florida, Orlando, FL

KEEP YOUR SECRETS SAFE: SIDE-CHANNEL ATTACKS AND ASSESSMENT TECHNIQUES

Topic Area(s): Hardware Security: Attack and Defense, Security

Side-channel attacks (SCA) have become an important challenge in the design of protected devices. This session focuses on side-channel attack techniques and methodologies to analyze cryptographic hardware implementations. The first half of the session explores SCA attacks on NIST's Round-3 post-quantum digital signature standard finalist FALCON and modern processors using the micro-architectural state held by predictors. The third paper presents a novel methodology to perform cross-device profiling of power and EM attacks with the help of meta transfer learning. The session further explores a pre-silicon SCA resistance assessment at the RTL stage to offer significant speed-up on security evaluations.

NEW PREDICTOR-BASED ATTACKS IN PROCESSORS

Shuwen Deng, Jakub Szefer, Yale University, New Haven, CT

CROSS-DEVICE PROFILED SIDE-CHANNEL ATTACKS USING META-TRANSFER LEARNING

Honggang Yu, Haoqi Shan, Maximillian Panoff, Yier Jin, University of Florida, Gainesville, FL

LEARN TO DESIGN BETTER NOC

Topic Area(s): EDA, In-Package and On-Chip Communication and Networks-on-Chip

Machine Learning (ML) plays an enabling role in NoC/NoI architecture design and optimization. The papers in this session highlight various opportunities to demonstrate the interplay between ML and manycore architectures. In fact, they focus on two broad classes: one is ML-enabled architecture design and the other is NoC architecture for ML accelerator.

NETWORK-ON-INTERPOSER DESIGN FOR AGILE NEURAL-NETWORK PROCESSOR CHIP CUSTOMIZATION

Mengdi Wang, Ying Wang, Cheng Liu,Lei Zhang, Chinese Academy of Sciences, Beijing, China

DISTILLING ARBITRATION LOGIC FROM TRACES USING MACHINE LEARNING: A CASE STUDY ON NOC*

Yuan Zhou, Zhiru Zhang, Cornell University, Ithaca, NY; Hanyu Wang, Shanghai Jiao Tong University, Shanghai, China; Jieming Yin, Lehigh University, Bethlehem, PA

LEARNING TO ACCELERATE CIRCUIT TIMING ANALYSIS

Topic Area(s): EDA, Digital Design, Timing and Simulation

This session presents advanced methods for circuit timing analysis and optimization. The first two papers use new algorithms, data structures, and machine-level optimizations for improving the efficiency of common path pessimism removal (CPPR) problem and path-based timing analysis. The last two papers use machine learning techniques for learning resistor networks from linear measurements and for gate sizing.

A PROVABLY GOOD AND PRACTICALLY EFFICIENT ALGORITHM FOR COMMON PATH PESSIMISM REMOVAL IN LARGE DESIGNS

Zizheng Guo, Yibo Lin, Peking University, Beijing, China; Tsung-Wei Huang, University of Utah, Salt Lake City, UT

GPU-ACCELERATED PATH-BASED TIMING ANALYSIS

Guannan Guo, University of Illinois at Urbana-Champaign, Champaign, IL; Tsung-Wei Huang, University of Utah, Salt Lake City, UT; Yibo Lin, Peking University, Beijing, China; Martin Wong, The Chinese University of Hong Kong, Shatin, Hong Kong

SGL: SPECTRAL GRAPH LEARNING FROM MEASUREMENTS

Zhuo Feng, Stevens Institute of Technology, New Providence, NJ

LET THERE BE LIGHT: EMERGING TECHNOLOGY FOR INTELLIGENT SYSTEMS

Topic Area(s): Design, AI/ML System Design

Modern artificial intelligence (AI) methods have high computing and memory costs. This session focuses on the use of emerging technologies, from silicon photonics to in-memory computing, to mitigate these costs and move us towards more efficient hardware implementations for AI.

OPTIMIZING ADC UTILIZATION THROUGH VALUE-AWARE BYPASS IN RERAM-BASED DNN ACCELERATOR

HanCheon Yun, Hyein Shin, Myeonggu Kang, Lee-Sup Kim, Korea Advanced Institute of Science and Technology, Daejeon, South Korea

LOCKS, CLONES AND HAMMERS: TRUSTING YOUR CHIP IN A VULNERABLE WORLD

Topic Area(s): Hardware Security: Attack and Defense, Security

The session presents reliability attacks in hardware design and proposes new methodologies for trustworthy fabrication. Get more insights into the Rowhammer vulnerability and its state-of-the-art variants by delving into a quantitative analytical model of capacitive-coupling weaknesses in DRAM. Learn about a new logic locking methodology which leverages high-level synthesis to protect IPs while mitigating attacks and minimizing area overhead and key size. Recent advances in Delay-PUFs are further analyzed to expose new modelling attacks that break previous security claims. Finally, a technique to fortify RTL locking techniques with scan-based functional mode isolation helps protect your keys along with your IP.

QUANTIFYING ROWHAMMER VULNERABILITY FOR DRAM SECURITY

Yichen Jiang, Dean Sullivan, Yier Jin, University of Florida, Gainesville, FL; Huifeng Zhu, Xuan Zhang, Washington University in St. Louis, St. Louis, MO; Xiaolong Guo, Kansas State University, Manhattan, KS

SACRED: AN ATTACK FRAMEWORK ON SAC RESISTANT DELAY-PUFS LEVERAGING BIAS AND RELIABILITY FACTORS

Durba Chatterjee, Urbi Chatterjee, Debdeep Mukhopadhyay, Aritra Hazra, Indian Institute of Technology Kharagpur, Kharagpur, India

LOGIC SYNTHESIS GOT EVEN BETTER. CAN YOU BELIEVE IT? MACHINE LEARNING TO THE RESCUE

Topic Area(s): EDA, RTL/Logic Level and High-level Synthesis

The use of machine learning in EDA is deeply impacting the field. In this session we show how machine learning (ML) techniques are used to improve logic synthesis. The first paper uses reinforcement learning to design parallel prefix circuits such as adders and priority encoders that are fundamental in high-performance circuits, while the second paper uses ML to develop a novel technology mapping algorithm. The third paper proposes a framework to generate hardware accelerators for tensor algebra application. The next paper applies FPGA-based synthesis methods to ASIC synthesis. Finally, the last two papers present methods to efficient simulate complex problems. In particular the tight integration between the circuit simulation and a Boolean satisfiability solver, and a cycle-accurate simulation models with RTL models.

TENSORLIB: A SPATIAL ACCELERATOR GENERATION FRAMEWORK FOR TENSOR ALGEBRA

Liancheng Jia, Zizhang Luo, Liqiang Lu, Yun Liang, Peking University, Beijing, China

DEEP INTEGRATION OF CIRCUIT SIMULATOR AND SAT SOLVER

He-Teng Zhang, Jie-Hong Roland Jiang, National Taiwan University, Taipei, Taiwan; Luca Amaru, Synopsys, Sunnyvale, CA; Alan Mishchenko, Robert Brayton, University of California, Berkeley, Berkeley, CA

A MELANGE OF MACHINE LEARNING FRAMEWORKS FOR OPTIMIZATION

Topic Area(s): Design, AI/ML System Design

The landscape of machine learning systems is evolving very fast, and many optimizations are needed across algorithm, compiler, and hardware accelerator designs. In this session, we highlight frameworks for machine learning system optimization covering four topics: memory-efficient graph neural network design, neural hardware-compiler co-design, energy-efficient unsupervised spiking neural network framework, and Bayesian neural network hardware accelerator.

GRAPHSPY: FUSED PROGRAM SEMANTIC EMBEDDING THROUGH GRAPH NEURAL NETWORKS FOR MEMORY EFFICIENCY

Yixin Guo, Yingwei Luo, Xiaolin Wang, Peking University, Beijing, China; Pengcheng Li, Alibaba US Inc., Sunnyvale, CA; Zhenlin Wang, Michigan Technological University, Houghton, MI

SPIKEDYN: A FRAMEWORK FOR ENERGY-EFFICIENT SPIKING NEURAL NETWORKS WITH CONTINUAL AND UNSUPERVISED LEARNING CAPABILITIES IN DYNAMIC ENVIRONMENTS

Rachmad Vidya Wicaksana Putra, Technische Universität Wien, Vienna, Austria; Muhammad Shafique, New York University Abu Dhabi, Abu Dhabi, United Arab Emirates

MEMORY – THE WORKHORSE OF MACHINE LEARNING

Topic Area(s): Design, AI/ML System Design

Memory management and optimization are key considerations for machine learning system design. Memory access dominates power consumption and limits the size of applications that can be run on a system. This session takes on this critical topic with four exciting papers on how to use or implement memory more efficiently for machine learning. Two papers in this session use algorithmic techniques to compress memory usage and the following two papers implement efficient and reliable neural network systems based on ReRAM and beyond.

EFFICIENT TUNSTALL DECODERS FOR COMPRESSED DEEP NEURAL NETWORK

Chunyun Chen, XiaoWei Chen, Mohamed M. Sabry Aly, Nanyang Technological University, Singapore, Singapore; Zhe Wang, Jie Lin, Institute for Infocomm Research, Singapore, Singapore

TAIT: ONE-SHOT FULL-INTEGER LIGHTWEIGHT DNN QUANTIZATION VIA TUNABLE ACTIVATION IMBALANCE TRANSFER

Weixiong Jiang, Xinzhe Liu, Hao Sun, Rui Li, Yajun Ha, ShanghaiTech University, Shanghai, China; Heng Yu, University of Nottingham Ningbo, China, Ningbo, China

BRAHMS: BEYOND CONVENTIONAL RRAM-BASED NEURAL NETWORK ACCELERATORS USING HYBRID ANALOG MEMORY SYSTEM

Tao Song, Xiaoming Chen, Xiaoyu Zhang, Yinhe Han, Chinese Academy of Sciences, Beijing, China

FAULT-FREE: A FAULT-RESILIENT DEEP NEURAL NETWORK ACCELERATOR BASED ON REALISTIC RERAM DEVICES

Hyein Shin, Myeonggu Kang, Lee-Sup Kim, Korea Advanced Institute of Science and Technology, Daejeon, South Korea

NEW TRENDS IN MEMORY ARCHITECTURE DESIGNS FOR I/O SYSTEMS

Topic Area(s): Embedded Systems, Embedded Memory, Storage and Networking

This session describes new architectures and designs for embedded memory and storage devices. The first two papers address the dynamic adjustment of the new RAM-based designs for a reduced refresh rate against an excessive timing margin for the worst-case temperature, as well as looking at cross-layer optimizations. The last two papers look at new possible architectural designs of solid-state drives and memories with alternative technologies.

CDAR-DRAM: AN IN-SITU CHARGE DETECTION AND ADAPTIVE DATA RESTORATION DRAM ARCHITECTURE FOR PERFORMANCE AND ENERGY EFFICIENCY IMPROVEMENT

Chuxiong Lin, Weifeng He, Yanan Sun,Zhigang Mao, Shanghai Jiao Tong University, Shanghai, China; Mingoo Seok, Columbia University, New York City, NY

LOLLIRAM: A CROSS-LAYER DESIGN TO EXPLOIT DATA LOCALITY IN OBLIVIOUS RAM

Yi Wang, Weixuan Chen, Xianhua Wang, Rui Mao, Shenzhen University, Shenzhen, China

BLOWING TREES TO THE GROUND: LAYOUT OPTIMIZATION OF DECISION TREES ON RACETRACK MEMORY

Christian Hakert, Kuan-Hsun Chen, Jian-Jia Chen, Technische Universität Dortmund, Dortmund, Germany; Asif-Ali Khan, Fazal Hameed, Jeronimo Castrillon, Technische Universität Dresden, Dresden, Germany

NOVEL STRATEGIES FOR I/O SYSTEMS AND DEVICES MANAGEMENT

Topic Area(s): Embedded Systems, Embedded Memory, Storage and Networking

This session describes new strategies based on machine learning and cross-layer approaches to improve the performance and energy levels of new I/O devices, as well as addressing the robustness of novel technologies. The first two papers of the session explore a new update strategy against crashes in magnetic recording devices, and the use of reinforcement learning for persistent caches. The last two papers look at new management approaches for mobile memory systems.

MOVE-ON-MODIFY: AN EFFICIENT YET CRASH-CONSISTENT UPDATE STRATEGY FOR INTERLACED MAGNETIC RECORDING

Yuhong Liang, Ming-Chang Yang, The Chinese University of Hong Kong, Hong Kong, Hong Kong

REINFORCEMENT LEARNING-ASSISTED CACHE CLEANING TO MITIGATE LONG-TAIL LATENCY IN DM-SMR

Yungang Pan, Zhiping Jia, Zhaoyan Shen, Shandong University, Qingdao, China; Bingzhe Li, Oklahoma State University, Stillwater, OK; Wanli Chang, Hunan University, Changsha, China; Zili Shao, The Chinese University of Hong Kong, Shatin, Hong Kong

MOBILESWAP: CROSS-DEVICE MEMORY SWAPPING FOR MOBILE DEVICES

Changlong Li, Liang Shi, East China Normal University, Shanghai, China; Chun Jason Xue, City University of Hong Kong, Hong Kong, Hong Kong

PANDA OR GIBBON AND BACK: ATTACKING AND DEFENDING MODERN MACHINE LEARNING SYSTEMS

Topic Area(s): Hardware Security: Attack and Defense, Security

Machine learning, particularly deep neural networks, have been adopted in diverse applications for classification and object detection with exceptional performance. However, the research community has developed powerful attacks on models. The papers in this session include both novel attacks and defenses for machine learning models. One paper presents an adversarial attack against models that process 3D point clouds, typically found in autonomous systems; the second presents a model inversion attack on hyper-dimensional models, which leads to compromise of the training data; the other two papers illustrate how recently proposed in-memory computing systems have built-in defense mechanisms against adversarial attacks.

PRID: MODEL INVERSION PRIVACY ATTACKS IN HYPERDIMENSIONAL LEARNING SYSTEMS

Alejandro Hérnandez-Cano, Universidad Nacional Autónoma de México, Mexico City, Mexico; Rosario Cammarota, Intel Corporation, San Diego, CA; Mohsen Imani, University of California, Irvine, Irvine, CA

LEVERAGING NOISE AND AGGRESSIVE QUANTIZATION OF IN-MEMORY COMPUTING FOR ROBUSTNESS IMPROVEMENT OF DNN HARDWARE AGAINST ADVERSARIAL INPUT AND WEIGHT ATTACKS

Sai Kiran Cherupally, Adnan Siraj Rakin, Shihui Yin, Deliang Fan, Jae-sun Seo, Arizona State University, Tempe, AZ; Mingoo Seok, Columbia University, New York City, NY

RECONFIGURABILITY ACROSS THE SPECTRUM: FROM ICS TO INTELLIGENCE

Topic Area(s): Design, SoC, Heterogeneous, and Reconfigurable Architectures

Reconfigurability has become essential, for efficient processing at all layers of the compute stack. This session presents novel architectures for integrating thousands of cores on a single wafer, as well as interconnect technologies for 3D integration. Moreover, architectures for emerging AI paradigms such as hyper-dimensional computing and graph neural networks are presented. Finally, ultra-fast reconfiguration techniques for CGRAs and for virtualizing FPGAs are discussed.

STOCHD: STOCHASTIC HYPERDIMENSIONAL SYSTEM FOR EFFICIENT AND ROBUST LEARNING FROM RAW DATA

Prathyush Poduval, Indian Institute of Science, Bengaluru, India; Zhuowen Zou, University of California, San Diego, La Jolla, CA; Hassan Najafi, University of Louisiana, Lafayette, LA

HOUMAN HOMAYOUN, UNIVERSITY OF CALIFORNIA, DAVIS, RIVERSIDE, CA

Mohsen Imani, University of California, Irvine, Irvine, CA

MEGATRON: SOFTWARE-MANAGED DEVICE TLB FOR SHARED-MEMORY FPGA VIRTUALIZATION

Yanqiang Liu, Zhengjun Zhang, Linsheng Li, Zhengwei Qi, Haibing Guian, Shanghai Jiao Tong University, Shanghai, China; Jiacheng Ma, Univerity of Michigan, Ann Arbor, MI; Shanghai Jiao Tong University, Shanghai, China

DYGNN: ALGORITHM AND ARCHITECTURE SUPPORT OF DYNAMIC PRUNING FOR GRAPH NEURAL NETWORKS

Cen Chen, Kenli Li, Xiaofeng Zou, Yangfan Li, Hunan University, Chang Sha, China

REINFORCED: ANALOG CIRCUIT SIZING AND LAYOUT

Topic Area(s): EDA, Analog Design, Simulation, Verification and Test

This session starts with four inspiring papers to boost the analog and mixed-signal circuit sizing and optimization process with various flavors of reinforcement learning and Bayesian optimization, as for instance using deep neural network, localized and trust-based modeling and exploration, and exploiting design knowledge. The last two papers present exciting ideas on unsupervised symmetry constraint extraction and interactive analog layout editing with legalization.

TRUST-REGION METHOD WITH DEEP REINFORCEMENT LEARNING IN ANALOG DESIGN SPACE EXPLORATION

Kai-En Yang, National Tsing Hua University, Hsinchu, Taiwan; Chia-Yu Tsai, Hung-Hao Shen, Chen-Feng Chiang, Feng-Ming Tsai, Yiju Ting, Chung-An Wang, Chia-Shun Yeh, Chin-Tang Lai, MediaTek Inc., Hsinchu, Taiwan

LOCAL BAYESIAN OPTIMIZATION FOR ANALOG CIRCUIT SIZING

Konstantinos Touloupas, Nikos Chouridis, Paul Peter Sotiriadis, National Technical University of Athens, Zografou, Greece

RELIABILITY FROM FAB TO MISSION

Topic Area(s): EDA, Manufacturing Test and Reliability

As CMOS scaling continues deeper into the nanometer scale and new device technologies proliferate to enhance performance, reliability of products through their lifetime is an increasing concern. This session presents analysis and mitigation methods to prevent and detect wearout based failures for a variety of technologies, ranging from analog, digital, and mixed signal devices to memristors.

SENSITIVITY IMPORTANCE SAMPLING YIELD ANALYSIS AND OPTIMIZATION FOR HIGH SIGMA FAILURE RATE ESTIMATION

Wenfei Hu, Sen Yin, Zhikai Wang, Zuochang Ye, Yan Wang, Tsinghua University, Beijing, China

PRUNING OF DEEP NEURAL NETWORKS FOR FAULT TOLERANT MEMRISTOR-BASED ACCELERATORS

Ching-Yuan Chen, Krishnendu Chakrabarty, Duke University, Durham, NC

REMAINS OF THE DAY: RERAMS FOR MODERN AI

Topic Area(s): Design, AI/ML System Design

Resistive RAM technology is a promising candidate for AI/ML acceleration. This session focuses on new methods to leverage ReRAM technology for 3D and graph convolutions, and for processing in memory (PIM).

F3D: ACCELERATING 3D CONVOLUTIONAL NEURAL NETWORKS IN FREQUENCY SPACE USING RERAM

Bosheng Liu, Zhuoshen Jiang, Jigang Wu, Peng Liu, Guangdong University of Technology, Guangzhou, China; Xiaoming Chen, Yinhe Han, Chinese Academy of Sciences, Beijing, China

TARE: TASK-ADAPTIVE IN-SITU RERAM COMPUTING FOR GRAPH LEARNING

Yintao He, Ying Wang, Cheng Liu, Huawei Li, Xiaowei Li, Chinese Academy of Sciences, Beijing, China

PIMGCN: A RERAM-BASED PIM DESIGN FOR GRAPH CONVOLUTIONAL NETWORK ACCELERATION

Tao Yang, Dongyue Li, Yibo Han, Yilong Zhao, Fangxin Liu, Xiaoyao Liang, Zhezhi He, Li Jiang, Shanghai Jiao Tong University, Shanghai, China

REPIM: JOINT EXPLOITATION OF ACTIVATION AND WEIGHT REPETITION FOR IN-RERAM DNN ACCELERATION

Chen-Yang Tsai, Chin-Fu Nien, Hsiang-Yun Cheng, Academia Sinica, Taipei, Taiwan; Tz-Ching Yu, Hung-Yu Yeh, National Taiwan University, Taipei, Taiwan

SCALING THE DATA WALL: NOVEL HETEROGENEOUS ARCHITECTURES FOR EMERGING DATA-INTENSIVE APPLICATIONS

Topic Area(s): Design, SoC, Heterogeneous, and Reconfigurable Architectures

With increasing acceleration of computing, data movement has become the major bottleneck in novel/upcoming applications in machine learning, graph analytics, stream processing etc. This session covers novel approaches for accelerating data movement across the design stack ranging from emerging technology to heterogeneous packaging, and domain-specific architectures. In particular, the papers in this session look towards application-driven insights to drive some of the underlying hardware design decisions in memory system design, reconfigurable architectures, photonic interconnections, chiplet-based designs, and 3D ICs.

SKEW-OBLIVIOUS DATA ROUTING FOR DATA INTENSIVE APPLICATIONS ON FPGAS WITH HLS

Xinyu Chen, Hongshi Tan, Bingsheng He, Weng-Fai Wong, National University of Singapore, Singapore, Singapore; Yao Chen, Advanced Digital Sciences Centre, Singapore, Singapore; Deming Chen, University of Illinois at Urbana-Champaign, Urbana-Champaign, IL

FORMULATING DATA-ARRIVAL SYNCHRONIZERS IN INTEGER LINEAR PROGRAMMING FOR CGRA MAPPING

Yijiang Guo, Jiarui Wang, Jiaxi Zhang, Guojie Luo, Peking University, Beijing, China

SECURITY TECHNIQUES ACROSS THE BOARD (STAB)

Topic Area(s): Embedded and Cross-Layer Security, Security

This session presents security defenses and attacks across a range of abstraction layers. The first two papers present machine learning techniques to hardware-based malware detection. The first paper's approach estimates and reduces uncertainty in the detection process and the second paper presents a collaborative federated learning approach. The next two papers investigate side-channel attacks, proposing an architecture to obfuscate timing side-channels and presenting a new interruption-based side-channel attack against a secure enclave. The next paper presents a Network-on-Chip architecture to defend cloud services. The final paper presents a method to detect confidentiality vulnerabilities in mixed hardware/firmware systems using formal verification.

LOAD-STEP: A PRECISE TRUSTZONE EXECUTION CONTROL FRAMEWORK FOR EXPLORING NEW SIDE-CHANNEL ATTACKS LIKE FLUSH+EVICT

Zili Kou, Wenjian He,Wei Zhang, The Hong Kong University of Science and Technology, Sai Kung, Hong Kong; Sharad Sinha, Indian Institute of Technology Goa, Ponda, India

SEMPE: SECURE MULTI PATH EXECUTION ARCHITECTURE FOR REMOVING CONDITIONAL BRANCH SIDE CHANNELS

Andrea Mondelli, Paul Gazzillo, Yan Solihin, University of Central Florida, Orlando, FL

ON-DEVICE MALWARE DETECTION USING PERFORMANCEAWARE AND ROBUST COLLABORATIVE LEARNING

Sanket Shukla, Sai Manoj Pudukotai Dinakarrao, George Mason University, Fairfax, VA; Gaurav Kolhe, Setareh Rafatirad, University of California, Davis, CA

SHIPP – SECURITY HARDENING FOR INTELLECTUAL PROPERTY PROTECTION

Topic Area(s): Hardware Security: Primitives, Architecture, Design & Test, Security

This session covers the topic of intellectual property protection through piracy detection and secure design flow using high level synthesis tools and emerging devices. The presenters will discuss state of the art graph neural network-based piracy detection schemes, the implementation of side-channel attack resilient domain-oriented masking using high-level-synthesis to improve design time, and the security of hardware IP using emerging spin-based devices that utilize reconfigurable IP blocks. In addition, the use of architectural features for resource binding will be discussed as a means to enhance SAT resilience.

GNN4IP: GRAPH NEURAL NETWORK FOR HARDWARE INTELLECTUAL PROPERTY PIRACY DETECTION

Rozhin Yasaei, Shih-Yuan Yu, Emad Kasaeyan Naeini, Mohammad Abdullah Al Faruque, University of California, Irvine, Irvine, CA

SHORTEST PATH TO SECURED HARDWARE: DOMAIN ORIENTED MASKING WITH HIGH-LEVEL-SYNTHESIS

Rajat Sadhukhan, Sayandeep Saha, Debdeep Mukhopadhyay, Indian Institute of Technology Kharagpur, Kharagpur, India

SECURING HARDWARE VIA DYNAMIC OBFUSCATION UTILIZING RECONFIGURABLE INTERCONNECT AND LOGIC BLOCKS

Gaurav Kolhe, Soheil Salehi, Tyler Sheaves, Setareh Rafatirad, Houman Homayoun, University of California, Davis, Davis, CA; Sai Manoj Pudukotai Dinakarrao, Avesta Sasan, George Mason University, Fairfax, VA

SMARTER COMPUTE ENGINES FOR GREENER ML

Chair/Co-Chair: Narasinga Rao (Oak Ridge National Laboratory); Weiwen Jiang (University of Notre Dame)

This world is always seeking better hardware accelerators to improve machine learning computing performance. This session presents four research works focusing on optimizing computer hardware to improve machine learning execution performance. Efficient hardware accelerators incorporated with innovative optimizations are presented in this session to accelerate widely-used machine learning networks, such as 2D and 3D convolutional neural networks as well as reinforcement learning, with less energy consumption.

AN ENERGY-EFFICIENT LOW-LATENCY 3D-CNN ACCELERATOR LEVERAGING TEMPORAL LOCALITY, FULL ZERO-SKIPPING, AND HIERARCHICAL LOAD BALANCE

Changchun Zhou, Min Liu, Siyuan Qiu, Hailong Jiao, Peking University Shenzhen Graduate School, Shenzhen, China; Yifan He, Reconova Technologies, Xiamen, China

SMARTER MEMORY SOLUTIONS FOR FASTER ML

Topic Area(s): Design, AI/ML System Design

The well-known memory-wall issue is the major bottleneck of data-intensive machine learning based computing. This session presents two different approaches to tackle this issue through either emerging in-memory computing architecture based on SRAM/RRAM or optimizing dynamic refresh of DRAM.

A CHARGE-SHARING BASED 8T SRAM IN-MEMORY COMPUTING FOR EDGE DNN ACCELERATION

Kyeongho Lee, Sungsoo Cheon, Joongho Jo, Jongsun Park, Korea University, Seoul, South Korea; Woong Choi, Sookmyung Woman's University, Seoul, South Korea

ASBP: AUTOMATIC STRUCTURED BIT-PRUNING FOR RRAM-BASED NN ACCELERATOR

Songyun Qu, Ying Wang, Lei Zhang, Chinese Academy of Sciences, Beijing, China; Bing Li, Capital Normal University, Beijing, China

ADROIT: AN ADAPTIVE DYNAMIC REFRESH OPTIMIZATION FRAMEWORK FOR DRAM ENERGY SAVING IN DNN TRAINING

Xinhan Lin, Liang Sun, Leibo Liu, Xiangyu Li, Shaojun Wei, Shouyi Yin, Tsinghua University, Beijing, China; Fengbin Tu, University of California, Santa Barbara, Santa Barbara, CA

SMARTER SOFTWARE FRAMEWORKS FOR EASIER ML DEVELOPMENT

Topic Area(s): Design, AI/ML System Design

It is always painful and difficult for software engineers with little ML background to craft a high performance and efficient ML system. This session presents a collection of novel software frameworks for improving the productivity of ML practitioners by assisting the development of high-performance ML accelerators, novel ML algorithms, and emerging ML applications.

CASCADEHD: EFFICIENT MANY-CLASS LEARNING FRAMEWORK USING HYPERDIMENSIONAL COMPUTING

Yeseong Kim, Jiseung Kim, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea; Mohsen Imani, University of California, Irvine, Irvine, CA

SPACE: SECURITY OF POST-QUANTUM AND ACCELERATOR-BASED CRYPTOGRAPHIC ENGINES

Topic Area(s): Hardware Security: Primitives, Architecture, Design & Test, Security

The security of post-quantum and accelerator rich cryptographic platforms requires novel techniques and methodologies that extend across the computing stack. From novel neural network models to highly optimized architectures for post-quantum crypto, this session covers an array of methods that can be applied to enhance the security of critical next generation systems. In addition, architectural techniques that validate the integrity of data and enhance the properties of branch predictors are discussed that provide additional security assurances in accelerator rich systems.

SEALING NEURAL NETWORK MODELS IN ENCRYPTED DEEP LEARNING ACCELERATORS

Pengfei Zuo, Yu Hua, Huazhong University of Science and Technology, Wuhan, China; Ling Liang, Xingfeng Xie, Yuan Xie, University of California, Santa Barbara, Santa Barbara, CA; Xing Hu, Chinese Academy of Sciences, Beijing, China

CLASSIFYING COMPUTATIONS ON MULTI-TENANT FPGAS

Mustafa Gobulukoglu, Kastner Lab, La Jolla, CA; Colin Drewes, Ryan Kastner, University of California, San Diego, La Jolla, CA; Bill Hunter, Georgia Tech Research Institute, Atlanta, GA; Dustin Richmond, University of Washington, Seattle, WA

A LIGHTWEIGHT ISOLATION MECHANISM FOR SECURE BRANCH PREDICTORS

Lutan Zhao, Peinan Li, Rui Hou, Jiazhen Li, Lixin Zhang, Dan Meng, Chinese Academy of Sciences, Beijing, China; Michael C. Huang, University of Rochester, Rochester, NY; Xuehai Qian, University of Southern California, Los Angeles, CA

CUCKOONSAI: AN EFFICIENT MEMORY AUTHENTICATION USING AMALGAM OF CUCKOO FILTERS AND INTEGRITY TREES

Omais Shafi, Ismi Abidi, Indian Institute of Technology Delhi, New Delhi, India

OPTIMIZED POLYNOMIAL MULTIPLIER ARCHITECTURES FORPOST-QUANTUM KEM SABER

Andrea Basso, Sujoy Sinha Roy, University of Birmingham, Birmingam, United Kingdom

TALES OF MEMORY, LATENCY, AND ENERGY OPTIMIZATIONS

Topic Area(s): Embedded Systems, Embedded System Design Methodologies

This session covers novel techniques for memory, latency, and energy optimizations in emerging processing chip platforms. The first paper proposes a co-design of OS and SSD that exploits the redundancy in transactional systems to cut ultra-dense SSDs' read tail latency. The second paper proposes a hardware-friendly multi-stage Personalized Pagerank to minimize local latency with a tight memory budget through stage and linear decomposition. The third paper presents an information-theoretic framework that creates pareto-optimal resource management policies for mobile heterogeneous SoCs. The fourth paper tackles the problem of dynamic range growth for the efficient implementation of fixed-point FFT.

REPTAIL: CUTTING STORAGE TAIL LATENCY WITH INHERENT REDUNDANCY

Yun-Chih Chen, Chun-Feng Wu, National Taiwan University, Taipei, Taiwan; Yuan-Hao Chang, Academia Sinica, Taipei, Taiwan; Tei-Wei Kuo, City University of Hong Kong, Hong Kong, Hong Kong

MELOPPR: SOFTWARE/HARDWARE CO-DESIGN FOR MEMORY-EFFICIENT LOW-LATENCY PERSONALIZED PAGERANK

Lixiang Li, Dalhousie University, Halifax, Canada; Yao Chen, Advanced Digital Sciences Centre, Singapore, Singapore; Zacharie Zirnheld, Pan Li, Purdue University, West Lafayette, IN; Cong Hao, Georgia Institute of Technology, Atlanta, GA

LEARNING PARETO-FRONTIER RESOURCE MANAGEMENT POLICIES FOR HETEROGENEOUS SOCS: A INFORMATION-THEORETIC APPROACH

Aryan Deshwal, Syrine Belakaria, Ganapati Bhat, Janardhan Rao Doppa, Partha Pande, Washington State University, Pullman, WA

BITWIDTH-OPTIMIZED ENERGY-EFFICIENT FFT DESIGN VIA SCALING INFORMATION PROPAGATION

Xinzhe Liu, Fupeng Chen, ShanghaiTech University, Shanghai, China; Raees Kizhakkumkara Muhamad, David Blinder, Peter Schelkens, Vrije Universiteit Brussel, Brussel, Belgium; Dessislava Nikolova, Francky Catthoor, IMEC, Leuven, Belgium; Yajun Ha, ShanghaiTech University, Shanghai, China

THAT QUANTUM SESSION EVERYONE IS TALKING ABOUT

Topic Area(s): Design, Quantum Computing

Quantum noise is a major roadblock towards its applicability. Furthermore, there is a strong need to accelerate the quantum simulations and explore the application domains of quantum computing. This session addresses these challenges via novel approaches to design and simulate quantum circuits, develop various error mitigation/correction techniques and explore applications in machine learning.

AN EFFICIENT ALGORITHM FOR SPARSE QUANTUM STATE PREPARATION

Niels Gleinig, Torsten Hoefler, ETH Zürich, Zürich, Switzerland

BIT-SLICING THE HILBERT SPACE: SCALING UP ACCURATE QUANTUM CIRCUIT SIMULATION

Yuan-Hung Tsai, Jie-Hong Roland Jiang, Chiao-Shan Jhang, National Taiwan University, Taipei, Taiwan

MITIGATING CROSSTALK IN QUANTUM COMPUTERS THROUGH COMMUTATIVITY-BASED INSTRUCTION REORDERING

Lei Xie, Jidong Zhai, Weimin Zheng, Tsinghua University, Beijing, China

QECOOL: ON-LINE QUANTUM ERROR CORRECTION WITH A SUPERCONDUCTING DECODER FOR SURFACE CODE

Yosuke Ueno, Masaaki Kondo, Yutaka Tabuchi, University of Tokyo, Japan; Masamitsu Tanaka, Nagoya University, Nagoya, Japan; Yasunari Suzuki, NTT, Musashino, Japan

A BRIDGE-BASED COMPRESSION ALGORITHM FOR TOPOLOGICAL QUANTUM CIRCUITS

Chen-Hao Hsu, Wan-Hsuan Lin, Wei-Hsiang Tseng, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

TRANSFORMING EMERGING TECHNOLOGIES IN THE POST-MOORE ERA

Topic Area(s): Design, Emerging Device Technologies

The impending end of Moore's Law shifts the focus of technology competitions from applications back to developing new devices. In this session, we study some transformative devices including memristors, nanomagnets, superconducting materials, and nanophotonics. These enabling technologies, which are still in their nascent stage, start to emerge as the candidate to replace CMOS devices in the post-Moore era. The four papers cover some compelling innovations in logic circuits design, computing architectures, and synthesis tools that are critical to the adoption of these technologies.

BAYESIAN INFERENCE BASED ROBUST COMPUTING ON MEMRISTOR CROSSBAR

Di Gao, Qingrong Huang, Xunzhao Yin, Cheng Zhuo, Zhejiang University, Hangzhou, China; Grace Li Zhang, Bing Li, Ulf Schlichtmann, Technische Universität Munich, Munich, Germany

TAMPER-RESISTANT OPTICAL LOGIC CIRCUITS BASED ON INTEGRATED NANOPHOTONICS

Jun Shiomi, Shuya Kotsugi, Boyu Dong, Hidetoshi Onodera, Kyoto University, Kyoto, Japan; Akihiko Shinya Masaya Notomi, NTT Basic Research Laboratories, Atsugi, Japan

VERIFICATION IS RUNNING: WHAT ARE THE NEXT STOPS?

Topic Area(s): EDA, Design Verification and Validation

This session features advances in verification and testing to address increasing system complexity, security and emerging technologies.

It first proposes abstractions and mechanisms to detect bugs and vulnerabilities at system-level.

To this aim, trace notation for ISA definition is proposed for capture processor behaviors, while efficient extraction of reset-controlled events and concolic testing are used for detecting security vulnerabilities in SoC with asynchronous partial reset.

The session also addresses emerging directions in the verification of control systems based on neural networks and equivalence checking of quantum circuits. This is achieved by synthesizing barrier certificates of closed-loop systems controlled by neural networks and by employing tensor network contraction for computing the fidelity between an ideal quantum circuit and its noisy implementations.

SOCCAR: DETECTING SOC SECURITY VIOLATIONS UNDER ASYNCHRONOUS RESETS

Xingyu Meng, Kanad Basu, The University of Texas at Dallas, Richardson, TX; Kshitij Raj, Atul Prasad Deb Nath, Sandip Ray, University of Florida, Gainesville, FL

SYNTHESIZING BARRIER CERTIFICATES OF NEURAL NETWORK CONTROLLED CONTINUOUS SYSTEMS VIA APPROXIMATIONS

Meng Sha, Xin Chen, Yuzhe Ji, Qingye Zhao, Enyi Tang, Xuandong Li, Nanjing University, Nanjing, China; Zhengfeng Yang, East China Normal University, Shanghai, China; Wang Lin, Zhejiang Sci-Tech University, Hangzhou, China; Qiguang Chen, British Columbia Academy, Nanjing, China

APPROXIMATE EQUIVALENCE CHECKING OF NOISY QUANTUM CIRCUITS

Xin Hong, Mingsheng Ying, Yuan Feng, Xiangzhen Zhou, Sanjiang Li, University of Technology Sydney, Sydney, Australia

WHEN THEY GO HIGH – WE GO LOW (IN COMPUTATION)

Topic Area(s): Design, Approximate Computing for AI/ML

Low computational complexity improves hardware efficiency. To that end, this session reports cutting-edge developments in the domain of Approximate Computing for AI Hardware-Software codesign. Along with novel algorithmic techniques addressing pruning and reduced precision, the session dives deeper into cross-layer optimization and approximate arithmetic for different types of deep neural network accelerators ranging from embedded FPGA systems to in-memory computing.

CLAPPED: A DESIGN FRAMEWORK FOR IMPLEMENTING CROSS-LAYER APPROXIMATION IN FPGA-BASED EMBEDDED SYSTEMS

Salim Ullah, Siva Satyendra Sahoo, Akash Kumar, Technische Universität Dresden, Dresden, Germany

COSAIM: COUNTER-BASED STOCHASTIC-BEHAVING APPROXIMATE INTEGER MULTIPLIER FOR DEEP NEURAL NETWORKS

Shuyuan Yu, Yibo Liu, Sheldon Tan, University of California, Riverside, Riverside, CA

BAYESFT: BAYESIAN OPTIMIZATION FOR FAULT TOLERANT NEURAL NETWORK ARCHITECTURE

Nanyang Ye, Zhicheng Fang, Huaying Wu, Xiaoyao Liang, Shanghai Jiao Tong University, China; Jingbiao Mei, Ziqing Zhang,University of Cambridge, Cambridge, United Kingdom; Yuwen Zhang, University College London, London, United Kingdom

ALGORITHMS WITH GPUS AND MACHINE LEARNING

Topic Area(s): EDA, Machine Learning/AI

Session Organizer: Brucek Khailany, NVIDIA, Austin, TX; David Pan, The University of Texas at Austin, Austin, TX

Recent advancements in GPU accelerated computing platforms and machine learning (ML) based optimization techniques have led to exciting recent research progress with large speedups on many EDA algorithms fundamental to semiconductor design flows. In this session, we highlight ongoing research deploying GPUs and ML to mask synthesis, IC design automation, and PCB design at commercial EDA vendors and semiconductor design and manufacturing companies. Research into mask synthesis techniques shows the potential for GPUs to accelerate inverse lithography and for running training and inference of ML models for process modeling. In PCB layout editing, GPU-accelerated path rendering techniques can scale to millions of rendered objects with interactive responsiveness. In IC physical design, GPU-accelerated reinforcement learning for DRC fixing combined with traditional EDA optimization techniques can automate standard cell layout generation. The combination of GPUs and ML can enable large speedups and automate key EDA tasks previously seen as intractable.

NVCELL: STANDARD CELL LAYOUT IN ADVANCED TECHNOLOGY NODES WITH REINFORCEMENT LEARNING

Haoxing Ren, NVIDIA, Austin, TX

DEMOCRATIZING DESIGN AUTOMATION: NEXT GENERATION OPENSOURCE TOOLS FOR HARDWARE SPECIALIZATION

Topic Area(s): EDA, Machine Learning/AI

Session Organizer: Antonino Tumeo, Pacific Northwest National Laboratory, Richland, WA

The growth of autonomous systems, coupled with design efforts and cost challenges brought by new technology nodes, is driving the need for generators that could quickly transition high-level algorithmic specifications to specialized hardware implementations. The necessity to explore additional dimensions of the design space (e.g., accuracy, security, system size and cooling) is further emphasizing the need for interoperable tools. This special session focuses on efforts for interoperable, modularized, and opensource tools to provide a no-human-in-the-loop design cycle from high-level specifications to ASICs and further promote novel research. The first talk introduces the status quo and CIRCT, an initiative aiming at applying MLIR and the LLVM development methodology to design automation. The second and third talks describe state-of-the-art tools, for high-level synthesis, and for logic synthesis, respectively, and discuss explorations to bridge the two. The session overviews how interoperability is achieved today, opportunities, challenges, and new perspectives enabled by community efforts.

CIRCT – CIRCUIT IR COMPILERS AND TOOLS

Stephen Neuendorffer, Xilinx, San Jose, CA

BAMBU: AN OPEN-SOURCE RESEARCH FRAMEWORK FOR THE HIGH-LEVEL SYNTHESIS OF COMPLEX APPLICATIONS

Fabrizio Ferrandi, Politecnico di Milano, Milan, Italy; Vito Giovanni Castellana, Marco Minutoli, Pacific Northwest National Laboratory, Richland, WA; Serena Curzel, Pietro Fezzardi, Michele Fiorito, Marco Lattuada, Christian Pilato, Politecnico di Milano, Milan, Italy

GETTING THE MOST OUT OF YOUR CIRCUITS WITH HETEROGENEOUS LOGIC SYNTHESIS

Pierre-Emmanuelle Gaillardon, Ashton Snelgrove, Xifan Tang, University of Utah, Salt Lake City, UT; Scott Temple, Walter Lau Neto, University of Utah, Salt Lake City, UT

DESIGN AUTOMATION OF AUTONOMOUS SYSTEMS: STATE-OF-THE-ART AND FUTURE DIRECTIONS

Topic Area(s): Autonomous Systems, Design

Session Organizer: Qi Zhu, Northwestern University, Evanston, IL; Shaoshan Liu, PerceptIn, Mountain View, CA

Design processes leverage various automated tools to support requirement engineering, design, implementation, verification, validation, testing and evaluation. In the domains of automotive and aerospace, design automation processes and tools have been architected and developed over the years and used to design products with established level of confidence. The recent success of Artificial Intelligence (AI) has shown great promises in improving system intelligence and autonomy for these applications. However, the adoption of those techniques also presents significant challenges for the design processes to ensure system safety, performance, reliability, security, etc. This special session will discuss essential design automation processes/tools and industrial efforts to support the development and deployment of future autonomous systems, particularly in the domains of automotive and aerospace.

SAFETY IN AUTONOMOUS DRIVING: CAN TOOLS OFFER GUARANTEES?

Alberto Sangiovanni-Vincentelli, Sanjit A. Seshia, University of California, Berkeley, Berkeley, CA Daniel Fremont, University of California, Santa Clara, Santa Clara, CA

REQUIREMENT SPECIFICATION, ANALYSIS AND VERIFICATION FOR AUTONOMOUS SYSTEMS

Alessandro Pinto, Raytheon Technologies Research Center, Berkeley, CA

HARDWARE/SOFTWARE DESIGN METHODS CO-SYNTHESIS AND OPTIMIZATION FOR AUTONOMOUS SYSTEMS

Simon Burton, Fraunhofer Institute for Cognitive Systems IKS, Munich, GermanWanli Chang, Hunan University, Changsha, China; Shuai Zhao, Nan Chen, Neil Audsley, University of York, York, United Kingdom; Ting Chen, University of Electronic Science and Technology of China, Chengdu, China

TOWARDS FULLY INTELLIGENT TRANSPORTATION THROUGH INFRASTRUCTURE-VEHICLE COOPERATIVE AUTONOMOUS DRIVING: CHALLENGES AND OPPORTUNITIES

Author: Bo Yu, PerceptIn, Beijing, China; Jie Tang, South China University of Technology, Guangzhou, China

HARDWARE AWARE LEARNING FOR MEDICAL IMAGE COMPUTING AND COMPUTER ASSISTED INTERVENTION

Topic Area(s): Design, Machine Learning/AI

Session Organizer: Lei Yang, University of New Mexico, Albuquerque, NM

Deep learning has recently demonstrated performance comparable with, and in some cases superior to, that of human experts in medical image computing. However, deep neural networks are typically very large, which combined with large medical image sizes create various hurdles towards their clinical applications. In medical image computing, not only accuracy but also latency and security are of primary concern, and the hardware platforms are sometimes resource-constrained. The first two talks in this session propose novel solutions for the data acquisition and data processing stages in medical image computing respectively, using hardware-oriented schemes for lower latency, memory footprint and higher performance in embedded platforms. Considering the privacy requirement, the third talk further demonstrates a software/hardware co-exploration framework for hybrid trusted execution environment in medical image computing, preserving privacy while achieving higher efficiency than human experts.

HARDWARE-AWARE REAL-TIME MYOCARDIAL SEGMENTATION QUALITY CONTROL IN CONTRAST ECHOCARDIOGRAPHY

Dewen Zeng, Yukun Ding, Yiyu Shi, University of Notre Dame, South Bend, IN; Haiyun Yuan, Boston Children's Hospital, Boston, MA; Lei Yang, University of New Mexico, Albuquerque, NM; Meiping Huang, Xiaowei Xu, Jian Zhuang, Guangdong Provincial Peop

KCC-NET FOR COMPRESSION OF BIOMEDICAL IMAGE SEGMENTATION NETWORKS

Danny Chen, Suraj Mishra, Notre Dame, South Bend, IN

PRIVACY-PRESERVING MEDICAL IMAGE SEGMENTATION VIA HYBRID TRUSTED EXECUTION ENVIRONMENT

Weiwen Jian, Notre Dame, South Bend, IN; Takashi Sato, Kyoto University, Kyoto, Japan; Song Bian, Kyoto University, Kyoto, Japan

MACHINE LEARNING MEETS COMPUTING SYSTEMS DESIGN: THE BIDIRECTIONAL HIGHWAY

Topic Area(s): Design, Machine Learning/AI

Session Organizer: Partha P. Pande, Washington State University, Pullman, WA

With the rising needs of advanced algorithms for large-scale data analysis and data-driven discovery, and significant growth in emerging applications from the edge to the cloud, we need low-cost, high-performance, energy-efficient, and reliable computing systems targeted for these applications. Developing these application-specific hardware elements must become easy, inexpensive, and seamless to keep up with extremely rapid evolution of AI/ML algorithms and applications. Therefore, it is of high priority to create innovative design frameworks enabled by data analytics and machine learning that reduces the engineering cost and design time of application-specific hardware. There is also a need to continually advance software algorithms and frameworks to better cope with data available to platforms at multiple scales of complexity. To the best of our knowledge, this is the first special session at any EDA conference that explores both directions of cross-fertilization between computing system design and ML.

MASTERING THE THREE PILLARS OF ACCELERATOR DESIGN FOR DEEP LEARNING

Sunil Shukla, IBM, Yorktown Heights, NY

FUNCTIONAL CRITICALITY CLASSIFICATION OF STRUCTURAL FAULTS IN AI ACCELERATORS

Presenter(s): Jonti Talukdar, Arjun Chaudhuri, Duke University, Durham, NC
Author(s): Krishnendu Chakrabarty, Biresh Kumar Joardar, Duke University, Durham, NC; Janna Doppa, Washington State University, Pullman, WA

CONVERGENCE OF SOC ARCHITECTURE AND SEMICONDUCTOR MANUFACTURING THROUGH AI/ML SYSTEMS

Presenter(s): Pushkar Ranade, Intel Corporation, Hillsboro, OR
Author(s): Srinivas Bodapati, Intel Corporation, Santa Clara, CA

A QUANTUM LEAP IN MACHINE LEARNING: FROM APPLICATIONS TO IMPLEMENTATIONS

Topic Area(s): Design

Session Organizer: Robert Wille, Johannes Kepler University, Linz, Austria

Classical machine learning techniques that have been extensively studied for discriminative and generative tasks are cumbersome and, in many applications, inefficient. They require millions of parameters and remain inadequate in modeling a target probability distribution. For example, computational approaches to accelerate drug discovery using machine learning face curse-of-dimensionality due to exploding number of constraints that need to be imposed using reinforcement learning. Quantum machine learning (QML) techniques, with strong expressive power, can learn richer representation of data with less number of parameters, training data and training time. However, the methodologies to design these QML workloads and their training is still emerging. Furthermore, usage model of the small and noisy quantum hardware in QML tasks to solve practically relevant problems is an active area of research. This special session will provide insights on building, training and exploiting scalable QML circuits to solve socially relevant combinatorial optimization applications including drug discovery.

BUILDING SCALABLE VARIATIONAL CIRCUIT TRAINING FOR MACHINE LEARNING TASKS

Kathleen Hamilton, Emily Lynn, Titus Morris, Tyler Kharazi, Ryan Bennink, Raphael Pooser, Oak Ridge National Lab

QUANTUM RANDOM ACCESS CODING IN QUANTUM MACHINE LEARNING APPLICATIONS

Rudy Raymond Harry Putra, IBM, Tokyo, Japan; Napat Thumwanit, Chayapol Lortararparset, University of Tokyo, Tokyo, Japan

DRUG DISCOVERY APPROACHES USING QUANTUM MACHINE LEARNING

Mahabubul Alam, Junde Li, Swaroop Ghosh, Mike Sha, Jian Wang, Nikolay V. Dokholyan, Pennsylvania State University, University Park, PA

SECURITY-AWARE COMPUTER AIDED ELECTRONIC DESIGN

Event Type: Special Session
Topic Area(s): Security

Chair/Co-Chair: Ujjwal Guin (Auburn University)

Session Organizer: Ujjwal Guin, Auburn University, Auburn, AL

Due to the lack of standard tools, methods, or solutions currently in practice, there is an urgent need for developing chip-level security solutions. The primary reason for the lack of security features in a chip has resulted from the economic hurdles and technical trade-offs often associated with chip design. This special session will highlight these concerns and opportunities. The first presentation will be an overview of the benefits of the security-aware CAD flows and discuss the attack surfaces such as side-channel attacks, reverse engineering, supply chain attacks, and malicious hardware attacks that need to be addressed. The second talk will focus on Security-Aware Computer-Aided Electronic Design Tools. The third talk will focus on Independent Verification & Validation (IV&V) of Security-Aware CAD tools. The final talk will discuss the Integration of IC Design Changes into a BlockChain for Traceability in the Electronic CAD Flow.

INTEGRATION OF IC DESIGN CHANGES INTO A BLOCKCHAIN FOR TRACEABILITY IN AISS DESIGN FLOW

Roman Vaculin, IBM, New York City, NY

SMART ROBOTS WITH SENSING, UNDERSTANDING, AND ACTING

Topic Area(s): Autonomous Systems, Machine Learning/AI

Session Organizer: Janardhan Rao (Jana) Doppa, Washington State University, Pullman, WA; Yu Wang, Tsinghua University, Beijing, China

The robotics industry holds enormous promise but development rates are bogged down by increasingly complex software to meet performance and safety requirements in the face of long tail events. Moreover, intelligent robots should adapt in the field to unexpected conditions that may not have ever been observed during design time. Design automation for autonomy has the potential to accelerate the rate at which we overcome these challenges (particularly outside of the autonomous driving sector which throws massive resources at the problem.) In this talk I discuss how the key tools of machine learning, AutoML, simulation, and design optimization have made an impact on systems development for two medical robotics projects - ocular microsurgery and tele-nursing - and will continue to make an impact in other sectors like automated warehouses, service robots, and agriculture.

PROGRESS AND CHALLENGES OF 3D VISION & DEEP LEARNING IN INDUSTRIAL ROBOTICS APPLICATION

Tianlan Shao, Mech-Mind Inc, Beijing, China

TACOS: TACTILE CORE WITH OPTICAL STRING SENSOR FOR ROBOTIC SMART SKIN

Huichan Zhao, Jingyi Zhou, Zheyu Liu, Xinjun Liu, Qi Wei, Fei Qiao, Tsinghua University, Tsinghua, China

LATE-BREAKING RESULTS POSTERS

A NOVEL MACHINE-LEARNING BASED SOC PERFORMANCE MONITORING METHODOLOGY UNDER WIDE-RANGE PVT VARIATIONS WITH UNKNOWN CRITICAL PATHS

Ding-Hao Wang, Pei-Ju Lin,Hui-Ting Yang, Global Unichip Corp., Hsinchu, Taiwan; Ching-An Hsu, Sin-Han Huang, Mark Po-Hung Lin, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

POLYNOMIAL FORMAL VERIFICATION OF FAST ADDERS

Alireza Mahzoon, Rolf Drechsler, University of Bremen, Bremen, Germany

REINFORCEMENT LEARNING FOR SCALABLE LOGIC OPTIMIZATION WITH GRAPH NEURAL NETWORKS

Xavier Timoneda, Lukas Cavigelli, Huawei Technologies Switzerland AG, Zürich, Switzerland

ALL ROUTES LEAD TO CLOSING TIMING

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Topic Area(s): Back-End Design

This session focuses on how to build advocacy in your organization to leverage public cloud platforms to help accelerate throughput and time to market. In this session, we'll walk through the advocacy playbook, hear from a company that used those principles to get a proof of concept started, and end with a panel session with EDA on cloud experts.

MIDDLE OF LAYER ROUTING ENABLEMENT FOR INCREASING ROUTING RESOURCE

SungOk Lee, Dayeon Cho,Sangdo Park, Yeongyeong Shin, Joonyoung Shin, Sua Lee, Hyung-Ock Kim, Sangyun Kim, Samsung Electronics, Hwaseong, South Korea

ENABLING HIERARCHICAL FLATTENED FUNCTIONAL ECO FLOW FOR QUALITY PATCH GENERATION WITH RUNTIME BENEFITS

Sidharth Ranjan Panda, Intel Corporation, Bangalore, India

METHODOLOGY FOR ACCURATE ANALYSIS OF DYNAMIC VOLTAGE DROP INDUCED CLOCK JITTER FOR IMPROVED PPA

Mathew Kaipanatu, Google, Bangalore, India

CHIP DESIGN AND CLOUD: THE GOOD, THE EMERGING, AND THE POTENTIAL

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Event Type: Designer, IP and Embedded Systems Track Presentations

Topic Area(s): Cloud

In this first-of-its-kind session, you will hear multiple perspectives, from educators to researchers to practitioners on how they have leveraged cloud for their work. Cloud provides a foundational platform to accelerate silicon workflows by providing seemingly limitless capacities. Presentations in this session cover how cloud enabled enhanced delivery of academic courses, technologies to implement hybrid flows, real-world experience from a cloud-based foundry, cloud-native EDA tools or "EDA 3.0", and fnally, workloads that see oversized benefits from cloud.

IP META DATA – CLOUD DB A NOVEL METHOD FOR SOC INTEGRATION

Nikhil Krishna Gopalakrishna, Intel Corporation, Santa Clara, CA; Ajit Dingankar, Intel Corporation, Folsom, CA; Bindu Lalitha, Intel Corporation, Hillsboro, OR

EMBEDDED SYSTEMS! PROJECTS AND SOLUTIONS

Topic Area(s): Embedded Systems

Embedded systems have become a necessity in every aspect of our daily life. Embedded systems design and deployment pose significant challenges in the areas of compute, power, privacy, security, connectivity, scalability and reliability. DAC Embedded systems track brings together embedded system software developers, IC designers, security experts and product managers to analyze and discuss current and future trends in the embedded systems field. In this Embedded systems session we will be discussing the challenges in security, real-time software design, Machine learning hardware accelerators, and performance modeling software design challenges.

BLOF:A BINARY GROUP LIST BASED LOW OVERHEAD INDEX STRUCTURE AND FAST FILE MANAGEMENT METHOD

Lei Qiao, Jingjing Jiang, Bo Liu, Bin Gu, Zhi Ma, Beijing Institute of Control Engineering, Beijing, China; Mengfei Yang, China Academy of Space Technology, Beijing, China

"DEBUG IN/ON/WITH THE VIRTUAL PLATFORM" – PLEASE CLARIFY!

Jakob Engblom, Intel Corporation, Stockholm, Sweden

MONICA – ON-CHIP MONITORING SYSTEMS CHARACTERIZATION

Giacomo Valente, Federica Caruso, Luigi Pomante, Tania Di Mascio, Università degli Studi dell'Aquila, L'Aquila, Italy

EXPLORING THE NEW WAVES

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Topic Area(s): Back-End Design

VIRTUAL ENVIRONMENT FOR DEVELOPING REINFORCEMENT LEARNING AND ITS APPLICATION FOR THERMAL MANAGEMENT
Wook Kim, Samsung Electronics, Hwasung, South Korea

THERMAL-AWARE SOC FLOORPLANNING METHOD BASED ON A CUSTOMIZED DEEP-Q NETWORK ALGORITHM
Taekeun An, Samsung Electronics, Hwasung, South Korea

SIGNAL INTEGRITY AWARE HBM3 6.4GBPS INTERFACE CHANNEL OPTIMIZATION
Tae Yun Kim, Soo Hyang Jeon, Chan Min Jo, Sung Wook Moon, Samsung Electronics, Hwaseong, South Korea

OPTICAL AND THERMAL SIMULATIONS FOR INTEGRATED III-V/SI HETEROGENEOUS LASERS ON SILICON PHOTONICS SYSTEM
Stanley Cheung, Raymond Beausoleil, Hewlett Packard Enterprise, Milpitas, CA; Antoine Descos, Di Liang, Hewlett Packard Enterprise, Santa Barbara, CA; James Pond, Karthik Srinivasan, Stephen Pan, Norman Chang, Ansys, Vancouver, Canada

SYSTEMATIC GENERATION AND REFRESH OF STANDARD CELL ABUTMENT DATABASE
Anuradha Ray, Veny Mahajan, STMicroelectronics, Noida, India

SILICON DEBUGGING USING FUNCTION FAILURE ORIENTED PATH DELAY FAULT VECTORS
Keunsoo Lee, Jaehyeon Kang, Sungmin Oh, Yun Heo, Ilryong Kim, Samsung Electronics, Hwaseong, South Korea; Khader Abdel-Hafez, Girish Patankar, Ruifeng Guo, Synopsys, Mountain View, CA; Tae-Jin Jung, Synopsys, YongJoon Kim, Synopsys, Hwaseong

INNOVATIVE SOLUTIONS FOR SIMULATION AND REGISTERS

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Topic Area(s): Front-End Design

In this session, you will learn a variety of innovative automation techniques for test/debug, verification and validation of SoC designs.

MACHINE LEARNING BASED EFFICIENT REGRESSION TEST FRAMEWORK IN SOC VERIFICATION
Jicheon Kim, Daewoo Kim, Seonil B. Choi, Samsung Electronics, Hwaseong-si, South Korea

DIMM LEVEL VERIFICATION METHODOLOGY FOR DRAM CUSTOM DFT
SeaEun Park, ByeongJun Bae, SeoHa Yang, IJae Kim, YounSik Park,JungYun Choi, Samsung Electronics, Hwaseong-Si, South Korea

GET MORE OUT OF YOUR UVM REGISTER LAYER!
Pavan Yeluri, Ranjith Nair, NVIDIA, Hyderabad, India

UNIFIED FW/ASIC CO-SIMULATION FOR EARLIER AND ACCELERATED PRE-SILICON TESTING
Elliot Gin, Joshua Loo, Kiel Boyle, Scott Nelson, Kyle Balston, Intel Corporation, Vancouver, Canada; Anthony Cabrera, Intel Corporation, Folsom, CA

NOVEL END TO END NON-COHERENT ACCESS MECHANISM ON X86 SOC
Manoj Kumar Munigala, N. Madhusudhan, Surinder Sood, Harshal Mumaikar, Intel Technology India Pvt. Ltd., Bengaluru, India

IS YOUR PRODUCT SECURE? - AN IP DRIVEN APPROACH TO PRODUCT SECURITY

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Topic Area(s): IP

SMART DIGITAL SENSORS AGAINST TAMPERING
Sylvain Guilley, Michel Le Rolland, Secure-IC, Rennes, France

HIGH BANDWIDTH ALL-DIGITAL CLOCK AND DATA RECOVERY ARCHITECTURE
Ankur Bal, Rupesh Singh, STMicroelectronics, Greater Noida, India

COMPREHENSIVE PROCESSOR SECURITY VERIFICATION: A CIA PROBLEM
Ashish Darbari, Axiomise, London, United Kingdom

PUF-BASED HROT FOR SUPPLY CHAIN SECURITY
Evans Yang, Meng-Yi Wu, Lawrence C. Liu, PUFsecurity, Jhubei, Taiwan

NEW FRONTIERS IN FORMAL AND STATIC VERIFICATION

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Topic Area(s): Front-End Design

In this essential session, there will be talks that focus on new explorations of formal techniques and tools by industry giants and research lab. A new approach to use formal analysis to ensure automotive SoC's adhere to safety standards will be presented. Other presentations focus on architectural analysis, design partitioning and completeness for formal sign-off. Finally, a couple of presentations focus on static verification techniques for reset/power domains and constraint based clock-domain crossing sign-off that circumvent error-prone waiver mechanism.

ARCHITECTURAL FORMAL SIGN-OFF OF COMPRESSION SYSTEM DATA COHERENCY
Anuj K. More, Sanjay Bishnoi, Dhruv Gupta, Oski Technology, Gurugram, India; David K. Cassetti, Intel Corporation, Tempe, AZ; Bhushan G. Parikh, Mark A. Yarch, Intel Corporation, Chandler, AZ

OVERLAPPING CHECKERS – A BETTER SUBSTITUTE OF END-TO-END CHECKERS
Sumit Kumar Kulshreshtha, Intel Technology India Pvt. Ltd., Bengaluru India

VERIFYING RESET AND POWER DOMAINS TOGETHER
Manjunatha Srinivas, Abdul Moyeen, Manish Bhati, Siemens EDA, Bangalore, India; Inayat Ali, NXP Semiconductors Inc., Noida, India

NOVEL METHODS FOR CLOCKING AND FUNCTIONAL SAFETY

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Topic Area(s): Front-End Design

Clocking continues to be an important aspect of chip development, end to end functional safety is increasingly becoming more important. This session explores novel methods in both of these important aspects of chip design.

PRACTICAL METHOD FOR CLOCK DOMAIN CROSSING USING SIMULATION-BASED PATH EXTRACTION

YoungRok Choi, Hyungjung Seo, So-Jung Park, ByongWook Na, Younsik Park, Jung Yun Choi, Samsung Electronics, Hwaseong-si, South Korea

A NOVEL CLOCK GATING DESIGN AND VERIFICATION METHODOLOGY TO ENSURE SAFE POWER OPTIMIZATION

Hao Chen, Ang Li, Suhas Prahalada, Howard Yang, Miguel Gomez-Garcia, Jonathan E. Schmidt, Leo Sporn, Intel Corporation, Vancouver, Canada

AUTOMATIC CLOCK GATING AND CLOSED-LOOP DVFS FOR 4NM EXYNOS MOBILE SOC PROCESSOR

Jae-Gon Lee, Wookyeong Jeong, Jaeyoung Lee, Byung Su Kim, Se Hun Kim, Young Duk Kim, Youngsan Kim,Yonghwan Kim, Sung Hoon (Ryan) Shim, Byeongho Lee, Jong-Jin Lee, Hoyeon Jeon, Younsik Choi, Joonseok Kim, Samsung Electronics, Hwaseong-si, South Korea

ACCELERATING MUTATION COVERAGE MEASUREMENT BY USING CONCURRENT FAULT SIMULATOR

Kota Sakai, Kenichi Otsuka, Fumitaka Fukuzawa, Shintaro Imamura, Renesas Electronics Corporation, Tokyo, Japan

ANALOG FAULT SIMULATION FOR AUTOMOTIVE SENSOR DESIGNS

Soohyun Kim, Yun Heo, Seokyong Park, Seongyeop Park, Ilryong Kim, Samsung, Hwaseong, South Korea; Sungjin Park, Kwangsoo Seo, Synopsys, Sungnam, South Korea

EFFICIENT DATA EXCHANGE TOWARDS FASTER FUNCTIONAL SAFETY DEVELOPMENT

Shivakumar Chonnad, Synopsys, Mountain View, CA; Vladimir Litovtchenko, Synopsys, Aschheim/Dornach, Germany

PCI EXPRESS SPECIFICATIONS: ENABLING EMERGING APPLICATIONS OF TODAY AND TOMORROW

PERFORMANCE, AGING, RELIABILITY – KEY ANALYSES

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Topic Area(s): Back-End Design

EFFICIENT SYSTEM PDN ANALYSIS METHODAT PRE-LAYOUT STAGE

Seungki Nam,Jungil Son, Jeewon Kwon, Sumant Srikant, Haemin Lee, Sungwook Moon, Samsung Electronics, Hawsung, South Korea

AGING AWARE STATIC TIMING ANALYSIS

Sangwoo Han, Samsung Electronics, Hwaseong-si, South Korea; Chirayu Amin, Cadence Design Systems, Inc., Hillsboro, OR

MACHINE LEARNING BASED IR DROP PREDICTION ON ECO REVISED DESIGNS FOR FASTER CONVERGENCE

Sashank Nishad, Santanu Kundu, Manoranjan Prasad, Intel Technology India Pvt. Ltd., Bengaluru, India

SIMULTANEOUS DESIGN METHODOLOGY OF HIGH SPEED & HIGH DENSITY CELL LIBRARIES USING TWO DIFFERENT ROWS IN SINGLE DESIGN

Dayeon Cho, SungOk Lee, Sangdo Park, Hyung-Ock Kim, Sungyoul Seo,Ingeol Lee, Sangyun Kim, Samsung Electronics, Hwaseong-si, South Korea

SOLIDIFYING YOUR SOC BEYOND DESIGN

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Topic Area(s): IP

Does a solid design in itself guarantee solid end product? With SOC Design methodologies well understood, often times teams face challenges in terms of having robust Silicon due to power/performance, test coverage and reliability related issues. In this session, experts will talk about some of the key factors that can be considered during design phase of the Chip to solidify the Silicon. We will look at techniques used by some of the experienced engineers to improve effects of aging and reduce variability challenges, ways to improve power and performance of your designs and key considerations while integrating Mixed-Signal IPs.

INPUT QUALIFICATION METHODOLOGY HELPS ACHIEVE SYSTEM LEVEL POWER NUMBERS 8X FASTER

Mohammed Fahad, Siemens EDA, Noida, India; Rohit Komatineni, Arm Ltd., Austin, TX; Richard Langridge, Siemens EDA, Newbury, United Kingdom; John Reed, Siemens EDA, Austin, TX

STRATEGY FOR MIXED SIGNAL IP INTEGRATION TO ACCELERATE HIGH-QUALITY SOC DEVELOPMENT

Gaurav Kumar Varshney, Shruti Kasetty, Texas Instruments, Bangalore, India

DIAGNOSTIC COVERAGE OF MEMORY IP WITH FAULT INJECTION SIMULATION USING TESTMAX CUSTOMFAULT SIMULATOR

Kedar Janardan Dhori, Atul Bhargava, STMicroelectronics, Greater Noida, India; Rakesh Panemangalore Shenoy, Synopsys, Noida, India

SOLVING POWER CHALLENGES AT THE FRONT END

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Topic Area(s): Front-End Design

This session covers various low power design techniques and power reduction methodologies to achieve most optimal power budgets. In this session, audience will learn about recent innovations in low power domain related to coverage mechanism, workload management and advancement in the field of power and performance.

SCORING VECTORS FOR IR SIGN-OFF USING POWER-WEIGHTED COVERAGE METRICS

Huei-Shan Lin, MediaTek Inc., Hsinchu, Taiwan; Arti Dwivedi, Ansys, San Jose, CA

DESIGNING IP TO ACHIEVE OPTIMAL LOW POWER USING PROTOCOL DEFINED LOW POWER STATES

Saleem Mohammad, Venkataraghavan Krishnan, Shivakumar Chonnad, Synopsys, Mountain View, CA

POWER MINIMIZATION FOR PEAK POWER AND IMPROVED GPU SUSTAINABILITY

Saurabh Shrimal, Qualcomm, Noida, India Jiaze Li, Qualcomm, Santa-Clara, CA; Yadong Wang, Bagus Wibowo, Qualcomm, San Diego, CA

POWER MINIMIZATION OF MCM/2.5D CHIP-2-CHIP COMMUNICATION INTERFACE

Muhammad waqas Chaudhary, Fraunhofer Institute for Integrated Circuits IIS, Dresden, Germany

WOW: APPROXIMATE WORKLOAD WATCHER

Junghwan Oh, Sunwook Kim, Manhwee Jo, Wooil Kim, Samsung Electronics, Hwaseong, South Korea

A COMPREHENSIVE UPF COVERAGE METHODOLOGY TO AVOID LATE SI ISSUES

Rohit Sinha, Intel Corporation, Bangalore, India

TUNE IN TO THE CLOCKS!

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Topic Area(s): Back-End Design
Clock design continues to be an important aspect of the overall chip design. In this session, you would come across some novel techniques used to resolve challenges in clock design during chip development.

OPTIMAL FUNCTION CLOCK AWARE SCAN METHODOLOGY
Chen Yuan Kao, Min Hsiu Tsai, Global Unichip Corp., Hsinchu, Taiwan

ACCURATE GLITCH NOISE ANALYSIS CONSIDERING IMPACT OF SECONDARY AGGRESSORS
Hyungoo Kim, Samsung Electronics, Yongin, South Korea

ON-CHIP DYNAMIC IR DROP INDUCED DETERMINISTIC JITTER ANALYSIS
Dongchul Kim, Samsung Electronics, Hwaseong-si, South Korea

AUTONOMOUS ROBOT DESIGN: HOW CAN EDA HELP?

Organizer: Iris Bahar, Brown University

Moderator: Iris Bahar, Brown University

Panelists: Hadas Kress-Gazit Cornell University; Sonia Chernova, Georgia Tech; Sabrina Neuman, Harvard University; Shaoshan Liu, Perceptin

QUANTUM COMPUTING: AN INDUSTRIAL PERPECTIVE

Organizer: Michael Niemier, Notre Dame

Moderator: Robert Wille, Johannes Kepler University Linz

Panelists: Leon Stok, IBM; Krysta Svore, Microsoft; Austin Fowler, Google

HOMOMORPHIC COMPUTING AS A FOUNDATIONAL TECHNOLOGY: THEORY, PRACTICE, AND FUTURE BUSINESS

Organizer: Yiorgos Makris, The University of Texas at Dallas

Moderator: Mihalis Maniatakos, New York University

Panelists: Kurt Rohloff, Duality; Kim Laine, Microsoft; Ingrid Verbauwhede, KU Leuven; Shafi Goldwasser, MIT

ENVIRONMENTALLY-SUSTAINABLE COMPUTING

Organizer: Carole-Jean Wu, Facebook & Arizona State U.

Moderator: Carole-Jean Wu

Panelists: Srilatha (Bobbie) Manne, Facebook; Karen Strauss, Microsoft; Fahmida Bangert, ITRenew; David Brooks, Harvard; Andrew Byrnes, Micron

MOVING TO EMBEDDED C++

Event Type: Training Day
Topic: Embedded Systems Design

Speaker: Eileen Hickey – Doulos, Longmont CO

As a language, C++ has been available for over 30 years, until recently its popularity has lagged its predecessor, C. Rapid growth in embedded system complexity has now offered engineers the opportunity to re-evaluate the value that object-oriented programming and access to a wide variety of reusable libraries that C++ brings to the table resulting in C++ now leading C in popularity among embedded systems programmers.

This track will help guide you through the process of switching to using C++ in your future designs rather than using pure C. It will look at the differences between the languages, features and pitfalls of converting existing code. It will also give an overview of Object- Oriented Design techniques and libraries that allow for more efficient embedded systems and quicker project completion.

Featured Topics:

- Comparison of C and C++, covering some of the C++ enhancements. Also including methods for mixing C++ with existing C code
- Introduction to Object Oriented Design. Hiding details and protecting data from inadvertent modification
- Letting the compiler do all the work. Language features for optimizing the output code for size and speed
- Standard libraries and pre-written code

THE PYTHON LANGUAGE: BECOME A PYTHONEER!

Event Type: Training Day
Topic: Machine Learning, Artificial Intelligence

Speaker: John Aynsley – Doulos, Ringwood, United Kingdom

This session will teach attendees the basics of the Python programming language. Python has become enormously popular as a programming language because it is compact, elegant, productive, readable, and extensible. People often remark that a Python program looks like pseudo-code, an English language description of what the code is meant to do. These attributes have led Python to be widely used as a general-purpose scripting language in EDA tool flows, for scientific computing and deep learning, for embedded software test, and even for digital hardware verification and system modeling.

People sometimes become very enthusiastic about Python because of its elegance as a programming language – so-called Pythoneers. This session is your chance to become a Pythoneer, and to learn about some of the cool things you can do with Python right out-of-the-box!

This track is taught by Doulos Co-founder and Technical Fellow John Aynsley, winner of the Accellera Systems Initiative 2012 Technical Excellence Award for his contribution to the development of language standards.

ANATOMY OF AN EMBEDDED LINUX SYSTEM & USER/KERNEL DEBUG

Event Type: Training Day
Topic: Embedded Systems Design

Speaker: Eileen Hickey – Doulos, Longmont CO

In this session we cover each of the components required for Linux to work on an embedded system (i.e. the Linux kernel, toolchain, bootloader, filesystem). We will review how each of these components fit into the system and what functionality they provide for development and in the final deployed product. We will review some of the choices that can be made, looking at what options there are for creating an integrated development environment for embedded Linux.

An essential part of the process for developing embedded Linux systems is debugging. Whether to remove bugs or verify the behavior of the system it is vital for developers to know how to debug their code running on a Linux target. We look closely at embedded Linux application & kernel debugging and review the different tools and methodologies available in a typical embedded Linux system.

Each of these presentations will be augmented with demos, providing the attendees a chance to see the actual mechanics and ask questions.

COLOCATED CONFERENCES

IWLS

OSFPGA

Thursday, December 9 | 12:00 pm - 5:00 pm | Room: 3007

SemiCon West 2021

December 7-9

SEMICON West 2021 combines the best of both worlds offering a hybrid event live at Moscone and online. Reunite with your peers, customers and suppliers to experience the latest technological progression from across the entire electronics supply chain from design, materials and equipment to manufacturing and system integration. Enjoy three jam-packed days of keynotes, executive panels, technical sessions, forums, exhibits and networking opportunities and see what's driving the latest innovation engines.

RISC-V Summit

December 6-8

RISC-V Summit brings the community together to show the power open collaboration can have on the processor industry. The audience spans across industries, organizations, workloads, and geographies to learn about the technology advancements in the RISC-V ecosystem and visibility of RISC-V successes.

ADDITIONAL MEETINGS

IEEE/CEDA

Board of Governors and Executive Committee

Sunday, December 5 | 8:00 am – 5:00 pm | Room: 3000

Accellera

Accellera Luncheon Panel (TOPIC TBD)

Monday, December 6 | 11:30 am – 1:00 pm | Speaker Breakfast Room: 3022 – 3024

Additional Information to come**

IEEE/CEDA

CEDA Distinguished Speaker Luncheon

Tuesday, December 7 | 12:00pm – 1:30pm | Speaker Breakfast Room: 3022 – 3024

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DESIGN-ON-CLOUD THEATER SCHEDULE

Booth 1258

Thank you to our Design-On-Cloud Theater Sponsor: fastone 速石科技

MONDAY, DECEMBER 6	
10:00 am	**Exhibit Hall Opens**
10:30 am –-11:15 am	**Cadence: How Cadence Cloud is Empowering Digital Transformation for Electronic Design** **Speaker:** Mahesh Turaga, Vice President Business Development, Cloud
11:30 am – 12:15 pm	**Shanghai FASTONE Information Technology Co. Ltd. (China): Improve R&D Efficiency Significantly and Systematically – Using a Turnkey IC Design Cloud Platform** **Speaker:** Xi Chen
12:30 pm – 1:15 pm	**Amazon Web Services: Cloud-Based Collaboration for Design, Verification, and Manufacturing** **Speaker:** David Pellerin, Head of WW Business Development, Semiconductor
2:30 pm – 3:15 pm	**Synopsys: Accelerating Cloud Adoption in EDA** **Speaker:** Teng-Kiat Lee and Sridhar Panchapakesan
3:30 pm – 4:15 pm	**Siemens: Siemens EDA Cloud Offerings** **Speaker:** Craig Johnson, VP EDA Cloud Solutions, Siemens EDA
6:00 pm	**Exhibit Hall Closes**
TUESDAY, DECEMBER 7	
10:00 am	**Exhibit Hall Opens**
10:30 am – 11:15 am	**Microsoft: EDA on the Cloud: Where we are today, Speaker: Preeth Chengappa** **Speaker:** Preet Chengappa
11:30 am – 12:15 pm	**Spillbox: Scaling EDA workloads across Cloud and Datacenter** **Speaker:** Alok Sinha, Rajeev K. Prasad, Jasmin Ajanovic
12:30 pm – 1:15 pm	**ARM, Ltd.: Experience Arm IP in the Cloud** **Speaker:** Bill Neifert and Jason Andrews
2:30 pm – 3:15 pm	**Chip Scan: Hardware Hackers!: Subvert, Sabotage and Compromise a "Victim's" Design (And Why ESPY Will Ruin Your Day)** **Speaker:** Calvin Chu, Chief Operating Officer
6:00 pm	**Exhibit Hall Closes**

Design-on-Cloud Presenters - Booth 1258

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Program information as of November 9. All session information subject to change. Please check the DAC mobile app for the most recent information.

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