DESIGN AUTOMATION CONFERENCE
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WWW.DAC.COM

SAN FRANCISCO
JUNE 3-7, 2012
MOSCONE CENTER

KEYNOTES

JUNE 5
Scaling for 2020 Solutions
Mike Muller
ARM, Inc.

JUNE 7
My First Design Automation Conference - 1982
C.L. Liu
National Tsing Hua Univ.

JUNE 6
Designing High Performance Systems-on-Chip

Joshua Friedrich
IBM Server and Technology Group
POWER™ Processor Design and Methodology Directions

Brad Heaney
Intel Corp.
Designing a 22nm Intel® Architecture Multi-CPU and GPU

TECHNICAL PROGRAM HIGHLIGHTS

- **168 Technical Papers**
- **10 Special Sessions**
- **9 Technical Panels**
- **8 Workshops**
- **8 Colocated Conferences**
- **35% of the program is dedicated to Embedded Systems and Software (ESS)**

TECHNICAL PANELS *TECHNOLOGY SMACKDOWN*

- Will Reliability be the Death of Moore's Law?
- System Models - Does One Size Fit All?
- Will Your Next ASIC Ever be an FPGA?
- High-Level Synthesis Production Deployment: Are We Ready?
- Is EDA in the Cloud Just Pie in the Sky?

- Hot Apps, Cool Phones: Power-Efficient Mobile Design
- Is 3-D Ready for the Next Level?
- Parallel Speedup: Hope, Hype, or Horror?
- It's the Software, Stupid! Truth or Myth?

UT USER TRACK Sponsored by: ANSYS Apache
80 POSTERS, 11 SESSIONS BY AND FOR USERS

EXHIBIT FLOOR — *200+ EXHIBITORS*

ALL OF DESIGN AUTOMATION & ESS UNDER ONE ROOF
DAC is the leading technical conference and tradeshow on electronic design, design automation, embedded systems and software. It is where IC Design and the EDA ecosystem learns, networks, and conducts business.

EXHIBITS FREE ON MONDAY
Monday - Wednesday 9:00am - 6:00pm
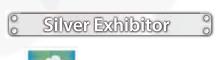
ARM® Connected Community® Pavilion

Platinum Exhibitor
cadence
SYNOPSYS

Gold Exhibitor
ANSYS Apache
GLOBALFOUNDRIES
Mentor Graphics

Silver Exhibitor
ATRENTA
SpringSoft *accelerating engineers*

15 PAVILION PANELS

ALL LOCATED ON THE EXHIBIT FLOOR
- Gary Smith on EDA: Trends and What's Hot at DAC
- Low Power to the People!
- Is "Lifecare" the Next Killer App?
- The Mechanics of Creativity
- Interview with Dr. Belle W. Y. Wei, 2012 Marie R. Pistilli Award Recipient
- Hogan's Heroes: Learning from Apple
- Chevy Volt Teardown: Automotive Electronics
- Conquering New Frontiers in Analog Design – Plunging Below 28nm
- Heritage Series: Interview with Jim Solomon, 1997 Phil Kaufman Award Recipient
- Real World Heterogeneous Multicore
- Town Hall: Dark Side of Moore's Law
- Foundry, EDA and IP: Solve Time-to-Market Already!
- Divide and Conquer – Intelligent Partitioning
- Hardware-Assisted Prototyping and Verification: Make vs. Buy?
- Teens Talk Tech

TUTORIALS *LEARN AT DAC, DESIGN TOMORROW*
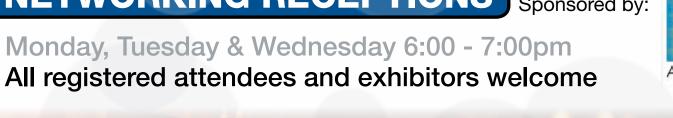
Monday, June 4
1. Synthesizing SystemC to Layout
2. Enough Talk! Practical Approaches to 3-D-IC, TSV, and Wide-IO Implementation from People who Have Been There and Done That
3. System-Level Exploration of Power, Temperature, Performance, and Area for Multicore Architectures
4. Understanding and Overcoming Patterning-Induced Design Challenges in the 20nm and 14nm Technology Nodes
5. Analog and Mixed-Signal Design at Advanced Process Node
6. Pre-Silicon, Native Embedded Software Development Solutions

MANAGEMENT DAY

THE EDGE OF BUSINESS AND TECHNOLOGY
Tuesday, June 5

The DAC 2012 Management Day provides managers with timely information to help them make decisions where business and technology intersect. This is a unique opportunity for managers to gain insights from their peers in the industry.

ESS EXECUTIVE DAY

Wednesday, June 6

Hardware and software design convergence and interdependence in today's complex embedded systems continue to increase. The ESS Executive Day provides attendees with timely information to help them make decisions where business and technology intersect. Presentations will focus on the state-of-the-art solutions for embedded software and systems and complex chips.

SUNDAY KICK-OFF RECEPTION
Sponsored by:

Sunday June 3, 6:00pm
Marriott Marquis

NETWORKING RECEPTIONS
Monday Sponsored by: ATRENTA

Monday, Tuesday & Wednesday 6:00 - 7:00pm
All registered attendees and exhibitors welcome

WORK-IN-PROGRESS (WIP)

Wednesday, June 6 @ 6:00 - 7:00pm
Esplanade Foyer
In contrast to other tracks at DAC, WIP aims to provide authors an opportunity for early feedback on their work and to share early results.

Sponsored by: sig da (acm), EDA CONSORTIUM, CEDA IEEE Council on Electronic Design Automation

In technical cooperation with: SSCS