CALL FOR CONTRIBUTIONS

DAC's technical program offers the best-in-class solutions that promise to advance Electronic Design Automation (EDA) and Embedded Systems and Software (ESS). DAC 2012 is seeking submissions that deal with design technologies and algorithms, addressing all aspects of electronic design across several submission categories.

Submission Categories: In addition to well established EDA and ESS subjects, special focus areas in 2012 include embedded software and architectures, multi-core, security, virtualization, energy harvesting, emerging devices, cloud computing, parallelization, 3-D, design for manufacturability, cyber-physical systems, bio interfaces, bio sensors, and bio design automation.

New SUBMISSION format in 2012: **Please note DAC's new submission procedures.** Authors are asked to submit their work in two stages. In stage one (Abstraction Submission), a title, abstract, and a list of all co-authors must be submitted at the DAC web submission website. In stage two (Manuscript Submission), the paper itself is submitted. Authors are responsible for ensuring that their manuscript submission meets all guidelines, and that the PDF is readable. To ensure fairness for all submitters, there will be no grace periods to fix problematic submission.

New RESEARCH MANUSCRIPT format in 2012: DAC encourages authors to submit in addition to the six pages self-contained manuscript up to four pages of supplemental material (similar in concept to appendices) that may include derivations, formal proofs, extensive experimental findings, commentary, traps for the wary, and/or detailed examples. The manuscript should stand on its own. Each section (numbered S1, S2, etc.) within the supplementary material should clarify or expand on a concept already discussed in the 6-page manuscript. The four pages are supplemental – for the benefit of the reader. Manuscripts without the supplementary material will not be penalized during the review process. Authors are responsible for ensuring that their manuscript meets the manuscript-length guidelines. There will be no resubmissions to correct this issue.

New DAC's FAQs: Consult our list of Frequently Asked Questions, for each type of submission area.

DAC invites **submissions** in the following categories:

- Electronic Design Automation (EDA) Research Manuscripts
- Embedded Systems and Software (ESS) Research Manuscripts
- "Perspectives" Manuscripts (new)
- "Work-in-Progress" (WIP) Abstracts
- "Wild and Crazy Ideas" (WACI) short manuscripts
- User Track Extended Abstracts
- Special Session Proposals
- Tutorial & Panel Proposals
- Workshop Proposals
- Colocated Conference Proposals

Electronic Design Automation (EDA) Research Manuscripts

ABSTRACT SUBMISSION: DUE BEFORE 5:00pm MT, (-7:00 GMT) November 29, 2011
MANUSCRIPT SUBMISSION: DUE BEFORE 5:00pm MT, (-7:00 GMT) December 5, 2011

All EDA research manuscript submissions MUST adhere to the following rules, and manuscripts that do not adhere to these rules will not be considered for any resubmission. Rules for submission:

1. **Submitter must enter the names, affiliations, city, state, country and email address of ALL co-authors**
2. Submissions uploaded in PDF format only
3. Contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission
4. The manuscript must not exceed ten pages (including the abstract, figures, tables, and references, supplemental material), double-columned, 9-pt or 10-pt font, and the manuscript must not exceed a total of ten pages including the manuscript and the supplementary material.
5. MUST NOT identify the author(s) by their name(s) or affiliation(s) anywhere on the manuscript or abstract, with all references to the author(s)'s own previous work or affiliations in the bibliographic citations being in the third person.
6. List all authors and their affiliations in the web-based submission form (i.e., not in the manuscript); **the addition of new authors will not be permitted at the time of manuscript submission, or to an accepted manuscript.**

DAC manuscripts go through a double-blind review process; i.e., the identity of authors and reviewers is only known to the TPC co-chairs. DAC ensures that there are no conflicts of interest between authors and reviewers. DAC will compare each submission against a vast database and any manuscript with significant similarity to previously published works or with manuscripts that are simultaneously under review with other venues with archival publications (e.g., conferences, symposia, journals, and workshops with archival proceedings). Duplicate submissions will be rejected. Furthermore, DAC will notify the technical chair of the venue where the duplicate was submitted.

Format templates are available on the DAC website. All EDA research manuscripts will be reviewed as finished manuscripts. Preliminary submissions will be at a disadvantage. A listing of titles of all accepted manuscripts will be posted on the DAC web site on February 10, 2012. Accept/reject notices will be sent to all authors by email on February 20, 2012, and will be available thereafter to all authors by logging into the DAC website after Feb. 10, 2012. Complete instructions for final manuscript submission and required release forms will be available on the DAC website by March 6, 2012. Authors of accepted manuscripts must sign and submit a copyright release form for their manuscript. All conference presenters will be required to register at the time of final manuscript submission, present their manuscript and participate in an EDA research poster session.

ACM and IEEE reserve the right to exclude a manuscript from archival distribution after the conference if the manuscript is not presented by one of the co-authors at the conference, or in other exceptional cases. DAC will support the IEEE Prohibited Authors List.

Select authors of submitted DAC manuscripts that are not accepted for publication in 2012 will be invited in mid-February 2012 to participate in "Work-In-Progress" (WIP) poster sessions. They will be asked to submit a 100 word abstract to publish on the website (and not in the proceedings). Authors will also be given the option to post their poster presentation on dac.com.

SUBMISSION CATEGORIES FOR EDA RESEARCH MANUSCRIPTS

Authors of EDA research manuscripts are required to specify a category from the list below. Authors of submissions that cover cross-cutting topics (e.g. low-power, reliability, 3-D, etc.) should select a category that is closest to the essential contribution of the submission. Authors may choose a second submission category to accommodate cross-cutting contributions. Please note the separate categories for embedded systems and software topics.

EDA1. System-Level Design & Codesign
EDA1.1 System specification, modeling, simulation, verification, and performance analysis
EDA1.2 Scheduling, HW/SW partitioning, HW/SW interface synthesis
EDA1.3 IP and platform-based design
EDA1.4 Security and IP protection
EDA1.5 Design of Multiprocessor System-On-Chip (MPSOC)
EDA1.6 Application-specific processor design tools

EDA2. System-Level Communication and Networks-on-Chip
EDA2.1 Modeling and performance analysis
EDA2.2 Communications-based design, communication and network synthesis
EDA2.3 Optimization for energy, fault tolerance, reliability
EDA2.4 Interfacing and software issues, beyond-the-die communication
EDA2.5 NoC design methodologies, case studies and prototyping

EDA3. Power Analysis and Low-Power Design
EDA3.1 System-level power design and thermal management
EDA3.2 System/Architectural low-power techniques: partitioning, scheduling, and resource management
EDA3.3 High-level power estimation and optimization
EDA3.4 Gate-level power analysis and optimization
EDA3.5 Device and circuit techniques for low-power design
EDA3.6 Power-aware and energy-efficient wireless protocols, algorithms and design techniques

EDA4. Verification
EDA4.1 Functional, transaction-level, RTL, and gate-level modeling and verification of hardware design
EDA4.2 Dynamic simulation, equivalence checking, formal (and semiformal) verification model and property checking
EDA4.3 Emulation and hardware simulators or accelerator engines
EDA4.4 Modeling languages and related formalisms, verification plan development and implementation
EDA4.5 Assertion-based verification, coverage analysis, constrained random testbench generation

EDA5. High-Level Synthesis, Logic Synthesis, and FPGAs
EDA5.1 Combinational, sequential and asynchronous logic synthesis
EDA5.2 Library mapping, cell-based design and optimization
EDA5.3 Transistor and gate sizing, resynthesis
EDA5.4 Interactions between logic design and layout or physical synthesis
EDA5.5 High-level, behavioral, algorithmic, and architectural synthesis, “C” to gates tools and methods
EDA5.6 Resource scheduling, allocation, and synthesis
EDA5.7 Logic synthesis and physical design techniques for FPGAs
EDA5.8 Configurable and reconfigurable computing

EDA6. Circuit, Interconnect and Manufacturing Simulation and Analysis
EDA6.1 Electrical, thermal, and electro-thermal simulation
EDA6.2 Model order reduction methods
EDA6.3 Interconnect and substrate modeling and extraction
EDA6.4 High-frequency and electromagnetic simulation of circuits
EDA6.5 Process technology characterization, and modeling
EDA6.6 Technology CAD and fab automation

EDA7. Timing Analysis, Integrity and Design Reliability
EDA7.1 Deterministic and statistical timing analysis
EDA7.2 Signal integrity and substrate noise
EDA7.3 Power delivery analysis and optimization

EDA7.4 Electrical and thermal reliability
EDA7.5 Soft errors
EDA7.6 Novel clocking methodologies

EDA8. Physical Design
EDA8.1 Floorplanning, partitioning, placement
EDA8.2 Buffer insertion, routing, interconnect planning
EDA8.3 Physical verification and design rule checking
EDA8.4 Automated synthesis of clock networks
EDA8.5 Physical design of 3-D integrated circuits
EDA8.6System-in-package design, package-board codesign

EDA9. Design for Manufacturability
EDA9.1 Reticle enhancement, lithography-related design optimizations
EDA9.2 Design for manufacturability, yield, defect tolerance, cost issues, and DFM impact
EDA9.3 Design for resilience under manufacturing variations

EDA10. Analog, Mixed-Signal, and RF
EDA10.1 Analog, mixed-signal, and RF design methodologies
EDA10.2 Automated synthesis
EDA10.3 Analog, mixed-signal, and RF simulation
EDA10.4 High-frequency design and advanced antenna design for wireless design

EDA11. Testing
EDA11.1 Test quality/reliability, current based test, delay test, low-power test
EDA11.2 Digital fault modeling, automatic test generation, fault simulation
EDA11.3 Digital design for test, test data compression, built-in self test
EDA11.4 Memory test and repair, FPGA testing
EDA11.5 Fault-tolerance and online testing
EDA11.6 Analog/mixed-signal/RF testing, system-in-package (SIP) testing
EDA11.7 Board- and system-level test, system-on-chip (SOC) testing
EDA11.8 Silicon debug and diagnosis, post-silicon design validation

EDA12. Design Automation for System & Synthetic Biology
EDA12.1 Design methodologies for system & synthetic biology
EDA12.2 Tools for engineering parts and devices
EDA12.3 Tools for protein and pathway engineering
EDA12.4 Tools for bridging experimental and computational frameworks

EDA13. New and Emerging Design Technologies (including but not restricted to)
EDA13.1 New transistor structures, devices, and novel process technologies
EDA13.2 Nanotechnologies, nanowires, nanotubes
EDA13.3 Optical devices and communication
EDA13.4 Quantum computing
EDA13.5 Biologically-based or biologically-inspired computing systems
EDA13.6 MEMS, sensors, actuators, imaging devices
EDA13.7 Cyber-physical systems

EDA14 EDA Wild and Crazy Ideas (WACI)

Embedded Systems and Software (ESS) Research Manuscripts

ABSTRACT SUBMISSION: DUE BEFORE 5:00pm MT, (-7:00 GMT) November 29, 2011
MANUSCRIPT SUBMISSION: DUE BEFORE 5:00pm MT, (-7:00 GMT) December 5, 2011

The ESS Track at DAC 2011 was a huge hit, resulting in more than 33% of the conference's technical content focused on ESS. Authors of research manuscripts on all aspects of Embedded Systems and Software are encouraged to submit from the topic category from the list below. Authors may choose a second submission category (both from the EDA research topics as well as from the focus embedded topics) to accommodate cross-cutting contributions. All Embedded Systems and Software manuscript submissions must adhere to the same rules outlined for the EDA research manuscripts.

Select authors of submitted DAC Embedded Systems and Software manuscripts that are not accepted for publication in 2012 will be invited in mid-February 2012 to participate in "Work-In-Progress" (WIP) poster sessions. They will be asked to submit a 100-word summary to publish on the website (and not in the proceedings). Authors will also be given the option to post their poster presentation on dac.com.

ESS1. Embedded System Specification and Software Engineering
ESS1.1 Domain-specific programming languages
ESS1.2 Software architectures and software engineering
ESS1.3 Model- and component-based embedded software design
ESS1.4 Software frameworks
ESS1.5 Hardware/software co-specification techniques

ESS2. Embedded Software
ESS2.1 Real-time operating systems and middleware
ESS2.2 Middleware and virtual machines
ESS2.3 OS Runtime support for resources management
ESS2.4 Software techniques for multicore, GPU, multithreaded embedded architectures
ESS2.5 Compilation strategies, code transformation and parallelization techniques for embedded systems
ESS2.6 Static and dynamic timing analysis for embedded systems
ESS2.7 Hardware-dependent software
ESS2.8 Customized interfaces and protocols
ESS2.9 I/O management in embedded systems: device drivers, timers, etc.

ESS3. Architectures for Embedded Systems
ESS3.1 Many- and multi-core embedded architectures
ESS3.2 Application-specific platforms and embedded processors (ASIP) design
ESS3.3. Design of heterogeneous distributed embedded systems including wireless sensor networks
ESS3.4 Run-time and design time reconfigurable platforms and processors
ESS3.5 Architectures for self-adaptive computing systems
ESS3.6 On-chip memory architectures and management: scratchpads, compiler controlled memories, etc.
ESS3.7 Custom storage organizations: flash, etc.
ESS3.8 Custom communication design

ESS4. Embedded System Validation, Verification, Security, Dependability
ESS4.1 Formal verification
ESS4.2 System validation
ESS4.3 Testing and regression analysis
ESS4.4 Hardware/software co-validation
ESS4.5 Hardware and software security and dependability techniques
ESS4.6 Verification techniques for software correctness

ESS5. Embedded Systems Platforms and Case Studies
ESS5.1 Platforms and design flows for domain-specific applications (e.g., avionics, automotive, medical, mobile, multimedia, etc.)

ESS5.2 IP-based design
ESS5.3 Rapid prototyping
ESS5.4 Packaging issues
ESS5.5 Case studies

ESS6. Embedded systems design methodologies
ESS6.1 Modeling embedded constraints: performance, reliability, power, security, etc.
ESS6.2 Early estimation and co-simulation of embedded systems designs
ESS6.3 Multiple-constraint-driven embedded system design exploration, synthesis and optimization
ESS6.4 Design methodologies for pervasive distributed networked embedded systems
ESS6.5 Design methodologies for runtime reconfiguration management, self-adaptive systems and autonomous embedded systems
ESS6.6 System level power management and optimization in embedded systems

ESS7. Embedded Systems and Software (ESS) Wild and Crazy Ideas (WACI)

PERSPECTIVES MANUSCRIPT SUBMISSION

ABSTRACT SUBMISSION: DUE BEFORE 5:00pm MT, (-7:00 GMT) November 29, 2011
MANUSCRIPT SUBMISSION: DUE BEFORE 5:00pm MT, (-7:00 GMT) December 5, 2011

This year, DAC will be soliciting a new class of manuscripts that do not necessarily require original research content. The purpose of this category is to provide a forum for valuable, but non-traditional content for the DAC program. Submissions in this category are limited to 8 pages in length and will undergo a thorough review process in the appropriate technical subcommittee, and integrated within the technical sessions. Accepted manuscripts will be published in the proceedings. Authors must specify their submission as a "Perspective" submission during the ABSTRACT SUBMISSION stage.

Examples for submissions in this category include, but are not limited to:
* Surveys or historical perspectives on an important problem
* New problem formulations and benchmarks
* Critiques of a current subset of CAD literature (e.g., parallel CAD, floorplanning,..)
* Descriptions of new, yet relatively unexplored CAD problems
* Commentary on keynote or plenary talks from other EDA conferences that have not been published
* Visualization of complex design or algorithmic data
* New design / algorithm quality metrics or quantification methods
* Applications of EDA algorithms to non-traditional EDA applications
* Detailed comparisons and analysis of previously published approaches to better quantify value
* Position manuscripts that present opinions on important problems and how it can be attacked

"WORK-IN-PROGRESS" (WIP) ABSTRACTS

SUBMISSION DUE BEFORE 5:00pm MT, (-7:00 GMT) March 12, 2012
Authors are invited to submit a one-page abstract.

In contrast to other tracks at DAC, this track aims to provide authors an opportunity for early feedback on work-in-progress or to share early results. A WIP submission must be one page in length, in PDF format, and clearly specify a technical problem, outline a solution, and provide some early results. WIP submissions will be accepted for presentation at a poster session. A WIP submission will not be included in the DAC proceedings. The 100-word summary abstract will be published on the website. A WIP presentation at DAC is not considered a DAC publication. WIP submissions will be reviewed by the Technical Program Committee and expert external reviewers, but no specific

feedback will be provided. Acceptance notices will be available by logging in to the DAC website after April 16, 2012. The 100-word summary abstract will be placed on the dac.com website once the submission is accepted. WIP authors are at liberty to submit an extended version of their work to other conferences and to journals without violating common codes of ethics.

Some authors of submitted DAC research and embedded systems and software manuscripts that are not accepted for publication in 2012 will be given "WIP pre-selected" status. These authors will be invited in mid-February 2012 to participate in the WIP poster sessions. The authors will be asked to submit a 100-word summary abstract to be published on the website (and not in the proceedings). WIP submissions received by the WIP deadline are expected to be competitive with the WIP pre-selected submissions. The number of planned poster sessions will be commensurate with the quality of WIP submissions.

USER TRACK EXTENDED ABSTRACTS

ABSTRACT SUBMISSION DUE BEFORE 5:00pm MT, (-7:00 GMT) January 17, 2012

The User Track addresses practical and pressing issues facing IC designers, application engineers, and design-flow developers. Contributions provide insights and experiences with in-house and commercial EDA tool flows. User Track submissions may describe the application of EDA tools to the design of a novel electronic system, or the integration of EDA tools within a design flow or methodology to produce such systems. A User Track submission may be problem-specific in scope (e.g., analysing substrate coupling during floorplanning) or may address a specific application domain (e.g., designing wireless handsets).

The User Track has two components: a presentation track that runs parallel to other DAC tracks, and a poster track. User Track presentations and posters are not included in the DAC proceedings. However, User Track material will be posted on the DAC website after the conference.

A Best Presentation award will be selected from the User Track accepted submissions. The award will be based on both the quality of the submission and the DAC presentation itself. The award will be presented prior to the Thursday Keynote.

To spare authors the many hours of preparation associated with a regular manuscript submission, User Track submissions are in the form of a two-page extended abstract. Authors of accepted submissions will be invited to present a poster during a User Track poster session. Authors of particularly high-quality submissions will be invited to submit their work in the form of a slide presentation for a second review round. Authors of successful second-round submissions will be invited to present their work orally during a User Track session.

SUBMISSION DETAILS

An extended abstract is expected to include the following details:

1) A title
2) Name, affiliation, phone number and email addresses for all authors. Authors may NOT be added after the confirmation forms are returned (once the abstract is selected), so be sure to list all authors in the initial submission.
3) An introduction that specifies the context and motivation of the submission. Examples: identify challenges associated with the task accomplishing with the tools; clarify where in the design process the tools are used; explain why the problem addressed is of interest to the audience.
4) A summary of the specific contributions of your work. Examples: innovative use of tools to achieve a specific goal; user enhancements to the tool or the tool flow; dealing with scalability; details of integrating IP; study of design trade-offs; interfacing with manufacturing.

5) A summary that highlights results. Results are needed to evaluate the impact of your contribution. Metrics that could be used include productivity enhancement, improved quality of silicon, decreased complexity, and reduced time-to-market.

6) Citations, if appropriate

Extended abstracts are limited to two pages. Up to two additional pages of references, diagrams, and figures may be included as you deem appropriate.

Submissions must be in PDF and can be formatted as single or double column. Enough detail must be provided for the Technical Program Committee to evaluate the potential quality and interest of a poster or presentation at DAC. A one or two-paragraph summary will not fulfil this requirement.

USER TRACK SUBMISSION CATEGORIES

User Track authors must specify one of the three primary categories from the list below.

U1. Embedded Systems and Software

Architectural exploration, design and optimization
Software specification, models and frameworks
Security for embedded systems and software
Validation and verification
Design methodologies and flows
Case studies

U2. Silicon Design (Front-End)

System and high-level hardware synthesis
Power/area/performance trade-offs and low-power design
Bus and network communication
Logic simulation
Validation, test planning, and coverage
FPGAs and emulation
Formal verification

U3. Silicon Design (Back-End)

Physical synthesis tools and techniques
Floor planning
Timing and circuit analysis; circuit optimization
Reliability
Interconnect simulation and analysis
Physical design and manufacturability
Manufacturing test and silicon debug
Analog, mixed-signal, and RF design
Custom, standard cell, and FPGA design flows
Tool control and integration

WILD AND CRAZY IDEAS (WACI) MANUSCRIPTS

ABSTRACT SUBMISSION: DUE BEFORE 5:00pm MT, (-7:00 GMT) November 29, 2011
MANUSCRIPT SUBMISSION: DUE BEFORE 5:00pm MT, (-7:00 GMT) December 5, 2011
DAC invites submissions with genuinely forward-looking, radical, and innovative ideas in the area of electronic design or electronic design automation. The WACI sessions feature novel (and even preliminary or unproven) technical ideas. The aim of WACI is to promote revolutionary and way-out ideas that do not fit the conventional mold, that inspire discussion among conference attendees, that create a buzz, and that get people talking. Research that incrementally improves on prior work is not suited for this category.

Submissions to the “Wild and Crazy Ideas” track must not exceed a total of two pages, but must otherwise follow the above rules and deadlines for the research manuscripts. Unlike a DAC research manuscript that explores a specific technology problem and proposes a complete solution to it, with extensive experimental results, a WACI manuscript could present less developed but highly innovative ideas related to areas relevant to DAC. All WACI accepted manuscripts will be required to post a two-minute video describing the work as part of the acceptance process. DAC 2010 WACI videos may be seen at http://www.dac.com/47th+dac+videos+waci+videos.aspx

SPECIAL SESSION PROPOSALS

SUBMISSIONS DUE BEFORE 5:00pm MT, (-7:00 GMT) November 2, 2011
A special session is devoted to a topic of strong contemporary or future interest. The topic must represent an emerging area that does not yet receive sufficient focus from research manuscripts. A submission must list at least three inspiring speakers who address the topic from different angles. Special session proposals must include descriptions of the proposed manuscripts and speakers, and the importance of the special session to the DAC audience. DAC reserves the right to restructure all special session proposals. For early feedback on a proposal topic, please contact the Technical Program Co-Chairs.

PANEL PROPOSALS

SUBMISSIONS DUE BEFORE 5:00pm MT, (-7:00 GMT) November 2, 2011
The panel topic should be interesting, timely, informative, and enlightening. The topic should be relevant to one or more segments of DAC attendees. A good panel session explores a single, high-level issue or question and has representatives of differing viewpoints. Panel suggestions may include anything that might appeal to the DAC community. DAC is encouraging traditional topics in EDA; for example, DFM, Verification and Physical Design. Special focus areas in 2012 include embedded software and architectures, multi-core, security, virtualization, energy harvesting, emerging devices, cloud computing, parallelization, 3-D, design for manufacturability, cyber-physical systems.

DAC reserves the right to restructure all panel suggestions.

TUTORIAL PROPOSALS

SUBMISSIONS DUE BEFORE 5:00pm MT, (-7:00 GMT) November 2, 2011

In 2012, DAC tutorials will be scheduled as **two-hour, short tutorials** presented multiple times on tutorial day such that attendees can cover three topics of their choice. The preferred structure for a tutorial is to have a single speaker for a given session.

DAC is looking for tangible, hands-on topics that provide immediate value for the attendee. The areas can cover:

- Traditional EDA topics (for example “How to architect a parallel timing analyzer”)
- Hot design topics (for example “How to design a low-power memory controller”)
- Emerging software development topics (for example “How to get started on writing iPhone apps”)

COLOCATED CONFERENCE PROPOSALS

SUBMISSIONS DUE BEFORE 5:00pm MT, (-7:00 GMT) December 2, 2011

Join Us and Colocate Your Event at DAC!

DAC Colocated Conferences are meetings that have already obtained event sponsorship from IEEE, ACM, the EDA Consortium or another organization. DAC invites you to colocate your conference with DAC, whether it is a conference, meeting or some other special event. Colocated Conferences must have a common sponsor with DAC, such as IEEE CEDA, ACM/SIGDA, or EDAC, be at least four hours long and have goals synergistic with those of DAC. Additionally, your conference/event must be financed and organized by you, have its own banking account to pay invoices and cover additional expenses.

WORKSHOP PROPOSALS

SUBMISSIONS DUE BEFORE 5:00pm MT, (-7:00 GMT) January 19, 2012

DAC invites you to organize a workshop on topics related to design, design methodologies, and design automation. DAC workshops are considered a central part of DAC’s technical program and span anywhere from two to nine hours. A workshop organizer is responsible for developing the agenda, selecting, inviting and confirming the speakers, and communicating the workshop details to the DAC office. DAC’s responsibility includes the financial management, setting registration fees, coordinating the logistics of the event and publicity.