#61DAC

61 THE CHIPS TO SYSTEMS CONFERENCE

SHAPING THE NEXT GENERATION OF ELECTRONICS

JUNE 23-27, 2024

MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA

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DEAR COLLEAGUES AND FRIENDS,

Welcome to 61st DAC – the "Chips to Systems Conference"!

DAC turned 60 last year. and we had a major celebration of its rich and long history as being the premier global research conference and industry event in electronic design and design automation. While EDA still remains at the core of DAC, we have seen some expansion in the topics of interest. Besides the traditional topics of EDA design, IP and Embedded Systems, we now have three additional topics -- AI, Autonmous Systems and Security.

The number of submissions in AI – both AI for chip design and AI hardware design and architecture – have literally exploded over the last few years and there seems to be no end in sight. AI is now 13% of the program and growing rapidly. We are embracing this expansion of DAC topic areas. Yes, still EDA at heart – but we're now featuring a much broader set of offerings for researchers and practitioners across industry and academia. As the premier global event for chips to systems, DAC is now very well-positioned to serve the rapidly evolving needs of the design and design automation communities across the world.

DAC61 has four wonderful keynote talks highlighting AI, Systems Foundry and Immersive Computing, along with several exciting SKYtalks and Techtalks covering a range of topics in chips, systems and applications.

There are 337 research papers across 29 tracks. We had a 34% increase in research paper submissions this year across all tracks and from all over the world, and a record 1,545 submissions—this is after an all-time record of submissions set last year. There are several Special Sessions featuring leading-edge research presentations by renowned experts along with Research Panels featuring luminaries from academia and industry discussing hot topics of current interest. To round out the Research Track, there are also Late Breaking Results (LBR) poster presentations and work-in-progress poster sessions.

Adding to the robust Research Track program is the exciting Engineering Track program targeted for industry practitioners and technical managers, focusing on four key areas: front-end design, back-end design, IP and embedded systems and software. Here, engineers from the industry share the latest innovations and key advancements. We had a 32% increase in the number of submissions this year, with strong focus on AI, Design and IP. We also have several invited presentations and panels featuring industry experts and executives discussing the latest hot topics driving innovation.

The exhibition floor is once again a highlight of the event, with the DAC Pavilion featuring analyst presentations, SKYtalks, Techtalks and controversial panels for lively discussions, along with the daily Poster Gladiator competition which is always fun to attend. New this year, the exhibit floor will host the Exhibitor Forum Theater with hourly technical presentations from exhibitors showcasing their technology and methodology offerings. We are pleased to also host 25 new exhibitors at this year's DAC! Make sure to visit the exhibition floor and check out the new technologies on the horizon.

Finally, I want to thank all who have helped to make DAC61 possible: Many thanks to my colleagues from the DAC EC, the TPC members of both the research and the engineering tracks, all the volunteers and employees from the sponsor's societies/councils as well as the management companies.

I look forward to welcoming you in person at the Moscone West in San Francisco – the "most cordial and sociable city", in the words of Mark Twain!

VIVEK DE

61st DAC General Chair

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CONFERENCE INFORMATION

Exhibit Hours

Location: First and Second Floor

Monday
10:00 am – 6:00 pm

Tuesday
10:00 am – 6:00 pm

Wednesday
10:00 am – 4:00 pm

Registration Hours

Location: Level 1 Lobby

Saturday	12:00 pm – 5:00 pm
Sunday	7:00 am – 7:00 pm
Monday	7:00 am – 7:00 pm
Tuesday	8:00 am – 6:00 pm
Wednesday	8:00 am – 6:00 pm

Online Proceedings

To view the proceedings, please visit – www.dac.com/proceedings61

Stay Connected

Enjoy complimentary WiFi at DAC:

Wifi Network: **DAC2024**
Wifi Password: **61DAC2024**

First Aid Room

Moscone West First Aid Office is located on the 1st Floor near the Howard Street entrance (behind registration).

Phone: 415.974.4159

REPORT ALL MEDICAL EMERGENCIES IMMEDIATELY

To report a medical emergency, call 511 on a white House Phone, or on a call phone dial 415.974.4021.

DAC Mobile App

You can download the official conference mobile app in the following ways:

- Search your device's App Store for "DAC Conferences"
- Go to the following link: www.core-apps.com/dl/61dac

Once the DAC Conferences application has downloaded,

- Choose "61st DAC"
- Select to download the event app.

Once you are in the app don't forget to set up your profile by going to the Publish My Profile icon. If you click the box to publish your profile your name (and picture if you upload one) will show in the Attendee icon. From there you can make "Friendships" with other attendees which will allow you to send messages, and set up private appointments.

For technical assistance please contact support@core-apps.com

DAC DIRECTORY MAP: LEVEL 1

LEVEL 1 LOBBY

Registration

LEVEL 1 EXHIBIT FLOOR

Exhibits - Aisles 1300 thru 1500

City Bytes & Beverages Food Court

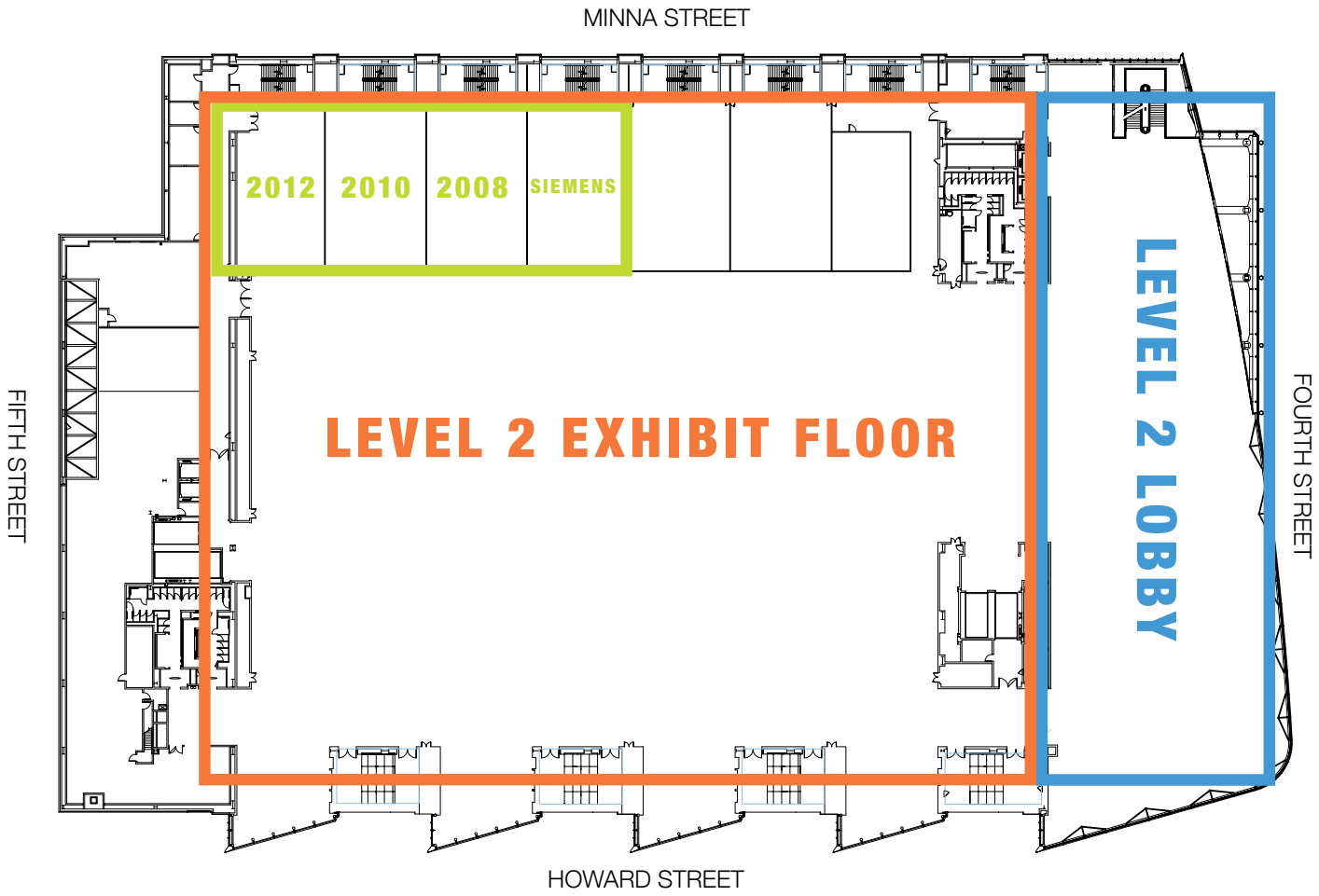
Exhibitor Forum

Exhibitor Meeting Rooms

2025 Exhibit Sales Office

Community Connection Zone

DAC DIRECTORY MAP: LEVEL 2



LEVEL 2 LOBBY

Networking Receptions

Work-in-Progress & Late Breaking Results Posters

HACK at DAC

Hands-on Training Sessions

PhD Forum/University Demo

LEVEL 2 EXHIBIT FLOOR

Exhibits - Aisles 2300 thru 2500

DAC Pavilion

Engineering Track Posters

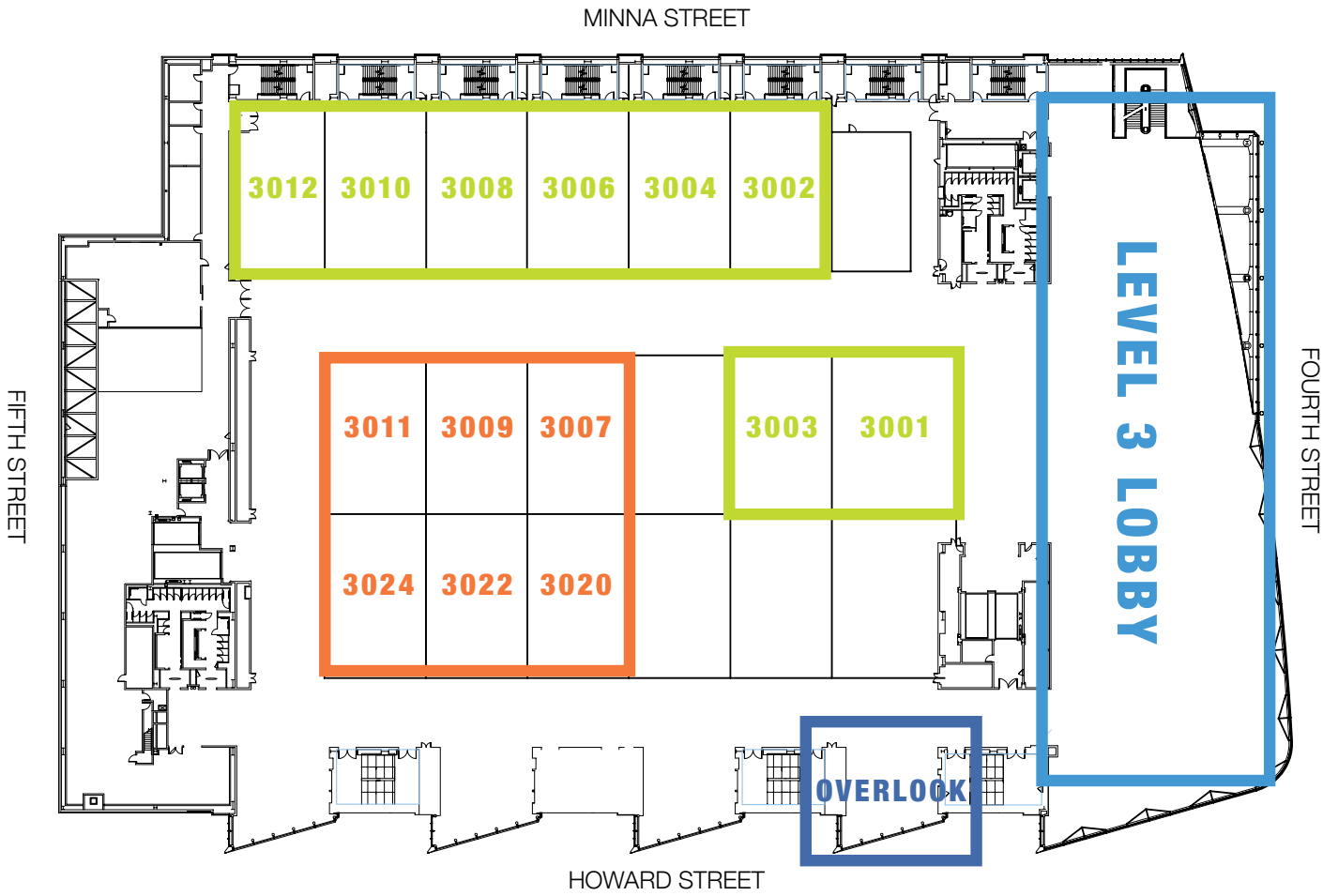
Engineering Track Sessions

Press Room

ROOMS 2008 – 2012

Engineering Track Sessions

DAC DIRECTORY MAP: LEVEL 3



LEVEL 3 LOBBY

Welcome Reception

Speaker Breakfast

Career Development Day

TPC Reception

ROOMS 3001 – 3012

Research Track Sessions

Birds of a Feather

Panel Sessions

Special Sessions

ROOM 3007, 3009, 3011, 3020-2024

Keynote *(Monday-Wednesday)*

OVERLOOK

Speaker Ready Room

DAC NETWORKING OPPORTUNITIES

Networking Receptions

Sunday, June 23

Welcome Reception
6:00 pm – 7:00 pm | Level 3 Lobby

Monday, June 24

Women in Tech Reception
6:00 pm – 7:00 pm | Level 2 Lobby

Engineering Track Poster Session
5:00 pm – 6:00 pm | Level 2 Exhibit Hall

Networking Reception
7:00 pm – 8:00 pm | Level 3 Lobby

Tuesday, June 25

Engineering Track Poster Session
5:00 pm – 6:00 pm | Level 2 Exhibit Hall

Networking Reception & Work-In-Progress Posters
6:00 pm – 7:00 pm | Level 2 Lobby

Wednesday, June 26

Networking Reception & Work-in-Progress/Late Breaking Results Poster Session
6:00 pm – 7:00 pm | Level 2 Lobby

THE CEDA DISTINGUISHED LUNCHEON KEYNOTE

Andrew B. Kahng: AI for EDA and Disruptive Innovation

Date: Tuesday, June 25 | **Time:** 12:00 pm – 1:30 pm | **Location:** 3018, 3rd Floor
Speaker: Andrew Khang, UC San Diego

Recent years have brought a flood of proposed applications for AI and machine learning in EDA. The potential benefits of AI for EDA, including improved design quality with reduced cost and schedule, have attracted significant efforts and focus across both academia and industry. But we have not seen truly disruptive innovation in this space – yet. This talk will examine what disruptive innovations at the AI-EDA nexus might look like. First, what are root causes for the absence of visible disruptions from AI-EDA innovations? These include technical and ecosystem challenges, the time and patience needed to reach tipping points, and the presence of active blockers to innovation. Second, where might advances in AI for EDA bring truly transformative, disruptive innovations to benefit the semiconductor ecosystem? Here, possibilities span analysis and simulation tooling, the nature of design signoff, the EDA-designer-foundry dynamic, and more. There are also basic categories of disruptive innovations: for the EDA business model; for the worldwide ecosystem of academic researchers, EDA vendors, and designers; and for EDA technology itself. Third, and finally, what will accelerate inevitable disruptive innovations, who might deliver them, and how?

Andrew B. Kahng is Distinguished Professor of CSE and ECE and holder of the endowed chair in high-performance computing at UC San Diego. He was visiting scientist at Cadence (1995-97) and founder/CTO at Blaze DFM (2004-06). He is coauthor of 3 books and over 500 journal and conference papers, holds 35 issued U.S. patents, and is a fellow of ACM and IEEE. He was the 2019 Ho-Am Prize laureate in Engineering. He has served as general chair of IEEE CEDA-sponsored conferences such as DAC, ISPD, SLIP and MLCAD, and from 2000-2016 served as international chair/co-chair of the International Technology Roadmap for Semiconductors (ITRS) Design and System Drivers working groups. He was the principal investigator of the U.S. DARPA "OpenROAD" project (https://theopenroadproject.org/) from June 2018 to December 2023, and until August 2023 served as principal investigator and director of "TILOS" (https://tilos.ai/), a U.S. NSF AI Research Institute.

KEYNOTE PRESENTATIONS

JIM KELLER

CEO, TENSTORRENT

Building AI with RISC-V

Monday, June 24 | 8:45 am – 9:45 am

How Tenstorrent built our first two generations of AI products. We'll tell you what went well, what went wrong and what we're doing next.

ABOUT: Jim Keller is CEO of Tenstorrent and a veteran hardware engineer. Prior to joining Tenstorrent, he served two years as Senior Vice President of Intel's Silicon Engineering Group. He has held roles as Tesla's Vice President of Autopilot and Low Voltage Hardware, Corporate Vice President and Chief Cores Architect at AMD, and Vice President of Engineering and Chief Architect at P.A. Semi, which was acquired by Apple Inc. Jim has led multiple successful silicon designs over the decades, from the DEC Alpha processors, to AMD K7/K8/K12, HyperTransport and the AMD Zen family, the Apple A4/A5 processors, and Tesla's self-driving car chip.

DR. GARY PATTON

CORPORATE VICE PRESIDENT AND GENERAL MANAGER OF THE DESIGN ENABLEMENT GROUP IN TECHNOLOGY DEVELOPMENT, INTEL CORPORATION

Systems Foundry - A Journey from 'System on a Chip' to 'System of Chips'

Tuesday, June 25 | 8:45 am – 9:45 am

In this keynote, Dr. Gary Patton will introduce the fundamental concepts driving the vision of a 'Systems Foundry', including a standards-based approach to assemble heterogenous dies. Dr. Patton will also cover the factors driving the inevitable need for disaggregation; factors like reticle limit, thermal constraints, cost, yield, etc., among others that are especially exacerbated in the need to satisfy the demands of HPC designs in the AI era. In addition, Dr. Patton will go over the transformative journey at Intel over the last 4-5 years that has helped orient the execution towards enabling the vision of a Systems Foundry. A journey that encompasses delivering to a full breadth of EDA offerings and development of advanced packaging capabilities, to name a few. The work is not done, however; the EDA & IP ecosystem has a vital role to play in this vision - to enable a seamless 3DIC design platform for advanced packaging implementation & modeling, AI-driven 3D exploration and System-Technology Co-Optimization while tackling challenges in the multi-physics domain. Intel has several collaborative projects with EDA to address these challenges, and Dr. Patton will end with a call to action to the ecosystem partners on continued partnership to realize this vision

ABOUT: Dr. Gary L. Patton is corporate vice president and general manager of the Design Enablement group in Technology Development at Intel Corporation. Design Enablement is charged with delivering the Process Design Kits (PDKs), Test-Chips, Design-Technology Co-Optimization (DTCO), and Foundational IP (FIP) & Embedded Memory Solutions to maximize technology value and meet customer needs and schedules. Prior to joining Intel, Dr. Patton served as is the Chief Technology Officer and Senior Vice President of Worldwide Research and Development and Design Enablement at GlobalFoundries where he was responsible for the semiconductor technology R&D roadmap, operations, and execution. Prior to that, Dr. Patton was vice president of IBM's Semiconductor Research and Development Center—a position that he held for eight years where he was responsible for IBM's semiconductor R&D, design enablement, and technology development alliances. Dr. Patton is a well-recognized industry leader in semiconductor technology R&D with over 30 years of semiconductor experience. He is a Fellow of the IEEE and recipient of the 2017 IEEE Frederik Philips Award for industry influence and leadership in the development of leading-edge microelectronics technology and collaborative research. In 2016, Dr. Patton was inducted into the VLSI Research Hall of Fame for his contributions to the advancement of the semiconductor industry over several decades. Dr. Patton received his bachelor's degree in electrical engineering from UCLA and his master's and Ph.D. degrees in electrical engineering from Stanford University

KEYNOTE PRESENTATIONS *continued*

ALAN LEE

CHIEF TECHNOLOGY OFFICER, ANALOG DEVICES, INC. (ADI).

AI and the Intelligent Edge

Wednesday, June 26 | 8:45 am – 9:45 am

Artificial intelligence is changing the world around us, but most of the focus has been on large models running on immense compute servers. There is a critical need for AI in edge applications to decrease latency and power consumption. Fulfilling this need requires new approaches to meet the constraints of future industrial, automotive, and consumer platforms at the intelligent edge.

ABOUT: As Chief Technology Officer, Alan Lee develops and leads ADI's long-term technology strategy for applications across the company's end markets, working closely with ADI's global business units and manufacturing operations to drive ADI's competitive advantage. Alan is responsible for identifying, sourcing, and cultivating new business, technology, and research opportunities, as well as developing foundational technology capabilities in support of the current and future needs of our markets and customers. Alan is a highly accomplished executive with over 20 years of experience in the technology industry. Most recently he served as the Corporate Vice President of Research and Advanced Development at AMD. During his tenure at the company, he founded AMD Research where he oversaw the company's worldwide research and advanced technology labs, university engagements, and external research contracting. Alan also led extreme-scale computing technology at AMD, where he drove the software and hardware engineering efforts to build the world's fastest platforms for machine learning, industrial, and scientific applications.

SARITA V. ADVE

RICHARD T. CHENG PROFESSOR, UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

Enabling the Era of Immersive Computing

Thursday, June 27 | 8:45 am – 9:45 am

Immersive computing (including virtual, augmented, mixed, and extended reality, metaverse, digital twins, and spatial computing) has the potential to transform most industries and human activities to create a better world for all. Delivering on this potential, however, requires bridging an orders of magnitude gap between the power, performance, and quality-of-experience attributes of current and desirable immersive systems. With a number of conflicting requirements - 100s of milliwatts of power, milliseconds of latency, unbounded compute to realize realistic sensory experiences – no silver bullet is available. Further, the true goodness metric of such systems must measure the subjective human experience within the immersive application. This talk calls for an integrative research agenda that drives codesigned end-to-end systems from hardware to system software stacks to foundation models spanning the end-user device/edge/cloud, with metrics that reflect the immersive human experience, in the context of real immersive applications. I will discuss work pursuing such an approach as part of the IMMERSE Center for Immersive Computing which brings together immersive technologies, applications, and human experience, and in the ILLIXR project based on an open-source end-to-end system to democratize immersive systems research.

ABOUT: Sarita Adve is the Richard T. Cheng Professor of Computer Science at the University of Illinois Urbana-Champaign where she directs IMMERSE, the Center for Immersive Computing. Her research interests span the system stack, ranging from hardware to applications. Her work on the data-race-free, Java, and C++ memory models forms the foundation for memory models used in most hardware and software systems today. Her group released the ILLIXR (Illinois Extended Reality) testbed, an open-source extended reality system and research testbed, and launched the ILLIXR consortium to democratize XR research, development, and benchmarking. She is also known for her work on heterogeneous systems and software-driven approaches for hardware resiliency. She is a member of the American Academy of Arts and Sciences, a fellow of the ACM and IEEE, and a recipient of the ACM/IEEE-CS Ken Kennedy award. As ACM SIGARCH chair, she co-founded the CARES movement, winner of the CRA distinguished service award, to address discrimination and harassment in Computer Science research events. She received her PhD from the University of Wisconsin-Madison and her B.Tech. from the Indian Institute of Technology, Bombay.

SKYTALK PRESENTATIONS

DR. JAY LEWIS

DIRECTOR OF THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER (NSTC) PROGRAM, CHIPS R&D OFFICE AT THE DEPARTMENT OF COMMERCE

CHIPS for America and Sustained U.S. Leadership: A Vision for Innovation Through the National Semiconductor Technology Center (NSTC)

Monday, June 24 | 1:00 pm – 1:45 pm | DAC Pavilion, Level 2 Exhibit Hall

The semiconductor industry has always moved fast, but changes in the industry over recent years have been historic. We will discuss a variety of challenges in the ecosystem, and how the NSTC can unite the community to address those challenges. Some of these are technical – logic, mixed signal, memory, photonics, design / co-design, and architecture all need new breakthroughs to continue to advance the state of technology. Others are ecosystem challenges. Access to design tools, IP, and collaboration environments, as well as increasing use of AI in the design and verification flow will all transform the way that the industry does its work. Access to advanced R&D facilities and leading-edge shuttles can accelerate the pace of research. The traditional venture model has been mismatched with hardware investments for decades, and this has been a drag on innovation, but there are new ideas for how this can work better. In closing, we will provide updates on the priorities for this year and show how the NSTC can change the long-term trajectory for innovation.

ABOUT: Dr. Jay Lewis is the Director of the National Semiconductor Technology Center, or NSTC, Program, for the CHIPS R&D Office at the Department of Commerce. In this role he is working to establish the NSTC program, a public-private consortium that will serve as a cornerstone of semiconductor research for the country. He previously worked at Microsoft, at DARPA, and had an early career in semiconductor research.

Dr. Lewis is a Fellow of the American Vacuum Society and is an IEEE and SPIE Senior Member. He has published over 50 articles in technical journals and conference proceedings and holds eleven U.S. patents. He received a Bachelor's degree in Materials Science from the Georgia Institute of Technology, and a Ph.D. in Materials Science and Engineering from the University of Florida.

NIELS FACHÉ

VP & GM, KEYSIGHT EDA

New EDA Methodologies are Transforming Engineering Lifecycle Management

Tuesday, June 25 | 1:00 pm – 1:45 pm | DAC Pavilion, Level 2 Exhibit Hall

This talk provides a broad, visionary perspective about the dynamic changes impacting electronic design automation tools and methodologies and their pivotal role in re-shaping engineering lifecycle management. It explains the trend toward convergence of EDA and CAE domains to address exploding system complexity and deliver multi-disciplinary solutions. Future workflows must incorporate digital threads that connect virtual prototypes and digital twins with physical systems. Predictive simulation and analysis across domains is key to accelerating engineering lifecycles.

Rapid industry adoption of AI, heterogeneous integrated circuits and chiplet technologies, software automation using scripting languages, and comprehensive data and intellectual property management tools is driving a seismic shift in design and verification methodologies. This talk covers how these EDA technologies contribute to more efficient and effective enterprise lifecycles. Application of these technologies must elevate RF, microwave, and mixed-signal design to an equal footing with digital design to achieve modernization of engineering workflows.

ABOUT: Niels Faché is responsible for Keysight's design and simulation portfolio. In his most recent positions, he was Vice President and General Manager of the Remarketing Solutions Division and then the Keysight Services Portfolio Organization, both part of Keysight's Global Services Organization (KGSO). Niels joined Hewlett Packard in 1994, when HP acquired Alphabit, a start-up software company in Belgium. He was co-founder and CEO of Alphabit, which developed the electromagnetic simulator Momentum - now part of the PathWave Advanced Design System (ADS). During his career, Niels has since held a variety of R&D, marketing, product planning and general management positions at HP, Agilent and Keysight in Electronic Design Automation, Test and Measurement Product Lines and Services. His roles have often involved leveraging technology and talented teams to transform and grow organizations into front-runners. He is based in Santa Clara, California. Niels holds a master's degree and Ph.D. in electrical engineering, both from the University of Ghent, Belgium, where he also served as a part-time professor from 1995 to 1997. He has a business degree from the Université Libre de Bruxelles, Belgium, and has completed coursework at the Stanford Center for Professional Development.

SKYTALK PRESENTATIONS CONTINUED

VIJI SRINIVASAN

DISTINGUISHED RESEARCH STAFF MEMBER, IBM

AI Acceleration Roadmap: Co-Designing Algorithms, Hardware, and Software

Wednesday, June 26 | 1:00 pm – 1:45 pm | DAC Pavilion, Level 2 Exhibit Hall

Deep Neural Networks (DNNs) have become state-of-the-art in a variety of machine learning tasks spanning domains across vision, speech, and machine translation. Deep Learning (DL) achieves high accuracy in these tasks at the expense of 100s of ExaOps of computation. Hardware specialization and acceleration is a key enabler to improve operational efficiency of DNNs, in turn requiring synergistic cross-layer design across algorithms, hardware, and software.

In this talk I will present this holistic approach adopted in the design of a multi-TOPs AI hardware accelerator. Key advances in the AI algorithm/application-level exploiting approximate computing techniques enable deriving low-precision DNNs models that maintain the same level of accuracy. Hardware performance-aware design space exploration is critical during compilation to map DNNs with diverse computational characteristics systematically and optimally while preserving familiar programming and user interfaces. The opportunities to co-optimize the algorithms, hardware, and the software provides the roadmap to continue to deliver superior performance over the next decade.

ABOUT: Viji Srinivasan is a Distinguished Research Staff Member and a manager of the accelerator architectures and compilers group at the IBM T.J. Watson Research Center in Yorktown Heights. At IBM, she has worked on various aspects of data management including energy-efficient processor designs, microarchitecture of the memory hierarchies of large-scale servers, cache coherence management of symmetric multiprocessors, accelerators for data analytics applications and more recently end-to-end accelerator solutions for AI. Many of her research contributions have been incorporated into IBM's Power & System-z Enterprise-class servers.

TECHTALK PRESENTATIONS

JUAN REY

VICE PRESIDENT OF GOVERNMENT PROGRAMS, SIEMENS

The Evolution of the Digital Twin in Semiconductor Design and the Central Role AI Plays

Tuesday, June 25 | 11:15 am – 12:00 pm | DAC Pavilion, Level 2 Exhibit Hall

Depending on who you talk with the Digital Twin is either the newest thing in semiconductor, or something that semiconductor has always had. The truth is that both are true. Semiconductor has long relied on domain specific Digital Twins of different aspects of the design in order to design, test, and integrate in the virtual world before committing to manufacture. Starting with the Siemens acquisition of EDA, but now being talked about more widely, we now talk about the Comprehensive Digital Twin of the design, which attempts to more completely capture the design and allow analysis using not only traditional EDA but also Multiphysics. This is just the beginning however, as we are already moving towards the merging of the Design Digital Twin, with the Manufacturing Digital Twin to enable closed loop manufacturing aware design.

This evolution brings with it new challenges of exponentially increasing complexity, and multiple disparate engineering domains that need to work together. It is here where AI is coming to the rescue to help guide where engineers need to focus their effort, encapsulate domain knowledge that they need to perform a task, and transform data between different domains either directly or via surrogate models.

In this presentation we will explore the way this evolution has affected IC and product design tools, the benefits it has brough to design teams, what the future holds, and how closed-loop manufacturing aware design will bring in a new era of design.

ABOUT: Juan C. Rey, vice-president of government programs, previous vice president of Engineering, Calibre, joined Mentor in 2001 as senior engineering director for Mentor's industry-leading Calibre product line, directing all development activities for Calibre products.

Previously he was vice-president of Engineering at Exend Corporation, managing all software development and quality activities. Prior to that he was engineering director for Physical Verification at Cadence Design Systems.

Earlier positions include: manager/developer for Process Modeling and Parasitic Extraction at Technology Modeling Associates; visiting scholar/science and engineering associate at Stanford University; senior research engineer at INVAP, Argentina; and associate professor at Universidad Nacional del Comahue, Argentina.

Juan holds a degree in Nuclear Engineering from Instituto Balseiro, Universidad Nacional de Cuyo, Argentina. The author or co-author of numerous papers and conference presentations, he serves on the Executive Technology Advisory Board of Semiconductor Research Corporation (SRC) and previously at the SI2 Board of Directors and the Industry Advisory Board of the UCLA Center for Domain-Specific Computing.

ANALYST PRESENTATIONS

JAY VLEESCHHOUWER

SENIOR INDUSTRY ANALYST COVERING ENGINEERING AND ENTERPRISE SOFTWARE, GRIFFIN SECURITIES

A View from Wall Street

Monday, June 24 | 10:15 am – 11:00 am | DAC Pavilion, Level 2 Exhibit Hall

We will examine the financial performance and key business metrics of the EDA industry through 2023, as well as the material technical and market trends and requirements that have influenced EDA business performance and strategies. Among the trends, we will again examine the progression of semiconductor R&D spending and how the market value of the publicly held EDA companies has evolved. Lastly, we will provide our updated financial projections for the EDA industry for 2024 through 2026.

ABOUT: Mr. Vleeschhouwer has over four decades of research experience. He is a senior industry analyst covering Engineering and Enterprise Software, responsible for fundamental research of companies under coverage, including the regular publication of proprietary company and industry reports and detailed company and industry financial modeling. Principal industry reports include The Software Standard (software industry commentary, news, data, and analysis) and The State of EDA (quarterly in-depth review of electronic design automation). Ranked by Refinitiv Starmine Analyst Awards (U.S.) #1 in “top stock pickers” for software (2020). He has been regularly invited to present at software and other industry conferences, in addition to broadcast media appearances and other print and online media

DYLAN PATEL

CHIEF ANALYST, SEMIANALYSIS

Designing an ASIC for the Generative AI Era

Tuesday, June 25 | 10:15 am – 11:00 am | DAC Pavilion, Level 2 Exhibit Hall

The presentation will cover what is required to design an ASIC for the Generative AI Era. It will cover the compute, networking, and memory constraints of generative AI as well as what companies are doing to push beyond it with optics, packaging, and system level design.

ABOUT: Dylan Patel is the founder and Chief Analyst of SemiAnalysis, a semiconductor and AI research company. SemiAnalysis has analysts across the US, Japan, Taiwan, Singapore, and France covering the industry from production of materials, equipment, process technology, fabs to design IP and fabless to physical infrastructe of datacenters, networking, and AI models.

ANALYST PRESENTATIONS CONTINUED

TOM HACKENBERG

PRINCIPAL ANALYST FOR COMPUTING AND SOFTWARE IN THE SEMICONDUCTOR, MEMORY AND COMPUTING DIVISION, YOLE INTELLIGENCE

Chiplets – The Next Generation Chip Design Trend Beyond Moore's Law

Wendesday, June 26 | 10:15 am – 11:00 am | DAC Pavilion, Level 2 Exhibit Hall

The next stage of integrated circuit manufacturing is disaggregation or breaking up the design of large chips into smaller units. These smaller units typically represent a unique function. The advantages are shorter design time, lower cost, easier drop-in inclusion of already available designs, increased modularity and scalability, and fewer manufacturing defects. This technique is especially well suited for leveraging the heterogeneous nature of large processors, coprocessors, system on chip (SoC) and integrated memory solutions, but the evolution of this trend is likely to spread throughout IC design.

This presentation is designed to provide a brief introduction to the nature of chiplet design and why it is so important at this time. The technical details will be presented in moderation including teardown examples of current chiplet solutions and which end-systems include them. The presentation will touch on technology advances that need to evolve to facilitate this approach. We will provide a market penetration and a five-year forecast for chiplet-based design strategies. We will provide longer views of the evolution to include such ICs as graphics, AI, and other accelerators, FGPAs, microcontrollers and other processors. We will conclude with why we think this trend is essential to the future of the semiconductor industry and design automation.

ABOUT: Tom Hackenberg is a Principal Analyst for Computing and Software in the Semiconductor, Memory and Computing Division at Yole Intelligence, part of Yole Group. Tom is an industry leading expert reporting on markets for semiconductor processors including CPUs, MPUs, MCUs and DSPs, SoCs, GPUs and discrete accelerators, FPGAs, and configurable processors since 2006. Tom is also well-versed in related technology trends including AI and edge computing, IoT, heterogeneous processing, chiplets, as well as vertical markets like Automotive, Computing and Telecommunications where processor trends play a significant role.

Tom has appeared as a presenter on these topics at associated events as the Chiplet Summit, OCP ODAS Workshop on Chiplets, Rosenblatt's Age of AI Scaling, System-on-Chip Conference, Vision and AI Summit, Xilinx Adapt: Automotive: Anywhere, Yole's Live Market Briefings and as well as custom proprietary presentations. He can also be found quoted or bylined in news and trade publications such as Cision, Computerworld, Design and Reuse, EE|Times & EE|Times Asia, Fierce Electronics, Insider, Semi Engineering, VentureBeat, and more for expertise on the processor market.

Tom worked with market-leading processor suppliers developing both syndicated and custom research. He holds a BSEE/BSECE from the University of Texas at Austin specializing in Processors and FPGAs.

IN MEMORIAM

Chris Spear 1960 – 2024

Chris Spear, a long-time veteran of our industry, passed away suddenly last February. Chris joined Mentor/Siemens EDA as a principal customer training engineer in 2016 drawing on his extensive background as an applications engineer working closely with verification engineers in his previous roles. He literally wrote the book on "SystemVerilog for Verification" and his dedication and passion for sharing his knowledge led to his pivotal role in shaping Siemens EDA's training strategies in the design verification domain. During his tenure, Chris's live training classes on SystemVerilog and UVM proved invaluable to hundreds of engineers, offering an unmatched educational experience to both new and seasoned engineering professionals. This is a quote from a verification engineer who attended Chris's advanced UVM class shortly before his passing: "I really enjoyed the in-class instruction of Chris Spear; his willingness to impart, engage and understand makes him an invaluable resource and highly effective instructor."

Chris's love for his family knew no bounds. He was an avid cyclist and enjoyed spending time in nature during his cycling expeditions and explorations at home and in various countries around the globe. Many of you may be familiar with and have supported Chris's decades-long participation in the Pan-Mass Challenge, an annual bike-a-thon for life-saving cancer research and treatment at Dana Farber Cancer Institute, for which Chris fundraised and rode every summer.

In Siemens EDA and the design verification communities, we mourn the loss of a dear friend and colleague, and the world has lost an exceptional individual. Our deepest condolences go to his family, friends, and colleagues.

Lynn Ann Conway (1938 - 2024)

Lynn Ann Conway was an American computer scientist, electrical engineer and transgender activist. She worked at IBM in the 1960s and invented generalized dynamic instruction handling, a key advance used in out-of-order execution, used by most modern computer processors to improve performance.

Lynn initiated the Mead–Conway VLSI chip design revolution in very large scale integrated (VLSI) microchip design. That revolution spread rapidly through the research universities and computing industries during the 1980s, incubating an emerging electronic design automation industry, spawning the modern 'foundry' infrastructure for chip design and production, and triggering a rush of impactful high-tech startups in the 1980s and 1990s

DAC AWARDS AND SCHOLARSHIPS

2024 DAC UNDER-40 INNOVATORS AWARD

In recognition for technical contributions of notable impact in the field of design and automation of electronic circuits and systems

Nishant Patil, Apple

Bei Yu, Chinese University of Hong Kong

Bita Darvish Rouhami, Nvidia

Jingtong Hu, University of Pittsburgh

Farimah Farahmandi, University of Florida

2024 MARIE R. PISTILLI WOMEN IN ENGINEERING ACHIEVEMENT AWARD

For displaying equality, diversity, and acceptance while visibly helping to advance women in electronic design

Sashi Obilisetty, Synopsys

ACM/SIGDA

ACM TODAES ROOKIE AUTHOR OF THE YEAR (RAY) AWARD

Wenjing Jiang, University of Minnesota

2024 ACM TODAES BEST PAPER AWARD

Shanshi Huang, **Hongwu Jiang**, **Shimeng Yu**, Georgia Tech

ACM SIGDA DISTNGUISHED SERVICE AWARD

Marilyn Wolf, University of Nebraska-Lincoln

Patrick Haspel, Synopsys, Inc.

ACM SIGDA OUTSTANDING NEW FACULTY AWARD

Bonan Yan, Peking University

ACM FELLOWS

Anand Raghunathan, Purdue University

Rolf Drechsler, University of Bremen

Massoud Pedram, University of Southern California

ACM SIGDA OUTSTANDING PH.D. DISSERTATION AWARD

Lukas Burgholzer, Johannes Kepler University

SIGDA PIONEERING ACHIEVEMENT AWARD

John Darringer, IBM Research

SIGDA SERVICE AWARD

Weiwen Jiang, George Mason University

Yu-Guang (Andy) Chen, National Central University, Taiwan

Fan Chen, Indiana University

Ahmad Sadeghi, TU Darmstady

IEEE/CEDA

IEEE CEDA OUTSTANDING SERVICE AWARD

For outstanding service to the EDA community as DAC General Chair in 2022

Jorg Henekl, Karlsruhe Institute of Technology

IEEE FELLOWS

Jinjun Xiong, University of Buffalo

Qinru Qiu, Syracuse University

Haoxing Ren, NVIDIA

Sudeep Pasricha, Colorado State University

Sri Parameswaran, The University of New South Wales

Lei He, UCLA

Tsung-Yi Ho, The Chinese University of Hong Kong

IEEE/ACM A RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION

Mircea Stan, University of Virginia

Wayne Burleson, University of Massachusetts Amherst

IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS DONALD O. PEDERSON BEST PAPER AWARD

PACT: An Extensible Parallel Thermal Simulator for Emerging Integration and Cooling Technologies

Zihao Yuan, Boston University

Prachi Shukla, Boston University

Sofiane Chetoui, Boston University

Sean Nemtzow, Boston University

Sherief Reda, Boston University

Ayse K Coskun, Boston University

An Open-Source Framework for FPGA Emulation of Analog/Mixed-Signal Integrated Circuit Designs

Steven Herbst, Stanford University

Gabriel Rutsch, Infineon Technologies AG, Germany

Wolfgang Ecker, Infineon Technologies AG, Germany

Mark Horowitz, Stanford University

IEEE GUSTAV ROBERT KIRCHOFF AWARD

Mary Jane Irwin, Pennsylvania State University

2024 PHIL KAUFMAN AWARD FOR DISTINGUISHED CONTRIBUTIONS TO ESD

For overall impact on Electronics industry through contributions to scan design for testability, related test automation.

Lawrence Pileggi, Carnegie-Mellon University

DAC PAVILION SCHEDULE

The location for all events is:
DAC Pavilion | Level 2 Exhibit Hall

Monday, June 24

10:15 am – 11:00 am

ANALYST REVIEW: A VIEW FROM WALL STREET

Speaker: Jay Vleeschhouwer, Griffin Securities

11:15 am – 12:00 pm

PANEL: BEST OF BOTH WORLDS: BRIDGING THE GAPS IN ENGINEERING SOFTWARE FOR SEMICONDUCTORS AND SYSTEMS

Moderator: Jay Vleeschhouwer, Griffin Securities

Panelists: Tom Beckley, Cadence Design Systems, Inc.; Philippe Laufer, Dassault Systemes; Niels Fache, Keysight; Paul Sagar, PTC; Tony Hemmelgarn, Siemens; Shankar Krishnamoorthy, Synopsys

1:00 pm – 1:45 pm

SKYTALK: CHIPS FOR AMERICA AND SUSTAINED U.S. LEADERSHIP: A VISION FOR INNOVATION THROUGH THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER (NSTC)

Speaker: Dr. Jay Lewis, Director of the National Semiconductor Technology Center (NSTC) Program CHIPS R&D Office at the Department of Commerce

2:00 pm – 2:45 pm

PANEL: A NEW DESIGN VERIFICATION ERA AS OPEN-SOURCE UPENDS THE STATUS QUO

Moderator: Ron Wilson, Ojo-Yoshida Report

Panelists: Jean-Marie Brunet, Siemens; Darren Jones, Andes; Josh Scheid, Ventana Microsystems; Ty Garibay, Condor Computing

3:00 pm – 3:45 pm

COOLEY'S DAC TROUBLEMAKER PANEL

Moderator: John Cooley, Deepchip

Panelists: Tony Hemmelgarn, Siemens; Shankar Krishnamoorthy, Synopsys; Paul Cunningham, Cadence Design Systems, Inc.; Dean Drako, IC Manage; Prakash Narain, Real Intent; Joe Costello, Metrics

4:30 pm - 5:30 pm

GLADIATOR ARENA POSTER BATTLE

Tuesday, June 25

10:15 am – 11:00 am

ANALYST REVIEW: DESIGNING AN ASIC FOR THE GENERATIVE AI ERA

Speaker: Dylan Patel, SemiAnalysis

11:15 am – 12:00 pm

TECHTALK: THE EVOLUTION OF THE DIGITAL TWIN IN SEMICONDUCTOR DESIGN, AND THE CENTRAL ROLE AI PLAYS

Speaker: Juan Rey, Siemens

1:00 pm – 1:45 pm

SKYTALK: NEW EDA METHODOLOGIES ARE TRANSFORMING ENGINEERING LIFECYCLE MANAGEMENT

Speaker: Niels Fache, Keysight

2:00 pm – 2:45 pm

PANEL: BLACKOUT – MANAGING KW POWER BUDGETS

Moderator: Ed Sperling, Semiconductor Engineering

Panelists: Joe Davis, Siemens; Mo Faisal, Movellus; Trey Roessig, Empower; Dean Wallace, Marvell; Hans Yeager, Tenstorrent

3:00 pm – 3:45 pm

PANEL: ADVANCING CHIP SECURITY TO MEET HEIGHTENED REQUIREMENTS

Moderator: Ann Mutscher, Semiconductor Engineering

Panelists: Andreas Kuehlmann, Cycuity; Neeraj Paliwal, Rambus; Victoria Coleman, US Air Force; Vivek Tiwari, Intel

4:30 pm - 5:30 pm

GLADIATOR ARENA POSTER BATTLE

Wednesday, June 26

10:15 am – 11:00 am

ANALYST REVIEW: CHIPLETS – THE NEXT GENERATION CHIP DESIGN TREND BEYOND MOORE'S LAW

Speaker: Tom Hackenberg, Yole Group

11:15 am – 12:00 pm

PANEL: FROM DESIGN TO DEFENSE: SHAPING THE FUTURE OF MICROELECTRONICS SECURITY

Moderator: Nitin Dahadembedded.com

Panelists: Cayley Rice, Leidos; Margaret Schmitt, Amida Technology Solutions; Mark Tehranipoor, University of Florida; Simha Sethumadhavan, Columbia University/Chip Scan Inc.

1:00 pm – 1:45 pm

SKYTALK: AI ACCELERATION ROADMAP: CO-DESIGNING ALGORITHMS, HARDWARE, AND SOFTWARE

Speaker: Viji Srinivasan, IBM Thomas J. Watson Research Center

2:00 pm – 2:45 pm

GLADIATOR ARENA POSTER BATTLE

3:00 pm – 3:45 pm

ENGINEER TRACK BEST PAPER AWARD & GLADIATOR AWARDS ANNOUNCEMENT

Program accurate as of June 17, 2024.

Locations listed for each speaker are representative of where they live, not where their corporate office is located.

FULL PROGRAM

Sunday, June 23, 2024

DCGAA 2024: INTERNATIONAL WORKSHOP ON DL-HARDWARE CO-DESIGN FOR GENERATIVE AI ACCELERATION)

Time: 8:00 AM – 12:00 PM
Session Type: Workshop
Topic Area(s): AI
Room: 3004, 3rd Floor

Organizer(s): Dongkuan Xu, North Carolina State University, Raleigh, NC; Hua Wei, Arizona State University, Tempe, AZ; Ang Li, University of Maryland, College Park, MD; Tinoosh Mohsenin, Johns Hopkins University, Baltimore, MD; Peipei Zhou, University of Pittsburgh, Pittsburgh, PA; Caiwen Ding, University of Connecticut, Storrs, CT; Yingyan (Celine) Lin, Georgia Institute of Technology, Atlanta, GA; Yanzhi Wang, Northeastern University, Boston, MA

Description: In the ever-evolving domain of computational technologies, the profound impact of artificial intelligence (AI) is indisputable. The DCgAA 2024 Workshop stands at the forefront of this revolution, offering an essential platform for synergizing deep learning (DL) models with advanced hardware system designs. This second iteration of our workshop is dedicated to exploring and fortifying the symbiotic relationship between DL and hardware innovation, especially in the context of generative AI applications. Deep learning's integration across various computing sectors necessitates robust hardware solutions to amplify model performance and efficiency. However, current DL research often overlooks critical real-world computational constraints such as power efficiency, memory usage, and scalability of model sizes. This oversight limits the practical deployment of AI innovations, particularly in scenarios requiring high computational efficiency like mobile devices, AR/VR technologies, and other edge computing environments. Our workshop aims to bridge this gap by fostering discussions and research on optimizing hardware designs specifically tailored for generative AI applications. We will delve into the unique computational demands of these models and the necessity of hardware systems that can adapt to their complex requirements. This approach is pivotal for realizing the full potential of DL innovations and ensuring their effective application in real-world scenarios.

IN-MEMORY ARCHITECTURES AND COMPUTING APPLICATIONS WORKSHOP (IMACAW) - 3RD EDITION

Time: 8:00 AM – 5:00 PM
Session Type: Workshop
Topic Area(s): Design
Room: 3001, 3rd Floor

Organizers: Albert Bosio, Lyon Institute of Nanotechnology, Lyon, France; Nima TaheriNejad, Heidelberg University, Heidelberg, Germany; Deliang Fan, Johns Hopkins University, Baltimore, MD

Description: Today's computer architectures and device technologies used to manufacture them are facing major challenges, rendering them incapable of delivering the performances required by complex applications such as Big-Data processing and Artificial Intelligence (AI). The iMACAW workshop aims at providing a forum to discuss In-Memory-Computing (as an alternative architecture) and its potential applications. To this end, we take a cross-layer and cross-technology approach covering State-of-the-Art (SoA) works that use SRAM, DRAM, FLASH, RRAM, PCM, MRAM, or FeFET as their memory technology. The workshop also aims at reinforcing the In-Memory-Computing (IMC) community and at offering a holistic vision of this emerging computing paradigm to the design automation communities. This workshop proposal follows the two previous editions hosted in DAC1, it will provide an opportunity for the audience to listen to invited speakers who are pioneers of the field, learn from them, ask questions, and interact with them. Open submission contributors also get the opportunity to share their knowledge, present their most-recent work, and their work in progress with the community, interact with other experts in the field, and receive feedback.

SSH-SOC: SAFETY AND SECURITY IN HETEROGENEOUS OPEN SYSTEM-ON-CHIP PLATFORMS

Time: 8:00 AM – 5:00 PM
Session Type: Workshop
Topic Area(s): Security
Room: 3002, 3rd Floor

Organizer(s): Francesco Restuccia, University of California, San Diego, CA; Angelo Garofalo, University of Bologna, Bologna, Italy; Biruk Seyoum, Columbia University, New York City, NY; Luca Benini, ETH Zurich, Zurich, Switzerland

Description: The diminishing returns of technology scaling on performance have paved the way for innovation in computer architecture, shifting towards heterogeneous, domain-specific architectures. Modern systems incorporate domain-specific accelerators and specialized system components (buses, network-on-chip, peripherals, sensors, etc..) to efficiently manage complex and computationally demanding workloads.

A widely adopted approach to reduce the System-on-Chip (SoC) design complexity involves a hierarchical strategy that differentiates the system design efforts for the components of the heterogeneous architecture. This encompasses: (i) expensive in-house RTL development for critical modules, (ii) leveraging the most recent high-level synthesis (HLS) tools, and/or (iii) outsourcing highly specialized third-party intellectual property (IP) modules to reduce costs and development time.

Despite its advantages, such diversified design methodology exacerbates the challenge of system integration. Moreover, recent studies have demonstrated how careless system integration can lead to dangerous conditions, impacting the security, safety, and performance of the system. This can result from a combination of factors, including development bugs, lack of specifications, superficial verifications of IP components' behavior at the system level, and a scarcity of mechanisms supporting safe and secure system execution.

Addressing these challenges requires innovative approaches in the design and verification process, especially when dealing with the stringent safety and security requirements of mission-critical systems. The research community can play a disruptive role in overcoming these challenges. The availability of the complete codebase of multiple mature open hardware architectures and reconfigurable platforms represents an unprecedented opportunity for the development, testing, and native integration of novel mechanisms, tools, and analysis supporting security, safety, and performance efficiency for the development of the next-generation of systems.

This workshop welcomes work-in-progress contributions and innovative directions aimed at addressing challenges and profit from the opportunities provided by open hardware designs and architectures for the development of next-generation heterogeneous SoCs. The topics for the workshop include, but are not restricted to:

- Security verification for hardware designs and system architectures
- Architectural aspects of secure system integration
- Secure system integration of third-party hardware components
- Automated firmware generation supporting secure system execution
- Security aspects of reconfigurable designs
- Time-predictable system execution in open-hardware designs
- Performance analysis, timing analysis, and worst-case analysis supporting time-predictable system execution and/or communications in open-hardware designs
- Automated firmware generation supporting time-predictable execution
- Fault tolerance and execution in harsh conditions leveraging open-hardware designs
- System architectures and methodologies supporting energy efficient/performant system execution in open-hardware designs
- Hardware/software co-design, co-integration and co-verification of open-source processors, accelerators, and components
- Open architectures for reconfigurable platforms and open CAD tools
- Tools and analysis for open FPGAs and reconfigurable platforms

WORKSHOP ON CHIPLET-BASED HETEROGENEOUS INTEGRATION AND CO-DESIGN (CHICO)

Time: 8:00 AM – 5:00 PM
Session Type: Workshop
Topic Area(s): EDA
Room: 3003, 3rd Floor

Organizer(s): Yu Cao, University of Minnesota, Minneapolis, MN; Puneet Gupta, University of California, Los Angeles, CA

Description: Contemporary microelectronic design is facing tremendous challenges in memory bandwidth, processing speed and power consumption. Although recent advances in monolithic design (e.g. near-memory and in-memory computing) help relieve some issues, the scaling trend is still lagging behind the ever increasing demand of AI, HPC and other applications. In this context, technological innovations beyond a monolithic chip, such as 2.5D and 3D packaging at the macro and micro levels, are critical to enabling heterogeneous integration with various types of chiplets, and bringing significant performance and cost benefits for future systems. Such a paradigm shift further drives new innovations on chiplet IPs, heterogeneous architectures and system mapping.

This workshop is designed to be a forum that is highly interactive, timely and informative, on the related topics:

- Roadmap and technology perspectives of heterogeneous integration
- IP definition for chiplets
- Signaling interface cross chiplets
- Network topology for data movement
- Design solutions for power delivery
- Thermal management
- Testing in a heterogeneous system
- High-level synthesis for the chiplet system
- Architectural innovations
- Ecosystems of IPs and EDA tools

GREAT: GEN-AI RESEARCH IN ELECTRONIC DESIGN, AUTOMATION, AND TEST

Time: 1:00PM – 5:00 PM
Session Type: Workshop
Topic Area(s): Design
Room: 3004, 3rd Floor

Organizer(s): Ramesh Karri, New York University, New York City, NY; Siddharth Garg, New York University, New York City, NY; Jeyavijayan Rajendran, Texas A&M University, College Park, TX

Description: Large language models (LLMs) have been a significant breakthrough in artificial intelligence, demonstrating remarkable success in solving various real-world problems. These models, trained on vast amounts of text data, have shown an uncanny ability to generate human-like text, understand context, answer questions, and write code. They have been successfully deployed in numerous applications, including customer service, content creation, and language translation, to name a few. The versatility and robustness of LLMs have made them an invaluable tool in the AI toolkit, opening up avenues for exploration and innovation. Microsoft, Google, Meta, and Amazon have invested in generative AI technologies like LLMs.

One such avenue that has garnered attention is using LLMs in chip design. Digital chip design, a complex and intricate process, involves the creation of integrated circuits used in various electronic devices. LLMs are expected to aid designers during design and concept development, verification, validation, and security checks. For instance, Synopsys has recently developed an LLM-based framework to aid chip design and development.

With these revolutionary developments and interest from leading electronic design automation companies (Cadence, Synopsys, Siemens) and chip design companies (Intel, Nvidia, Qualcomm, IBM, etc.), there is an increasing need for a greater understanding of LLMs' roles in EDA. We are organizing this first "Workshop on Gen-AI for Chip Design", consisting of:

(i) Introductory session on LLMs for chip design (1:00-1:30)

(ii) Three-hour "Design a Chip in a Day" competition (e.g., RTL generation and testing) open to the EDA, AI, and Design community (students, academics, practitioners, hobbyists) (1:30-4:30)

(iv) Closing session on the next steps (4:30-5:00) Together, these sessions will highlight the advances of LLMs for chip design, research adventures in academia, and provide hands-on experience for LLM-based chip design.

HOW WILL AI DRIVE EDA AND IP GROWTH

Time: 5:00 PM - 6:00 PM
Topic Area: Ai, EDA, IP
Room: 3002, 3rd Floor

Author: Charles Shi, Needham & Company, LLC

Description: With the advent of generative AI, the landscape of the semiconductor industry is changing. AI is accelerating the in-sourcing of semiconductor design by systems companies. Vertical integration from silicon to systems is on the rise. One of the consequences of this changing landscape is that chip design appears to be capturing a greater piece of the pie in semiconductor value chain. This trend represents a major opportunity for the EDA and IP industry, who are the pick-and-shovel provider to the AI gold rush. In this presentation, we review the latest trends in semiconductors and explain why we think EDA and IP industry is the place to be in the AI super cycle.

KEYNOTE PRESENTATION WITH JIM KELLER

Time: 8:45 AM – 9:45 AM
Session Type: Keynote
Room: 3007, 3rd Floor
Description: Jim Keller is CEO of Tenstorrent and a veteran hardware engineer. Prior to joining Tenstorrent, he served two years as Senior Vice President of Intel's Silicon Engineering Group. He has held roles as Tesla's Vice President of Autopilot and Low Voltage Hardware, Corporate Vice President and Chief Cores Architect at AMD, and Vice President of Engineering and Chief Architect at P.A. Semi, which was acquired by Apple Inc. Jim has led multiple successful silicon designs over the decades, from the DEC Alpha processors, to AMD K7/K8/K12, HyperTransport and the AMD Zen family, the Apple A4/A5 processors, and Tesla's self-driving car chip.

A VIEW FROM WALL STREET

Time: 10:15 AM – 11:00 AM
Session Type: Analyst Presentation
Topic Area(s): EDA
Room: DAC Pavilion, Level 2 Exhibit Hall
Description: We will examine the financial performance and key business metrics of the EDA industry through 2023, as well as the material technical and market trends and requirements that have influenced EDA business performance and strategies. Among the trends, we will again examine the progression of semiconductor R&D spending and how the market value of the publicly held EDA companies has evolved. Lastly, we will provide our updated financial projections for the EDA industry for 2024 through 2026.

Speaker: Jay Vleeschouwer, Griffin Securities

FLASH - AN OVERLOOKED TECHNOLOGY IN VLSI DESIGN

Time: 10:30 AM – 12:00 PM
Session Type: Tutorial
Topic Area(s): Design
Room: 3002, 3rd Floor
Description: In the semiconductor industry, floating gate (flash) transistors have exclusively been used for non-volatile memory such as USB memory and solid-state drives (SSDs). This tutorial will present work on circuit design and design automation approaches demonstrating that flash can be used to design high-quality general-purpose VLSI ICs, both digital and analog. In particular, we will cover:

A) Flash-based realizations of both digital [2-9] and secure digital [1] ICs. These realizations have shown significantly improved power, delay and area compared to CMOS standard-cell based designs. The approaches in [2-7] use a PLA-based design flow. In contrast, [8-9] utilize a standard-cell based design approach augmented with flash cells, thereby leveraging many decades of EDA development in the standard-cell based design flow. The approach of [1] provides significant security against foundry-based reverse engineering, without a penalty in power, delay or area compared to CMOS designs. In all these approaches, we have developed logic synthesis flows to automate the insertion of flash-based cells in the design.

B) Flash-based realizations of analog circuits such as low-dropout voltage regulators [10-11], Digital-to-Analog converters [13], FIR filters [12], and other DSP engines. Many benefits are availed by using flash-based designs for these [12-13] circuits, including reduced area, power, energy. In [10-11], flash-based design enables the use of the same design to achieve several LDO specifications, thereby resulting in a significant saving in manufacturing costs.

C) Flash-based mixed-signal designs such as convolutional neural network accelerators (both analog [14-16] and digital [17] variants), and other flash-based in-memory computing designs [18]. With flash-based mixed-signal current-mode CNN realizations [14-16], several common CNN architectures can be realized on the same die, resulting in 50X lower energy, and a latency improvement of 15X to 490,000X over [17], which is a state-of-the-art BNN.

A common theme of the above designs is that flash-based designs demonstrate several advantages over conventional CMOS designs, such as performance tunability, the ability to counteract circuit aging due to effects such as NBTI, the control of speed binning, and the ability to mitigate the effects of process variations. For secure designs, we show that if an adversary illegally gains possession of the IC, our approach can allow the functionality of a "kill switch", whereby the circuit operator can erase the flash transistors in the secure design, rendering it non-functional. We further demonstrate that scalability in the 3rd dimension can be leveraged for all these designs, using emerging 3D NAND and NOR flash technologies that are widely available for flash memory applications. Even though flash transistors do not scale to the feature sizes of traditional CMOS designs, we show that by using 3D flash fabrication techniques, a similar chip-level density (compared to traditional CMOS designs) in terms of transistors/area can be achieved.

Based on our findings, we posit that the programmability, robustness, stability, and maturity of flash give it a significant edge to CMOS in many ways, making it a practical alternative to CMOS in many applications.

Presenters: Sunil Khatri, Texas A&M University, College Station, TX; Sarma Vrudhula, Arizona State University, Tempe, AZ

GDSFACTORY: AN OPEN SOURCE PLATFORM FOR END-TO-END CHIP DESIGN, VERIFICATION AND VALIDATION

Time: 10:30 AM – 12:00 PM
Session Type: Tutorial
Topic Area(s): EDA
Room: 3003, 3rd Floor

Description: For efficient design, verification and validation of integrated circuits and components it is important to have an easy to customize and extend workflow. Python has become the standard programming language for machine learning, scientific computing and engineering.

Gdsfactory is a python library to build chips (Photonics, Analog, Quantum, MEMs, …) that provides you a common syntax for design (KLayout, Ansys, tidy3d, MEEP, MPB, DEVSIM, SAX, …), verification (Klayout DRC, LVS, netlist extraction, connectivity checks, fabrication models) and validation (JAX neural network model extraction, pandas, SQL database).

In this tutorial we will cover the gdsfactory design automation tool. Gdsfactory provides you an end to end workflow that combines layout, verification and validation using an extensible, open source, python driven flow for turning your chip designs into validated products.

https://gdsfactory.github.io/gdsfactory-photonics-training/notebooks/10_layout_full.html

Presenters: Joaquin Matres, Helge Gehring, Google, Mountain View, CA; Simon Bilodeau, Princeton University, Princeton, NJ; Niko Savola, Aalto University, Espoo, Finland; Troy Tamas, Rockley Photonics, Pasadena, CA

HIGH PERFORMANCE COMPUTING USING SUPERCONDUCTOR ELECTRONICS

Time: 10:30 AM – 12:00 PM
Session Type: Tutorial
Topic Area(s): Design
Room: 3001, 3rd Floor

Description: This half-day tutorial aims to impart a comprehensive understanding of the theory and application of superconductor electronics, spanning from the foundational principles of superconductivity to the operational intricacies of superconductor logic cells and digital circuits. The tutorial will explore diverse applications, ranging from neuromorphic computing and signal processing to homomorphic computing and quantum computing.

Presenters: Massoud Pedram, Sasah Razmkhah, University of Southern California, Los Angeles, CA; D. Scott Holmes, IEEE IRDS, Washington, DC; Eby Friedman, University of Rochester, Rochester, NY

EXPLORE CONCEPTS OF STA THRU INSIGHTFUL CRAFTSMANSHIP

Time: 10:30 AM – 12:00 PM
Session Type: Engineering Track
Topic Area(s): Back-End Design
Room: 2008, 2nd Floor

Session Chairs: Lakshmanan Balasubramanian, Texas Instruments (India) Pvt. Ltd., IEEE

Description: TBD. Dusamusda con pro oditatur molorum quam et audio. Ut aut de pore eicipis inti ut et ent quae vellit erchitatur, qui ant, quid est, et aut labor aut aut aliqui berument magnisitas simentius aut ilia sitatib usdaernata ipsandae prorpor acea por sunt exerepudae estiorem repro ommo eos dolorerio. Itate prem voluptae et alit accabor epelitatur? Qui con nonsequas sandenist a sinus mo eate volorest reped etur, omnim eum restio. Ebisciatet pel inusti berendae. Lendit qui dolo eos evellorero estis volorum am et velit lamet atem dia vitatur mint que omnimint facest elis entin everitatem estrum imin cum nis evendae cone solorem. Ut eatur alicipsum quis imagnis magni ratiis auda consequi quiam nimpores

- **TSV KOZ Separation 3DIC P&R Area Optimization Methodology Considering Device Impact by TSV**
  Yongjin Hong, Ki-Ok Kim, Mijeong Lim, Jun Seomun Byunghyun Lee, Sangyun Kim, Samsung Electronics, Seoul, South Korea;
- **ML Based PPA Push using DRV Prediction**
  Jungho Kim, Kyoungsun Cho, Sunghoon Kim, Mintae Lee, Wook Kim, Ki-Ok Kim, Sangyun Kim, Samsung, Seoul, South Korea;
- **Model Margining Algorithm for High Performance SOC closure**
  Subhadeep Aich, Tejas Salunkhe, Siddharth Sarin, Gaurav Patil, Texas Instruments, Bengaluru, India;
- **Pruning Netlist: A Smarter Approach to Efficient and Reliable Circuit Characterization** Harsh Garg, Pawan Verma, Saurabh Srivastava, Anil Dwivedi, Fillaud Matthieu, Siemens, Grenoble, France;
- **Clock Parameter Tuning with an Intelligent Adaptive Learning to Improve Performance and Power of Multisource Clock Tree Synthesis**
  Divyarajsinh Vaghela, Jagadeesh Gnanasekaran, Gaurav Bhatia, Intel, Karnataka, India;
- **An Effective Hierarchical STA Solution for Closing Large SoC Design**
  Shourya Shukla, Sainarayanan Suryanarayanan, Marvell, Bengaluru, India; Sushant Hajare, Marvell, Jaipur, India; Harshit Jaiswal, Sharath AC, Cadence Design Systems, Inc., Bengaluru, India; Nitin Jain, Cadence Design Systems, Inc., Montbonnot-Saint-Martin, France

AI CO-PILOT: EXPLORING THE AI FRONTIER IN CHIP DESIGN

Time: 10:30 AM – 12:00 PM
Session Type: Engineering Track
Topic Area(s): Front-End Design
Room: 2010, 2nd Floor

Organizers: Moshe Zalcberg, Veriest Solutions Ltd., Petach Tikva, Israel

Moderator: Serge Leef, Microsoft, Camas, WA

Description: Generative AI is everywhere, but it's still making its first steps in Chip Design. In this session, we'll invite representative from the design community to review the challenges and present working solutions on using AI for front-end chip design, with an emphasis in sharing "how-to" ideas.

Presenters: Sid Dhodhi, NVIDIA, Santa Clara, CA; Amber Telfer, Microsoft, Hillsboro, OR; Priyanka Mathikshara, Voltai, Stanford, CA

CHERISHED MEMORIES - EXPLORING THE POWER OF INNOVATIVE MEMORY ARCHITECTURES FOR AI APPLICATIONS

Time: 10:30 AM – 12:00 PM
Session Type: Engineering Track
Topic Area(s): IP
Room: 2012, 2nd Floor

Organizers: Moshe Zalcberg, Veriest Solutions Ltd.

Moderator: Raul Camposano, Silicon Catalyst, Santa Clara, CA

Description: With all the discussion about Moore's Law, one thing is for sure: Memories aren't scaling as much as logic. On the other hand, AI applications, so popular these days, require increasing amount of memory. Add to that the need to extend the use of available fabs, and you get a great reason to explore new memory paradigms.

In this session we'll explore cutting-edge technologies transforming the landscape of memory design. The expert speakers will share real-world applications in AI, machine learning, and edge computing, exploring new technologies and optimization strategies.

Presenters: Andreas Burg, RAAM Technologies, Zurich, Switzerland; Gideon Intrater, Weebit Nano, San Francisco, CA; Sushil Sudam Sakhare, Veevx Inc, Mesa, India

SECURE COLLABORATION ACROSS ENTERPRISES ON THE CLOUD

Time: 10:30am – 11:00am
Session Type: Exhibitor Forum
Topic: IP
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Modern SoCs require the integration of IP and tools from multiple vendors. Chip designers often must work with their IP vendors, tool vendors, and design service providers. This collaboration often requires enterprises to onboard third parties into their network to jointly work on a solution, requiring security exceptions. By leveraging the cloud as a secure independent collaboration platform, customers no longer need to make compromises with security to onboard third parties. The Microsoft Azure Modeling and Simulation Workbench makes it easy for customers to bring up a secure design environment and invite third parties to collaborate while keeping them isolated to the workbench.

Presenters: Prashant Varshney, Microsoft

ULTRA-FAST VARIATION CHARACTERIZATION FOR EMBEDDED MEMORIES AND IP BLOCKS

Time: 11:15 AM – 11:45 AM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Process variation library models in the Liberty Variation Format (LVF) have become commonplace in timing signoff for standard cells, yet the embedded memories that comprise most of the chip area still employ library modeling methodologies from several technology generations ago. The main challenge is the greatly increased amount of simulation required to extract meaningful LVF data compared to nominal timing characterization.

It is known that the effect of random process variation is local to a small portion of the circuit. LVF characterization methods based on full-macro or critical-path simulation observe these effects at a global or near-global scale. As a result, they cannot fully utilize the simulation power and causes inefficiency. We believe a good methodology combining strategically partitioning the design and localized OCV models can greatly improve the efficiency of LVF characterization, without compromising accuracy.

This presentation unveils the key technologies behind Liberal-Mem, the memory characterization system from Empyrean, with a highly efficient solution to embedded memory characterization, especially to LVF extraction.

Presenters: Danny Li, Ken Tseng, Empyrean Technology

BEST OF BOTH WORLDS: BRIDGING THE GAPS IN ENGINEERING SOFTWARE FOR SEMICONDUCTORS AND SYSTEMS

Time: 11:15 AM – 12:00 PM
Session Type: Pavilion Panel
Room: DAC Pavilion, Level 2 Exhibit Hall

Moderator: Jay Vleeschouwer, Griffin Securities

Description: This panel will explore, with leading software companies, a phenomenon that has long been anticipated: the business, market and technical convergences of the two halves of Engineering Software (EDA and "industrial" software). These convergences are increasingly evident in the companies' product and acquisition strategies.

Panelists: Tom Beckley, Cadence Design Systems, Inc.; Philippe Laufer, Dassault Systemes; Niels Fache, Keysight; Shankar Krishnamoorthy, Synopsys; Tony Hemmelgam, Siemens; Paul Sagar, PTC

ENABLING A NEW ERA OF SOFTWARE SHIFT LEFT WITH VELOCE CS

Time: 12:00 PM – 12:30 PM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Speaker: Vijay Chobisa, Siemens

Description: As software defined products become the norm and software workloads impact every aspect of system architecture and implementation, we need ways to include software in every aspect of the design from early architecture exploration, through logic design, and into integration and validation. This places new demands on systems designers, creates new verification challenges, and at the same time opens opportunities for design teams to begin software design long before silicon availability.

In this presentation we will explore the changing face of design in a software defined world, how software shift lest can accelerate product development while reducing risk, and how the unique capabilities offered by the new Siemens EDA Veloce CS platform makes software shift left available to all design teams.

CHIPS FOR AMERICA AND SUSTAINED U.S. LEADERSHIP: A VISION FOR INNOVATION THROUGH THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER (NSTC)

Time: 1:00pm – 1:45pm
Session Type: SKYTalk
Topic: EDA
Room: DAC Pavilion, Level 2 Exhibit Hall

Description: The semiconductor industry has always moved fast, but changes in the industry over recent years have been historic. We will discuss a variety of challenges in the ecosystem, and how the NSTC can unite the community to address those challenges. Some of these are technical – logic, mixed signal, memory, photonics, design / co-design, and architecture all need new breakthroughs to continue to advance the state of technology. Others are ecosystem challenges. Access to design tools, IP, and collaboration environments, as well as increasing use of AI in the design and verification flow will all transform the way that the industry does its work. Access to advanced R&D facilities and leading-edge shuttles can accelerate the pace of research. The traditional venture model has been mismatched with hardware investments for decades, and this has been a drag on innovation, but there are new ideas for how this can work better. In closing, we will provide updates on the priorities for this year and show how the NSTC can change the long-term trajectory for innovation.

Presenters: Jay Lewis, National Semiconductor Technology Center

AUTOMATED CO-DESIGN OF COMPLEX SYSTEMS: FROM AUTONOMY TO FUTURE MOBILITY SYSTEMS

Time: 1:30 PM – 3:00 PM
Session Type: Tutorial
Topic Area(s): Design
Room: 3003, 3rd Floor

Description: The contemporary era struggles with the intricate challenge of designing ``complex systems''. These systems are characterized by intricate webs of interactions that interlace their components, giving rise to multifaceted complexities, springing from at least two sources.

First, the co-design of complex systems (e.g., a large network of cyber-physical systems) demands the simultaneous selection of components arising from heterogeneous natures (e.g., hardware vs. software parts), while satisfying system constraints and accounting for multiple objectives.

Second, different components are interconnected through interactions, and their design cannot be decoupled (e.g., within a mobility system). Navigating this complexity necessitates innovative approaches, and this tutorial responds to this imperative by focusing on a monotone theory of co-design. Our exploration extends from the design of individual platforms, such as autonomous vehicles, to the orchestration of entire mobility systems built upon such platforms.

In particular, we will delve into the theoretical foundations of a monotone theory of co-design, establishing a robust mathematical framework and its application to a diverse array of real-world problems, revolving around the domain of embodied intelligence.

The presented toolbox empowers efficient computation of optimal design solutions tailored to specific tasks and, in its novelty, paves the way for several possibilities for future research. This tutorial will focus on the particular application of computational design of autonomous systems, featuring both a technical and a practical session. Participants will have the opportunity to explore dedicated demos and “learn by doing” through guided exercises.

The tutorial provides participants with an introduction to robot co-design and aims to connect multiple communities to enable the development of composable models, algorithms, fabrication processes, and hardware for embodied intelligence. It is intended to be accessible from any background and seniority level and will present applications to a wide array of topics of interest to the design automation and robotics communities.

Presenters: Gioele Zardini, Massachusetts Institute of Technology, Cambridge, MA; Andrea Censi, ETH Zurich, Switzerland

EXPLORING ALTERNATIVE CORRIDORS FOR OPTIMAL ROUTES

Time: 1:30 PM – 3:00 PM
Session Type: Engineering Track
Topic Area(s): Back-End Design
Room: 2008, 2nd Floor

Session Chairs: Patricia Fong, Marvell Semiconductor

Description: Find your inner Nemo! Explore multiple pathways to getting around the barriers in floorplanning, be it memories. cutlines or using thesymmetry of the edges. Use AI to assist your route plan.

- **A Novel Solution for Fast and Efficient Custom Bus Routing with User-defined Reference Wire and Combination of Segmented Bus Option**
  Sungsik Park, Samsung Electronics, Seoul, South Korea; Keunbong Lee, Cadence Design Systems, Inc., San Francisco, CA;
- **Memory IO Block Routing Optimization using Semi-Automation of Single Trunk Steiner Tree Routing**
  Seyong Ahn, Hyeyoun Kim, Kwangok Jeong, Jungyun Choi, Samsung Electronics, Seoul, South Korea;
- **A New Frontier for Floorplanning with AI**
  Pinkesh Shah, Maxlinear, Bangalore, India; Alpesh Kothari, Siemens, Bengaluru, India; Raghu Ram Gude, Siemens, Fremont, CA;
- **A Systematic Approach to 3D Cutline Exploration and Benchmarking**
  Chung-Ching Peng, Kurt Chu, CH Yang, Zih-Nan Tseng, Aaron Liou, Bryant Chang, Intel, Taipei, Taiwan; Justin Aguilar, Wei Zhou, Intel, Santa Clara, CA; Vivek Rajan, Intel, Mountain View, CA; Pinhong Chen, Jags Jayachandran, Naresh Mummidivarapu, Yashodhara Tarey, Kumar Subramani, Cadence Design Systems, Inc., Saratoga, CA;
- **Automatic Layout Symmetry Annotation via Graph Node Embeddings**
  Jerome Lescot, Francois Lemery, STMicroelectronics, Grenoble, France

STATIC AND FORMAL VERIFICATION: PILLARS OF MODERN DESIGN ASSURANCE

Time: 1:30 PM – 3:00 PM
Session Type: Engineering Track
Topic Area(s): Front-End Design
Room: 2010, 2nd Floor

Session Chair: Puneet Anand, Qualcomm

Description: This session explores the essential role of static and formal tools in ensuring the correctness and reliability of complex hardware designs. We will discuss key techniques, industry trends, and case studies highlighting the benefits of these powerful methodologies.

- **Enhancing Formal Equivalence for Datapath Algorithms: A Proof Strategy with Intermediate Modeling to Address Structural Differences in Implementations**
  Suraj Kamble, Intel, Swaresh Phadke, Intel, Disha Puri, Intel, Bengaluru, India; Aarti Gupta, Intel, Folson, CA;
- **Leveraging Formal Verification to Create, Reproduce, Verify Design Scenarios from Simulation Wave-dump**
  Ujjwal Talati, Saikiran Ashwini, Aman Chauhan, Viraj Rawal, Nivin George, Synopsys India Pvt. Ltd., Bengaluru, India;
- **Formal CDC Glitch Check - Advanced Sign Off Solution**
  Noam Eshel Goldman, Liad Nehama, Marvell, Petah Tikva, Israel; Vikas Sachdeva, Polina Pashayev, Real Intent, Bengaluru, India;
- **Breaking the Formal Convergence Barriers for a Floating-Point Dot-Product Block for AI/ML Accelerators**
  Satyabrata Sarangi, Sai Ma, Adrian Lewis, Rohan Mallya, Eda Sahin, Meta, Sunnyvale, CA; Neelabja Dutta, Ashish Kapoor, Reily Jacoby, Synopsys, Sunnyvale, CA;
- **Ensuring Harmless Customization of RISC-V processors through Formal Sequential Equivalence Checking**
  Nicolae Tusinschi, SEDA, Munich, Germany; Laurent Arditi, Codasip, Valbonne, France;
- **A Novel Formal Verification Technique to System Verification using Contract Refinement**
  Surinder Sood, Nirmal Jose, Arm Ltd., Manchester, United Kingdom; Scott Meeth, Arm Ltd., San Jose, CA

LEADING EDGE DIGITAL IP

Time: 1:30 PM – 3:00 PM
Session Type: Engineering Track
Topic Area(s): IP
Room: 2012, 2nd Floor

Session Chair: Barun Bikash Paul, Broadcom

Description: Digital IP design has to improve rapidly to catch up with the speed and performance requirements for massive compute intensive applications in the AI era. IP designers are exhausting every possible combination to improve power, performance and area efficiency of digital design. In this section, we talk about algorithmic changes that double the throughput of an Ethernet switch, a fast calibration method for PHYs, an FPGA based hardware accelerator, AI based technology library selection to optimize the PPA, arbiter logic for high performing systems and a highly efficient CXL memory compression design for data center applications.

- **100Gbps Class In-vehicle Ethernet Switch Architecture for Next Generation Autonomous Driving Car**
  Takahiro Sekine, Renesas Electronics, Tokyo, Japan;
- **Hybrid Tiled Vector Systolic Architecture to Accelerate Convolution on FPGAs**
  Jay Shah, Nanditha Rao, International Institute of Information Technology, Bangalore, India;
- **Evaluating Power, Performance, and Area for Standard Cell Libraries from Different IP Providers**
  Aravind Radhakrishnan Nair, Infineon Technologies, Munich, Germany; Ajay Kumar, Siemens, Wilsonville, OR; Austin Shirley, Siemens, Houston, TX; Lars Kishchuk, Siemens, Saskatoon, Canada;
- **Window Feedback Based Multi-Master Arbiter IP for Efficient Hardware Resource Sharing**
  Gianluca Rigano, STMicroelectronics, Agrate Brianza, Italy;
- **An All-Digital IP for Fast Correction of Time-skew Mismatch in Time-Interleaved Analog to Digital Converters for Communication Receivers**
  Ankur Bal, Aradhana Kumari, STMicroelectronics, Noida, India;
- **Open Compute Platform(OCP) ready Hardware Accelerated CXL Memory Compression IP for Data Center Applications**
  Nilesh Shah, ZeroPoint Technology AB, Goteborg, Sweden

DESIGN AND SYNTHESIS OF CERTIFIABLY SAFE AI-ENABLED AUTONOMY WITH FOCUS ON HUMAN-IN-THE-LOOP HUMAN-IN-THE PLANT SYSTEMS

Time: 1:30 PM – 5:00 PM
Session Type: Tutorial
Topic Area(s): Autonomous Systems
Room: 3002, 3rd Floor

Description: Advent of Large Language Models (LLM) and generative AI has introduced uncertainty in operation of autonomous systems with significant implications on safe and secure operation. This has led to the US government directive on assurance and testing of trustworthiness of AI. This tutorial aims at introducing the audience to the arising safety issues of AI-enabled autonomous systems (AAS) and how is affects dependable and safe design for real life deployments. With the advent of LLMs and deep AI methods, AAS are becoming vulnerable to uncertainties. It will introduce a new human in the loop human in the plant design philosophy that is geared towards assured certifiability in presence of human actions and AI uncertainties while reducing data sharing between the AAS manufacturer and certifier. We will provide a landscape of informal and formal approaches in ensuring AI-based AAS safety at every phase of the design lifecycle, defining the gaps, current research to fill those gaps, and tools for detection of commonly occurring software failures such as doping. This tutorial also aims at emphasizing the need for operational safety of AI-based AAS and highlight the importance of explainability at every stage for enhancing trustworthiness. There has been significant research in the domain of model-based engineering that are attempting to solve this design problem. Observations from the deployment of a AAS are used to: a) ascertain whether the AAS used in practice match the proposed safety assured design, b) explain reasons for a mismatch in AAS operation and the safety assured design, c) generate evidence to establish the trustworthiness of a AAS, d) generate novel practical scenarios where a AAS is likely to fail.

AI has been widely adopted in different domains including autonomous vehicles and IoT medical device. In a competitive environment, engineers and researchers are focused on developing innovative applications while minimal attention is provided to safety engineering techniques that cope with the fast pace of technological advances. As a result, recent failures and operational accidents of AI-based system highlight a pressing need for the development of suitable stringent safety monitoring techniques. We advocate for a change in the linear AAS development lifecycle from design, validation, implementation, and verification by incorporating feedback from the field of operation. This will result in a circular AAS development lifecycle, where operational data can be used to identify novel states and can be used as feedback. This will enable an agile proactive redesign policy that can predict failures and propose techniques to circumvent any safety risks. The tools used in this circular lifecycle will provide interpretable reports to the appropriate stake holders such as certification agencies, developers and users at different stages. This tutorial directly relates to the Autonomous systems, ML, topic of DAC.

Presenters: Ayan Banerjee, Sandeep Gupta, Arizona State University, Tempe, AZ; Imane Lamrani, Nikola Motors, Tempe, AZ

SHOW TO WRITE RISC-V PSS MODELS TO ENABLE GENERATING VERIFICATION SCENARIOS FOR RISC-V PLATFORMS

Time: 1:30 PM – 5:00 PM
Session Type: Tutorial
Topic Area(s): EDA
Room: 3001, 3rd Floor

Description: RISC-V is an industry wide ISA (Instruction Set Architecture) standard used for developing embedded processors that target Semiconductor products of any type. PSS (Portable Stimulus) is an Accellera standard verification language used by EDA companies to develop tools, that given a PSS Model, generates coverage driven scenarios to enable meeting verification goals with less effort, taking advantage of portability, abstraction, and automation capabilities enabled by the language. In this tutorial we teach how to code PSS Models needed for the verification of any RISC-V platform (e.g. RISC-V embedded core platform, RISC-V multi-core coherent platform, RISC-V SOC (System on Chip) with external interfaces, etc.).

Synopsys as a RISC-V developer is providing reference methodologies for the verification and debugging of RISC-V system designs are available now, along with Synopsys EDA flows, emulation and virtual prototyping solutions, and methodologies to further support RISC-V SoC verification. Collaborative efforts include RISC-V verification methodology cookbook for Bluespec cores, "Understanding UVM Coverage for RISC-V Processor Designs" white paper, RISC-V and processor verification using ImperasDV verification solutions, and the industry-leading Synopsys VCS® simulation and Verdi® debug tools for improved efficiency (see news release).

As PSS usage grows together with the incoming requests to better enable PSS for RISC-V platforms, we endeavor to expand on a methodology cookbook with the addition of PSS. In this tutorial we enable the RISC-V PSS eco community with some fresh ideas on how to use PSS to get started. We introduce the PSS modeling patterns below that can be used to get started and hopefully provide an appetite to use and create more.

For each modeling pattern, we give a name and a short explanation of what the pattern consists of:

(1) Basic: PSS modeling techniques that can be used to generate basic RISC-V assembly code sequences. (2) Integration: PSS modeling techniques that can be used to generate RISC-V assembly code that interacts with generated traffic scenario's consisting of embedded C and SV testbench generate code.(3) Nested loops and routines: PSS modeling techniques that can be used to generate legal assembly code with nested loops and nested routine calls.(4) Memory sharing: PSS modeling techniques that can be used to generate blocks of assembly code that share memory, with exclusive and non-exclusive access. (5) Runtime parameterization: PSS modeling techniques that can be used to generate parameterized assembly code run on a post-silicon, where a host device can change parameters on-the-fly.(6) Validating the scenario: PSS modeling techniques to create a reference model in PSS that can be used as an executable specification to debug and validate PSS generated scenarios.

The expectation is that this 3-hour tutorial will provide any RISC-V platform developer with a good enough tool kit to be able to perform all verification requirements needed for a RISC-V platform.

Presenters: Sandeep Mehrotra, Synopsys, Mountain View, CA; Hillel Miller, Synopsys, Austin, TX; Santosh Kumar, Qualcomm, San Diego, CA

POST-QUANTUM CRYPTOGRAPHY IMPLEMENTATION ATTACKS AND COUNTERMEASURES

Time: 1:30pm – 5:00pm
Session Type: Tutorial
Topic: Security
Room: 3004, 3rd Floor

Description: Post-Quantum Cryptography (PQC) encompasses cryptographic algorithms, typically public-key algorithms, designed to be secure against quantum and classical computers. Motivated by the threat posed by quantum computing to the security of most public-key algorithms currently in use, the National Institute of Standards and Technologies (NIST) started in December 2016 the PQC Standardization Process, a public competition for selection of public-key cryptosystems designed to resist attacks by a quantum computer. After three rounds of competition, in July 2022, NIST announced the first four proposals to be standardized, which include one key-establishment mechanism (i.e., CRYSTALS-Kyber) and three digital signatures (i.e., CRYSTALS-Dilithium, Falcon and SPHINCS+). CRYSTALS-Kyber and CRYSTALS-Dilithium are the primary algorithms recommended for most use cases, while Falcon and SPHINCS+ are proposed for use cases that require small signatures and non-lattice-based signatures, respectively. Shortly after NIST's announcement, in September 2022, the National Security Agency (NSA) published the Commercial National Security Algorithm Suite (CNSA) 2.0 advisory on protection of National Security Systems (NSS), which includes the approved PQC algorithms and the transition timeline. In August 2023, NIST requested public comments on the drafts of the standards derived from CRYSTALS-Kyber, CRYSTALS-Dilithium, and SPHINCS+.

This tutorial aims to introduce the audience to the implementation attacks published in the literature against the primary PQC algorithms to be standardized by the National Institute of Standards and Technologies (NIST) and approved by the National Security Agency (NSA) for national security systems (i.e., Kyber and Dilithium) as well as countermeasures against these implementation attacks. Other PQC standardization efforts will be mentioned. The goal is to prepare the hardware security community with the information required to do research in this field, play an active role in the remaining steps of the standardization process, and support secure deployment of PQC.

Presenters: Daniel Dinu, Intel; Prasanna Ravi, Nanyang Technological University; Marrkku-Juhani Saarinen, PQShield Ltd; Silvio Dragone, IBM Research

UNDERSTANDING ANSYS SIGMADVD – A RADICAL NEW METHODOLOGY FOR VOLTAGE DROP ANALYSIS AND SIGNOFF

Time: 1:45pm – 3:00pm
Session Type: Exhibitor Forum
Topic: Design
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: One of the most difficult challenges for IC designers today is power integrity signoff at advanced nodes and how to achieve comprehensive dynamic voltage drop (DVD) coverage. Attend this session to learn how leading IC design teams no longer rely only on traditional vectored/vectorless analysis but are adopting a radical new SigmaDVD™ technology from Ansys to address urgent DVD issues at advanced nodes . SigmaDVD is becoming the leading method for avoiding DVD voltage and timing problems, shift-left prevention of voltage-drop issues, fixing IR violations, and achieving robust, high-coverage power integrity signoff.

Presenters: Murat Becer, Ansys; Chip Stratakos, Microsoft

A NEW DESIGN VERIFICATION ERA AS OPEN-SOURCE UPENDS THE STATUS QUO

Time: 2:00 PM – 2:45 PM
Session Type: DAC Pavilion Panel
Room: DAC Pavilion, Level 2 Exhibit Hall

Moderator: Ron Wilson, Ojo-Yoshida Report

Description: RISC-V and a growing open-source ecosystem have moved from hype to reality. Consequently, the semiconductor industry is at an inflection point as architectural paradigms require early power and performance metrics, creating demand for new design, verification and validation technologies and methodologies.

Engineers now have the ability to design a specific rather than generic open-source instruction set easily customizable to an application in a vertical market. It's an era where RISC-V starts are not just starts but used in volume production.

The status quo has been upended and with it a challenge with a new open-source ecosystem versus the trust of a traditional, well-established and rich ecosystem. The new open-source instruction set and software don't have legacy, experience and domain knowledge sharing, particularly software validation's usage and experience.

It could also become an exciting era for design verification as it becomes the chief enabler for the new ecosystem and architecture, especially hardware-assisted verification that can serve as a risk mitigation tool.

A panel of design and verification users and experts, all of whom have studied the open-source ecosystem and its requirements and deficiencies, will be part of the DAC Pavilion Panel. DAC attendees are invited to listen in as they discuss where emphasis should be placed for the next-generation design verification flow. Audience participation will be encouraged.

Panelists: Jean-Marie Brunet, Siemens; Darren Jones, Andes; Josh Scheid, Ventana Microsystems; Ty Garibay, Condor Computing

COOLEY'S TROUBLEMAKER PANEL

Time: 3:00pm – 3:45pm

Session Type: DAC Pavilion Panel; Analyst Review

Topic: EDA

Room: DAC Pavilion, Level 2 Exhibit Hall

Moderator: John Cooley, Deepchip

Description: Come watch the EDA troublemakers answer the edgy, user-submitted questions about this year's most controversial issues! It's an old-style open Q&A from the days before corporate marketing took over every aspect of EDA company images.

Panelists: Tony Hemmelgarn, Siemens; Shankar Krishnamoorthy, Synopsys; Paul Cunningham, Cadence Design Systems, Inc.; Dean Drako, IC Manage; Prakash Narain, Real Intent; Joe Costello, Metrics

TRANSFORMING SEMICONDUCTOR DESIGNS USING SYSTEMC BASED SHIFT-LEFT METHODOLOGIES

Time: 3:30 PM – 4:00 PM

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Since the inception of the semiconductor industry in the 1950s, there have been continuous advancements on multiple fronts. Semiconductor chips are becoming more and more powerful & complex.

Designing such complex chips is extremely difficult, costly and error prone. Design methodologies have also evolved to keep the pace with growing complexity. Historically this evolution came in the form of raising the abstraction of chip design: component level to gate level, and further to RTL.

Shift-left methodology allows the identification and resolution of flaws early in the design cycle. Fast simulation models allow early software development in parallel to hardware design. It is feasible to engage with the potential customers and validate the SoC architecture with the real customer workloads quite early in the cycle. These methodologies significantly reduce the Cost & Time to market. Overall it enhances the probability of success for a new SoC.

Two key trends in the industry today are, usage of chips for AI applications, and emergence of an open source processor architecture RISC-V ISA. Effective use of the ESL methodologies is necessary for the success of these trends.

The presentation will cover the virtual prototype of Core-V-MCU, an open source System on Chip from OpenHW group. This SoC has a RISC-V CPU core, an embedded FPGA, on chip SRAM, and a rich set of peripherals.

Presenters: Umesh Sisodia, Rameez Syed, CircuitSutra Technologies

DEEP DIVE IN FOUNDRY PROCESS DESIGN KITS (PDKS)

Time: 3:30 PM – 5:00 PM

Session Type: Tutorial

Topic Area(s): AI

Room: 3003, 3rd Floor

Description: In the realm of ever evolving Semiconductor technology landscape with complex SoC's and Systems, integration of Chat GPT like AI Transformers in IP/SoC Design Verification could potentially revolutionize a transformative wave of automating verification there by contributing to increased robustness of designs.

IP and SOCs underpin many modern electronic systems like HPC/ AI and Automotive SoC's. While functional correctness is crucial, it no longer suffices for real-world applications and usage. In this paper we have explored to utilize the power of light-weight generative AI BER Transformer Model in verification as it redefines the possibilities of how we interact with textual data, including hardware design specifications and taking verification to completeness by suggesting extra scenarios for Performance and Security aspects. It bridges the gap between 'what' a system does, 'how well' it performs, and 'how securely' it operates and addresses the grey areas in system level verification which cannot be captured at IP or sub-system level.

We can scale this model to SOC level and try to address verification challenges for miscellaneous SOC IP's like GPIO,DFT mux, Lower Power Elements and Safety Elements.

This paper highlights the power of using Generative AI in verification, Augmenting AI with verification can help us catch bugs/issues early in the verification life cycle.

Presenter: Amit Kumar, Microsoft, Mountain View, CA; James Baie, Intel, Austin, TX; Jignesh Patel, GlobalFoundries, Irvine, CA

HISTORY, PRESENT, AND FUTURE OF STA: A TRAVEL THROUGH TIMING

Time: 3:30 PM – 5:00 PM
Session Type: Engineering Track
Topic Area(s): Back-End Design
Room: 2008, 2nd Floor

Organizers: Sabya Das, Synopsys, Sunnyvale, CA

Moderator: Bertram Bradley, Marvell, Austin, TX

Description: Static Timing Analysis (STA) has evolved dramatically in the last 20 years. From a fairly simple extraction and back annotation of a single flat entity, and analysis in a couple of bounding timing corners, it has grown exponentially as technology nodes have advanced to consider many other physical factors, and handle design data sizes and STA engineering team sizes almost unthinkable 20 years ago. Join us on this historical retrospective, a brief check-in to current STA techniques and requirements, and a glimpse into the future as to what may be coming in the near future, and what EDA can do to help. Speakers from Marvell, Synopsys, and IBM will cover the full history, present and future of STA in this exciting and entertaining presentation.

Presenters: Tim Helvey, Marvell, Rochester, MN; Peivand Tehrani, Synopsys, Mountain View, CA; Kerim Kalafala, IBM, Hopewell Junction, NY

DEMOCRATIZING CHIP DESIGN

Time: 3:30 PM – 5:00 PM
Session Type: Engineering Track
Topic Area(s): IP
Room: 2008, 2nd Floor

Organizers: Sashi Obilisetty, Synopsys, Mountain View, CA

Description: It took sixty years for the semiconductor industry to reach 500 billion, but it is widely expected that we will hit the 1 trillion mark towards the end of this decade. This explosive growth needs to come with several shifts in the way we design chips, including attracting, educating, and enabling a whole new generation of designers. Learn from industry luminaries on their perspectives on how we can successfully hit the trillion dollar mark.

Presenters: Andrew Kahng, University of California, San Diego, CA; Mohamed Kassem, eFabless, Palo Alto, CA; Valeria Bertacco, University of Michigan, Ann Arbor, MI

NOC NOC - WHO'S THERE?

Time: 3:30 PM – 5:00 PM
Session Type: Engineering Track
Topic Area(s): IP
Room: 2012, 2nd Floor

Organizers: Moshe Zalcberg, Veriest Solutions Ltd., Petach Tikva, Israel

Moderator: Moshe Zalcberg, Veriest Solutions Ltd., Petach Tikva, Israel

Description: "Network on a Chip" or NoC refers to a communication subsystem that enables communication between various components or modules on the chip. It is a network-based approach to managing data transfer and communication within a microprocessor or a system-on-chip (SoC).

Presenters: Guillaume Boillet, Arteris, Cupertino, CA; Kamal Desai, Synopsys, San Ramon, CA; Jonathan Ezroni, Mobileye, Jerusalem, Israel; Andrea Majstorovic, Veriest Solutions Ltd., Belgrade, Serbia

HARDWARE SECURITY AT RTL - AN AI/ML-BASED APPROACH

Time: 4:15 PM – 4:45 PM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Speakers: Margaret Schmitt, Amida Technology Solutions

Description: Microelectronics are essential to critical infrastructure, yet they are increasingly at risk from cyber attacks and malicious hardware modifications. The current state of security analysis primarily addresses known threats, leaving undiscovered vulnerabilities largely concealed on the dark side of the attack surface.

We will introduce a patented Register Transfer Level (RTL) analysis technique that offers both qualitative and quantitative insights into semiconductor designs. This advanced methodology identifies and quantifies potential vulnerabilities that are susceptible to attack vectors that target functional behavior, operational reliability, and data integrity.

This predictive approach facilitates the cyber hardening of designs and helps achieve convergence on device-level security coverage. Furthermore, our experimental results show that the framework can be used to detect in-field attack. We utilize machine learning to adaptively recognize threats, and can demonstrate on-chip integration of next-generation protection into the semiconductor design lifecycle.

This session will detail our innovative approach, emphasize the importance of proactive security measures in the design phase of microelectronics development, and how this platform can reveal, surveil, quarantine, and remediate sophisticated cyber threats to improve the cyber resilience of critical electronic systems.

KEY FOR TRULY UP-TO-DATE, ACCURATE, AND REUSABLE EDA LIBRARY

Time: 5:00 PM – 5:30 PM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Speakers: Julie Liu, Palpilot International

Description: A DAC panel in year 1993[1] emphasized the need for design engineers to have a component library management system/platform that provides software tools for rapid generation and management of up-to-date, EDA-neutral, complete, and reusable libraries. This would save time and costs in product design. However, some questions remain unanswered until recently:

1) Should this library platform be provided by EDA tool providers, by component providers, by ODM/OEM companies, or by a third-party organization?
2) What factors enable a library platform to truly provide up-to-date, accurate, and reusable libraries?

In today' industry, different EDA tools are not compatible with each other, making it nearly impossible for a tool provider to develop a library platform that support multiple EDA formats. Component providers and semiconductor companies are only responsible for giving components to customers and supplying specification datasheets in PDF format. Product design and manufacturing companies (ODM/OEM) can only create libraries according to their own needs. Therefore, a third-party organization would be best positioned to develop a library platform that supports all EDA formats, all new components of all vendors, and meet the design for manufacturing and assembly (DFMA) requirements of all ODM and OEM companies.

More importantly, only up-to-date, accurate, and reusable libraries can truly benefit design engineers working on different design lines and help companies save time and costs in the design process. The library platform that revolutionizes the industry must have the following features:

The platform is publicly accessible, allowing users to download libraries directly anywhere anytime.

Rapidly building highly accurate libraries, that not only align with generic parts information from spec datasheets, but also incorporate built-in DFMA rules into parts. This is crucial to customers of all tiers. Almost all tier-1 OEM/ODM companies require libraries to adhere to custom DFMA rules, mid-size companies need standardized DFMA to help them avoiding manufacturing issues, and small companies seek generic parts that follow IPC standards.

Offering on-demand access to libraries of the latest components. Simply having a large database of old libraries is not enough. Engineers use the latest components in their new designs and thus need up-to-date libraries. Relying on outdated libraries means engineers must manually adjust part drawings to accommodate differences between old and new specs and varying DFMA requirements. On-demand services can solve this issue.

Essentially, leveraging AI and automation technologies to support rapid on-demand services, eliminating the traditional manual part creation process. AI digitization technologies can extract necessary information from spec datasheets. The EDA library automation engine with programmable DFMA functions can encode spec data and DFMA rules for part creations.

Establishing a standardized library format that can fully describe both component specifications and DFMA rules. The format can transfer DFMA knowledge between EDA formats and be compatible with most EDA software. Then, the mentioned programmable DFMA functions supported by this DFMA-enriched format can code DFMA rules for rapid parts creation and modification.

MONDAY ENGINEERING TRACK POSTER RECEPTION

Time: 5:00 PM – 6:00 PM
Event Type: Engineering Track Posters
Room: Exhibit Hall, 2nd Floor

2.5D DESIGN BREAKTHROUGH: UNLEASHING THE POWER OF AUTOMATED EMIB BRIDGES.

Sam Mirza, Intel, San Francisco,

3DIC PROTOTYPE DESIGN AND TRANSIENT EARLY THERMAL ANALYSIS

Yongjin Hong, Kiwook Jung, Ki-Ok Kim, Byunghyun Lee, Sangyun Kim, Samsung, Seoul, South Korea

ACCELERATE RF BOARD BOM SIMULATION WITH ADS DESIGN AUTOMATION

Zhen Zhang, Shengkang Zhang, Keysight, Beijing, China; Tom Demuer, Keysight, Leuven, Belgium; Juneyi Peng, Keysight, Taipei, Taiwan;

ACCELERATING AUTOMATED CUSTOM LAYOUT CREATION THROUGH SMART DESIGN INTENT MIGRATION

Girish Vaidyanathan, Cadence Design Systems, Inc., Pulau Pinang, Malaysia; Sravasti Nair, Cadence Design Systems, Inc., San Jose, CA

ACHIEVING HIGH LOCAL NOISE COVERAGE IN DYNAMIC EMIR ANALYSIS USING SIGMADVD

Govind Pal, STMicroelectronics, Noida, India; Amit Jangra, Ansys, Bengaluru, India; Koshy John, Ansys, San Jose, CA

ADVANCED LLE AWARE TIMING SIGNOFF METHODOLOGY

Yoobeom Kim, Jingon Lee, Chul Rim, Hyunseung Seo, Samsung, Seoul, South Korea; Sangwoo Han, Tajendra Singh, Sunik Heo, Synopsys, Seoul, South Korea; Ahmed Shebaita, Li Ding, Synopsys, Santa Clara, CA;

ADVANCING LOW POWER DESIGN IN THE ERA OF RISING ENERGY FOOTPRINTS: INSIGHTS FROM IEEE 2416 STANDARD AND FUTURE EXTENSIONS

Nagu Dhanwada, IBM, Yorktown Heights, NY; Jerry Frenkil, Ali Sadigh, Leigh-Anne Clevenger, Si2, Inc., Austin, TX; W. Rhett Davis, North Carolina State University, Raleigh, NC; Daniel Cross, Cadence Design Systems, Inc., San Jose, CA; Akil Sutton, IBM, Yorktown Heights, NY;

AI-ASSISTED DESIGN OPTIMIZATION FOR EXTENSIVE DESIGN SPACES: HANDLING 260,000+ COMBINATIONS

Austin Rhodes, Micron, Boise, ID; Mohamed Atoua, Siemens, Austin, TX

AI-DRIVEN FRONTIERS IN ENERGY-EFFICIENT NEURAL PROCESSOR DESIGN

Vikas Chelani, Nitin Chawla, Manuj Ayodhyawasi, Harsh Rawat, Harshal Ambatkar, STMicroelectronics, Noida, India; Thomas Boesch, STMicroelectronics, Lugano, Switzerland, Giuseppe Desoli, STMicroelectronics, Torino, Italy

AREAL AND TIME DECOMPOSED PHALANX BASED DYNAMIC IR-DROP PREDICTION USING DNN(DEEP NEURAL NETWORK) AT EARLIER STAGE OF DESIGN CYCLE

Seihyung Jang, Gyusun Park, Kibum Kang, Yun Ra, Kisun Kim, Kisik Lee, Changsik Lee, Hongsok Choi, SK hynix, Seoul, South Korea; Taejin Kim, Cadence Design Systems, Inc., Hongpa Che, Dongchul Kang, Cadence Design Systems, Inc., Seoul, South Korea

AUTOMATED FLOORPLAN SCALING SOLUTIONS AND FRAMEWORK

Sivaramakrishnan Harihara Subramanian, Intel, Folsom, CA; Venkatesh RS, Intel, Bengaluru, India; Khris Valencia Chacon, Intel, San Jose, CA

AUTOMATED PLACE AND ROUTE BASED SOLUTION FOR CUSTOM BLOCKS

Rajeev Singh, Atul Bhargava, Vijay Singh Khati, STMicroelectronics Pvt. Ltd., Bengaluru, India; Akshita Bansal, Vishesh Kumar, Cadence Design Systems, Inc., Bengaluru, India;

BALANCING POWER AND PERFORMANCE: THE HYBRID CLOCK NETWORK APPROACH FOR NETWORK ON CHIPS

Pallapu Lakshmi Sarvaani, Indian Institute of Technology, Tirupati, India; Subba Annapalli, Ponnada Appala Naidu, Intel Technology India. Pvt. Ltd, Bengaluru, India

BUS DELAY SKEW MINIMIZATION FOR HIGH BANDWIDTH MEMORY DESIGNS

Kwangok Jeong, Seoklip Ki, Sua Kim, Samsung, Seoul, South Korea; Alpesh Kothari, Siemens, Raghu Gude, Jaejun Lee, JeongGuk Choi, Siemens, Seoul, South Korea

CALIBRE AUTOWAIVER FOR EARLY DRC & DFM ANALYSIS IN BIG DIE DESIGNS

Venkata Chinni, Rahul Agarwal, Samsung, Sruti L Shridhar, Samsung, Bengaluru, India

CDC SIMULATION CHECKER IMPLEMENTATION FOR CONSTANT AND QUASI-STATIC DATA PATHS

Youngchan Lee, Samsung, Seoul, South Korea

CHARTING UNCHARTED WATERS: FUNCTIONAL SIMULATION RESHAPING CDC/RDC CONSTRAINTS SIGNOFF

Suhas S, Deepmala Sachan, Ponsankar Arumugam, Ritesh Jain, Intel, Bengaluru, India

A CLOSED LOOP IR AND TIMING COMPREHENSIVE CO-SIGNOFF METHODOLOGY

Onkar Hule, Microsoft, Morrisville, NC; Rossana Liu, Microsoft, Austin, TX; Medha Kulkarni, Microsoft, Mountain View, CA; Hailang Wang, Microsoft, Mountain View, CA; Amit Garg, Microsoft, Bengaluru, India; Pranav Ranganathan, Microsoft, Mountain View, CA; Sreekanth Rajan, Ansys, San Jose, CA; Amit Jangra, Ansys, Bengaluru, India

COBRA : CODE COVERAGE MEASUREMENT TECHNIQUE FOR ARM-BASED FIRMWARE USING BINARY MODIFICATION TECHNOLOGY

wonchol kim, Samsung, Seoul, South Korea

MONDAY ENGINEERING TRACK POSTER RECEPTION (CONTINUED)

A DECADE OF EVOLUTION IN FORMAL VERIFICATION

Erik Seligman, Cadence Design Systems, Inc., Wichita, KS; M V Kiran Kumar, Intel, Bengaluru, India

DESIGN AUTOMATION OF MINIMAL LAYER COUNT MICROPROCESSOR 2.5D SILICON INTERPOSER

Omer Vikinski, Intel, Tel Aviv, Israel; Basil Tarabiea, Intel, Tel Aviv, Israel; Alexander Waizman, Intel, Sunnyvale, CA

DESIGN CLOSURE METHODOLOGY USING STAGE WISE CHECKERS BY EASE OF REVIEW TO MINIMIZE PHYSICAL DESIGN IMPLEMENTATION & CLOSURE TAT

Shilpi Srivastava, Daniel Hand, Jagadeesh Gnanasekaran, Intel Technologies India Private Ltd, Bengaluru, India

DESIGN ENABLEMENT OF 2D/3D POWER-THERMAL SELF-CONSISTENT ANALYSIS

Mohamed Naeim, Cadence Design Systems, Inc., Leuven, Belgium; Yun Dai, Dwaipayan Biswas, imec, Leuven, Belgium; Dragomir Milojevic, imec, Leuven, Belgium

THE DESIGNER'S SUPERPOWER! EARLY CIRCUIT VERIFICATION WITH CALIBRE NMLVS RECON

Kesmat Shahin, Siemens, Cairo, Egypt, Rahul Sai T Govindaswamy, Rajashekar Sura, Google, Mountain View, CA; Smitha Shivaji Kamathi, Siemens, Austin, TX; Anish Padhi, Gurpreet Singh Lamba, Siemens, Delhi, India; Rakesh Reddy, Karishma Qureshi, Google, Hyderabad, India;

DEVELOPING SOFTWARE TEST LIBRARY (STL) AS A SAFETY MECHANISM FOR VISION AI DSP

Noam Meser, Zvika Melamed, Ceva Technologies, Ltd., Tel Aviv, Israel; Sesha Sai Kumar C V, Ayman Mouallem, Fares Jaraisy, Optima Design Automation Ltd, Tel Aviv, Israel;

DIE-LEVEL DYNAMIC-IR ANALYSIS SHIFT-LEFT ENABLED BY REDHAWK-SC SIGMADVD

Ruiqi Wu, UNISOC, Shanghai, China; Ran Zhang, Ansys, Shanghai, China; Luca Cui, Ansys, Shanghai, China; Chang Zhao, Ansys, Shanghai, China; Marc Zheng, UNISOC, Shanghai, China

EARLY CLOCK TREE POWER ESTIMATION AND CORRELATION AT SOC: A CASE STUDY

Sri Sai Pavan Pasumarthi, Sudheer Yadapalli, Qualcomm, Bengaluru, India

AN EFFECTIVE METHOD OF EVALUATING CHIP POWER NOISE IN SYSTEM-LEVEL WITH ICPM

Chenxi Yang, Ping Ding, Feng Wu, Jiangtao Zhang, Jianguo Zhang, Keqing Ouyang, Sanechips Technology Co.,Ltd, Shenzhen, China Yongsheng Guo, Li Zou, Ansys, Shanghai, China;

EFFICIENT HBM CHANNEL DESIGN IN 2.5D SILICON INTERPOSER WITH SIGNAL INTEGRITY OPTIMIZATION

Feng Ling, Xpeedic, Shanghai, China; Yan Ma, Xpeedic, Shanghai, China

ELECTROMAGNETIC SOLUTIONS FROM DESIGN TO SIGN-OFF STAGE FOR HIGH-SPEED SERDES DESIGN

Yuhang Zhao, JinRong Yan, Hang Sun, Xuewei Ding, Sanechips Technology Co.,Ltd, Shenzhen, China; Xiaomei You, Rodger Luo, Garth Sundberg, Ansys, Shanghai, China;

EMPOWERING EARLY-STAGE DESIGN: AN AUTOMATED SOLUTION FOR DIE SIZE ESTIMATION AND IO RING CREATION

Gaurav Varshney, Dheeraj HA, Megha Naik, MuraliMohan Thota, Texas Instruments (India) Pvt. Ltd., Bengaluru, India

ENHANCED STATE-PROPAGATION BASED VECTORLESS IR-DROP ANALYSIS EMULATING REALISTIC SILICON BEHAVIOR

Subhadeep Ghosh, Rishabh Singh, Texas Instruments (India) Pvt. Ltd., Bengaluru, India; Ruchin Gupta, Sushant Sharma, Cadence Design Systems, Inc., Bengaluru, India

ENHANCING ANALOG MIXED-SIGNAL (AMS) VERIFICATION: ADVANCED METHODS FOR RUNTIME AND SCOPE OPTIMIZATION

Aadhar Sharma, Avinash Chaudhary, Sooraj Sekhar, Lakshmanan Balasubramanian, Texas Instruments (India) Pvt. Ltd., Bengaluru, India

EXECUTABLE TABLES, 'A JOURNEY FROM DOCUMENT TO SIMULATION CAPABLE, EXEMPLIFIED USING DDR5 '

Rahil Jha, Joseph Bauer, Cadence Design Systems, Inc., San Jose, CA;

FASTER TIMING CLOSURE OF MULTIPLE POWER DOMAINS BASED DESIGNS WITH SMVA

Rajnish Garg, Rohit Goel, STMicroelectronics Pvt. Ltd., Bengaluru, India

FORWARD PROGRESS TESTING: SAFTEY VS LIVENESS ASSERTION

Ankit Kumar Garg, NVIDIA, San Jose, CA

GLOBALIZED BULK BIASING BASED SUBSTRATE NOISE REDUCING METHOD FOR SIZE REDUCTION IN DIGITAL CIRCUIT

Changyeon Yu, Ahreum Kim, Pansuk Kwak, Dongku Kang, Samsung, Seoul, South Korea

HOLISTIC APPROACH ON 3DIC PLANNING

Venkata Chinni, Sruti L Shridhar, Tadasa Mahapatra, Sandeep Jadhav, Samsung, Bengaluru, India

AN INTEGRATED BEHAVIORAL MODELING METHOD FOR MIXED SIGNAL IPS

Bhupendra Singh, Rahul Kumar, Pallav Kumar, Jean-Aranud Francois, STMicroelectronics, Grenoble, France, Mitu Mittal, Anil Dwivedi, STMicroelectronics, Noida, India

LEVERAGING SEVERAL AUTOMATED TECHNIQUES AND METHODOLOGIES FOR FASTER COVERAGE CLOSURE AND DESIGN SIGN-OFF

Gulshan Sharma, Samsung, Bengaluru, India; Sougata Bhattacharjee, Samsung, Bengaluru, India

MONDAY ENGINEERING TRACK POSTER RECEPTION (CONTINUED)

MACHINE-LEARNING-DRIVEN FLOORPLAN-AWARE POWER DELIVERY NETWORK CO-PLANNING
Bogdan Tabacaru, Infineon Technologies AG, Munich, Germany, Jerome Toublanc, Ansys, Provence-Alpes-Côte d'Azur, France

MEMORY CLUSTERS – DIVIDE THE DESIGN AND OPTIMIZE MBIST INSERTION EFFORTS
Santhosh Ramappa, Subhash Baraiya, Marvell India Pvt. Ltd., Bengaluru, India

MEMORY INTERFACE ARCHITECTURES FOR TEST TIME REDUCTION IN ZERO DPPM SOCS
Nitesh Mishra, Hrithik Sahni, Texas Instruments, Bengaluru, India

METHODOLOGY OF LINKING THE LDR AND DRC CODE BY AUTOMATICALLY GENERATED TEST PATTERN
Dongjin Kim, Kwonjae Kim, Seyeon Moon, Boyoung Lee, Youngwook Kim, Jungyun Choi, Samsung, Seoul, South Korea

METHODOLOGY TO ANALYZE AND OPTIMIZE SOC PERFORMANCE AND COST USING FUNCTION AGNOSTIC CYCLE ACCURATE MODELS
Atul Lele, Anuvrat Srivastava, Ajeet Singh, Texas Instruments (India) Pvt. Ltd., Bengaluru, India; Ashutosh Mishra, Malaviya National Institute of Technology Jaipur, India

MICROSOFT'S COMPREHENSIVE IP HANDOFF FLOW
Martin Sanchez, Microsoft, Mountain View, CA; Siddharth Ravikumar, Siemens, Austin, TX;

MODELING OPTIMAL NUMBER OF TAP-POINTS FOR FLEXIBLE H-TREE DURING CLOCK TREE SYNTHESIS
Anup Kumar, Akshay Mankotia, Cadence Design Systems, Inc., Bengaluru, India

NOISE FIXUP: FINDING AND FIXING NOISE PROBLEMS (CHOP AND SWAP)
Adam Matheny, IBM, Yorktown Heights, NY

A NOVEL APPROACH TO COST-EFFICIENT HYBRID CLOUD SOLUTIONS WITH SEASCAPE'S DATA LAKE AND MICRO-RESILIENCY
Mohit Srivastava, Ajay Chopra, Arm Ltd., Bengaluru, India; Naveen B, Sankar Ramachandran, Sooraj JP, Vyom Garg, Ansys, Bengaluru, India

A NOVEL APPROACH TO IMPLEMENT FUSA FEATURE IN COMPLEX AUTOMOTIVE SOCS USING USF
Deepti Khurana, Manikanta Akula, NXP Semiconductors, Delhi, India

A NOVEL METHODOLOGY FOR LIBRARY CHARACTERIZATION AND MODELING CONSIDERING LOCAL LAYOUT EFFECT
Yoobeom Kim, Hyunseung Seo, CheolJun Bae, Jingon Lee, Chul Rim, Samsung, Seoul, South Korea; Edson Gomersall, Ramesh Kamath, Shupeng Cui, Mehar Gupta, Cadence Design Systems, Inc., San Jose, CA

A NOVEL METHODOLOGY FOR RE-SIMULATION OF BLOCK VECTORS HELPING VALIDATE POWER OPTIMIZATION QOR 20X FASTER
Bhupesh Prajapat, Parul Dohare, Pratik Talekar, Manish Kumar, Siemens, Delhi, India; Divya Parihar, Siemens, Toronto, Canada; Sachin Kumar, Mahima Jain, Mohammed Fahad, Siemens, Delhi, India

NOVEL WAY OF CHECKING AND ANALYZING PEAK TO PEAK VOLTAGE VARIATION CHALLENGES FOR HIGH COMPUTATIONAL MULTIPROCESSORS SOC
Amit Singh, Govind Pal, Anil Yadav, Amit Jangra, Ansys, Bengaluru, India; Koshy John, Ansys, San Jose, CA

ON CLOUD SECURED COLLABORATION FROM CHIPS TO EMBEDDED SYSTEMS
Smriti Joshi, Manuel Rei, Dassault Systèmes, Paris, France

OVERCOMING COLLABORATION HURDLES IN HIGH-TECH PRODUCT DEVELOPMENT WITH KEYSIGHT TOOL ON AZURE INFRASTRUCTURE
Amit Varde, Keysight Technologies; Joe Tostenrude, Microsoft

OVERCOMING THE GROWING CHALLENGE OF IR DROP BY EFFECTIVE POWER GRID ENHANCEMENT DURING CHIP FINISHING
Rahul Sai T Govindaswamy, Google, Mountain View, CA; Smitha Shivaji Kamathi, Ben Allen, Christian Miles, Jeff Wilson, Siemens, Austin, TX; Ravikanth Kosuru, Google, Hyderabad, India; Prateek Pendyala, Google, Taipei, Taiwan; Zvart Askanazyan, Siemens, Yerevan, Armenia, Heba Sharaf, Siemens, Cairo, Egypt, Esraa Swilliam, Siemens, Toronto, Canada; Gurpreet Lamba, Siemens, Delhi, India

PROGRAMMABLE IO RING BUILDER AND CHECKER
Manoj Kumar, Anurag Mittal, Praveen Jakki, Avinash Gupta, Priyanshi Jain, Priyanka Goel, Synopsys, Noida, India;

PNR IMPLEMENTATION CHALLENGES IN 3D IC
Arvind Kumar Mishra, Samsung, Bengaluru, India; choudhary Aditya Kumar, Samsung, Bengaluru, India; Jeshwanth Rahul, FDS SSIR, Hyderabad, India; Sandeep Jadhav, Samsung, Bengaluru, India

PREDICTING COMPUTER RESOURCE NEEDS USING MACHINE LEARNING AND CONVENTIONAL DESIGN
Justin Conklin, Marvell, Burlington, VT

QUALITY ASSURANCE OF DRC DECK FOR DEVICES BY SKILL AUTOMATION
Ambika Bhardwaj, Chirag Agarwal, Piyush Soni, STMicroelectronics, Noida, India; Kancou Traore, STMicroelectronics, Grenoble, France

RAPID RETARGETING OF FORMAL CONNECTIVITY VERIFICATION OF AI FPGA SYSTEMS
Linh Nguyen, Benjamin Ting, Microsoft, Nguyen Le, Microsoft, Mountain View, CA; Jin Hou, Rahul Seth, Sasa Stamenkovic, Siemens, Austin, TX

MONDAY ENGINEERING TRACK POSTER RECEPTION (CONTINUED)

REDEFINING HIERARCHICAL POWER INTEGRITY SIGNOFF FOR ULTRA-LARGE SYSTEM-ON-CHIPS

Piyush Jain, Rossana Liu, Hailang Wang, Apurva Soni, Medha Kulkarni, Pranav Ranganathan, Microsoft, Mountain View, CA; Chidambaram Rakkappan, Sreekanth Rajan, Ansys, Vancouver, Canada; Amit Jangra, Ansys, Bengaluru, India; Godwin Rajasekhar, Ansys, San Jose, CA;

REDUCING INTERLAYER MISALIGNMENT CAUSED BY BLE (BULK LAYOUT EFFECT) : SOLUTIONS FOR IMPROVING IN-CHIP UNIFORMITY OF ALIGNMENT BETWEEN TWO LAYERS

Hyejin Kim, Ohhun Kwon, Jichang Sim, Daehee Lee, Hyunmi Ji, Jooseong Lee, Samsung, Seoul, South Korea

A "SHIFT-LEFT" ANALYSIS FLOW FOR LAYOUT PARASITICS OF HIGH SPEED ANALOG MIXED SIGNAL DESIGN

Wei Wei, Yaping Huang, Jie Hu, Sanechips Technology Co.,Ltd, Shenzhen, China; Xiaomei You, Ansys, Carnegie, PA

SHIFT-LEFT METHODOLOGY TO IDENTIFY INVALID VOLTAGE LEVEL SHIFTS & VALIDATE SIGNAL PINS' P/G ASSOCIATION IN IPS/BLOCK'S UPF & .LIB VIEWS USING PERC'S STATIC-VOLTAGE TRACING MECHANISM

Sarvagya Tiwari, NXP Semiconductors, Delhi, India; GAZAL SINGLA, Siemens, Delhi, India; Shubham Sachdeva, NXP Semiconductors, Delhi, India

SHIFT-LEFT SOLUTION FOR ENHANCING POWER INTEGRITY IN PHYSICAL DESIGN CONSTRUCTION WITH REDHAWK-FUSION

Kiran Adhikari, Hailang Wang, Karthikk Sridharan, Rossana Liu, Microsoft, Mountain View, CA; Jin Wang, Synopsys, Sreekanth R, Godwin Rajasekhar, Ansys, San Jose, CA

SIGMADVD: HIGH COVERAGE SOLUTION FOR POWER INTEGRITY SIGNOFF

Anusha Vemuri, Emmanuel Chao, Santosh Santosh, NVIDIA, San Jose, CA; Chidambaram Rakkappan, Ansys, Vancouver, Canada; Ed Deeters, Ansys, San Jose, CA

A SINGLE SOURCE UNIFIED APPROACH TO CSR REGISTER DEVELOPMENT

Insaf Meliane, Arteris, Montigny-le-Bretonneux, France, Andy Nightingale,; Rich Weber, Arteris, Cambridge, MA

SMART TESTING: INTEGRATING FAULT SIMULATION AND AI/ML FOR EFFICIENT IP VALIDATION

Himanshu Vishwakarma, Priyanka Gharat; Gopi Srinivas Deepala, Silicon Interfaces, Bengaluru, India

SOLVING MEMORY SUBSYSTEM VERIFICATION CHALLENGES FOR MULTI-INSTANCE DESIGNS

Shyam Sharma, Manish Chand, Cadence Design Systems, Inc.

STRUCT BASED LOWER LEVEL MODELLING USING SYSTEMVERILOG UDT FOR VERIFICATION OF POWER MANAGEMENT IC

Vijay Kumar, Keerthana K, Celeste Anil Lagali, Samsung

SYSTEMATIC FLOW ON AC SCAN TIMING/ATPG CONSTRAINT GENERATION

Chen Yuan Kao, Yi Hsuan Chiu, Global UniChip Corp., Taipei, Taiwan

SYSTEMATIC VERIFICATION FRAMEWORK FOR MEMORY SUBSYSTEM ENSURING RELIABILITY AND ROBUSTNESS

Vatsal Patel, Pooja Patel, Dharini SubashChandran, Cadence Design Systems, Inc., Ritesh Desai, Pratibha Sukhija, Cadence Design Systems, Inc., Bengaluru, India;

TIMING CLOSURE METHODS ON 5NM DESIGN CHALLENGES

Patricia Fong, Marvell, Cupertino, CA

UNIFIED WAVEFORM ANALYSIS PLATFORM FOR TR.-LEVEL DESIGN VERIFICATION

Choi Wonwoo, Kwangsun Kim, Sungho Park, Hyungjung Seo, Younsik Park, Jungyun Choi, Samsung

SYSTEMS FOUNTRY – A JOURNEY FROM 'SYSTEM ON A CHIP' TO 'SYSTEM OF CHIPS'

Time: 8:45 AM – 9:45 AM
Session Type: Keynote
Room: 3007, 3rd Floor

Speaker: Gary Patton, Intel

Description: In this keynote, Dr. Gary Patton will introduce the fundamental concepts driving the vision of a 'Systems Foundry', including a standards-based approach to assemble heterogenous dies. Dr. Patton will also cover the factors driving the inevitable need for disaggregation; factors like reticle limit, thermal constraints, cost, yield, etc., among others that are especially exacerbated in the need to satisfy the demands of HPC designs in the AI era. In addition, Dr. Patton will go over the transformative journey at Intel over the last 4-5 years that has helped orient the execution towards enabling the vision of a Systems Foundry. A journey that encompasses delivering to a full breadth of EDA offerings and development of advanced packaging capabilities, to name a few. The work is not done, however; the EDA & IP ecosystem has a vital role to play in this vision - to enable a seamless 3DIC design platform for advanced packaging implementation & modeling, AI-driven 3D exploration and System-Technology Co-Optimization while tackling challenges in the multi-physics domain. Intel has several collaborative projects with EDA to address these challenges, and Dr. Patton will end with a call to action to the ecosystem partners on continued partnership to realize this vision.

DESIGNING AN ASIC FOR THE GENERATIVE AI ERA

Time: 10:15am – 11:00am
Session Type: Analyst Presentation
Topic: AI
Room: DAC Pavilion, Level 2 Exhibit Hall

Description: The presentation will cover what is required to design an ASIC for the Generative AI Era. It will cover the compute, networking, and memory constraints of generative AI as well as what companies are doing to push beyond it with optics, packaging, and system level design.

Presenters: Dylan Patel, SemiAnalysis

ARCHITECTING A TRUE HYBRID CLOUD ENVIRONMENT FOR MASSIVELY PARALLELIZED EDA WORKLOADS

Time: 10:30 AM – 11:00 AM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Bursting EDA workloads from on-prem to cloud is a challenge for most on-prem environments that are increasingly running out of capacity due to the growing complexity of advanced-node designs. For massively parallelized workloads, such as library characterization, implementation and physical verification, engineers currently need to split their designs between on-prem and cloud execution if they want to leverage the scalable compute capacity on cloud. Depending on the design, this is a tedious activity that eats away at precious engineering productivity. And once job execution is complete, the process to transfer output data back from cloud to on-prem and aggregate it with output generated on-prem adds to this overhead. In this session, we will discuss a unique approach to enabling a true hybrid cloud environment architected specifically for EDA workloads which enables engineers to submit a large job exclusively on-prem automatically splitting the job, routing selective worker traffic through a secure network for cloud execution, and syncing data generated on cloud back to on-prem storage for further processing in the flow. Along with license management automation, hybrid cloud optimization can radically improve engineering productivity and enhance the coverall cloud experience for SoC design.

Presenter: Sridhar Panchapakesan, Synopsys; Vikram Bhatia, Synopsys

THERMO-ELECTRICAL ANALYSIS AND SIGNOFF ENGAGEMENT FOR ROBUST PERFORMANCE

Time: 10:30 AM – 12:00 PM
Session Type: Engineering Tracks
Topic Area(s): Back-End Design
Room: 2008, 2nd Floor

Session Chairs: Amol Joshi (Independent)

Description: Deliver a successful solution teaser by learning about ways to model the double helix of thermo-electric impacts on system design closure for timing, power supply delivery and test

- **A Methodology to Predict IR Drop Enhancement in BSPDN Compared to FSPDN by Formulating the On-Die IR Drop**
  Dean Huang, Odie Ou, Intel, Taipei, Taiwan; Andy Wei, Hank Wang, Intel, Hillsboro, OR;
- **Parasitic Leakage Detection in Layout Design**
  Dongseok Shin, Kiyoung Moon, Hyein Lee, Seongjin Mun, Seyoung Kim, Jung Yun Choi, Seongpil Chang, Se-Hoon Lee, Junhee Lim, Samsung Electronics, Seoul, South Korea; Sunsoo Byun, Siemens, Hwaseong-si, South Korea;
- **Efficient Representation of Cross Current Effects in Contributor-based Power Models**
  Spandana R, Arun Joseph, Rahul Rao, IBM, Bengaluru, India; Nagu Dhanwada, IBM, Fishkill, NY;
- **Timing Robustness: A Way Forward for Analyzing Timing-voltage Sensitive Paths for Accounting IR-Drop Variations**
  Shourya Shukla, Lavanya Padmanabhuni, Sainarayanan Suryanarayanan, Marvell, Bengaluru, India; Harshit Jaiswal, Sharath AC, Cadence Design Systems, Inc., Bengaluru, India; Nitin Jain, Cadence Design Systems, Inc., Montbonnot-Saint-Martin, France;
- **Reducing Test Dynamic IR and Vmin for Automotive and Industrial Radar SoCs using Power Aware DFT Methodology**
  Nitesh Mishra, Rupesh Lad, Hrithik Sahni, Texas Instruments (India) Pvt. Ltd., Bengaluru, India;
- **Automated Workflow for Comprehensive Thermal Analysis of IC Package Designs**
  Sharath C R, Senthil Kumar Sundaramoorthy, Texas Instruments, Bengaluru, India; Siva Gurrum, Blake Travis, Texas Instruments, Allen, TX

METHODOLOGIES FOR STREAMLINING SOC DESIGN CHALLENGES

Time: 10:30 AM – 12:00 PM
Session Type: Engineering Tracks
Topic Area(s): IP
Room: 2010, 2nd Floor

Session Chair: Nanditha Rao, Indian Institute of Information Technology

Description: SoC design poses several challenges in terms of design flow and methodologies. The use of advanced and automated methods is crucial, especially for compute-intensive workloads. This session presents various topics on design methodologies such as: accelerating placement-aware timing closure for NOCs, an open-source design flow promising support for generative AI, accelerating DRC checks, CDC multimode signoff methodology, droop mitigation and scalable sign-off/QA flow.

- **Advancing Power Signoff for High Speed ΔΣADC**
  Vaibhav Garg, Paras Garg, Atul Bhargava, STMicroelectronics, Noida, India; Prayes Jain, Cadence Design Systems, Inc., Noida, India;
- **Considering Selective Resistance Extraction for Performance & Accuracy Trade-off for Memory IP Simulation**
  Praveen Kumar Verma, Anuj Dhillon, Harshit Sharma, Vartul Sharma, Rakesh Shenoy, Ashish Kumar;
- **Fast and Deterministic Memory Yield Estimation Using Machine Learning Augmented Statistical Simulations**
  Ashish Kumar, Shashank Gupta, STMicroelectronics Pvt. Ltd., Noida, India; Rakesh Shenoy, Synopsys, Bengaluru, India;
- **Low-Cost Built In Self Test IP for Nextgen Continuous Time Sigma Delta ADCs**
  Ankur Bal, Sharad Gupta, Vaibhav Garg, STMicroelectronics, Noida, India;
- **An All-Digital Transient Filter IP for Serial Links**
  Ankur Bal, Aradhana Kumari, STMicroelectronics, Noida, India;
- **Interfacing High-Voltages Directly to Low Power CMOS Process Die for RF, MEMs and Analog Applications**
  Stephen Fairbanks, Certus, Queen Creek, AZ; Pradeep Thiagarajan, Siemens, Raleigh, NC; Lih-Jen Hou, Siemens, Santa Clara, CA

THE OPEN CHIPLET ECONOMY AND AI

Time: 10:30 AM – 12:00 PM
Session Type: Engineering Tracks
Topic Area(s): IP
Room: 2010, 2nd Floor

Organizers: Bapi Vinnakota, Open Compute Project, San Jose, CA

Description: The Open Chiplet Economy and AI: A brief introduction of how the open chiplet economy can help with AI - Bapi Vinnakota (OCP), Cliff Grossner (OCP); A Survey of AI-related IP for the Open Chiplet Economy - High performance D2D PHY IP and Other soft IP relevant to AI - Elad Alon (Blue Cheetah) Letizia Giuliano (Alphawave); AI-Related Chiplets in the Open Chiplet Economy: An overview of chiplets relevant to building AI and HPC systems; John Shalf (LBL); AI Packaging Workflow: Basic and advanced packaging workflows for AI systems, Lihong Cao (ASE) +

Presenters: Bapi Vinnakota, Open Compute Project, San Jose, CA; Cliff Grossner, OCP, Ottawa, ON, Canada; Letizia Giuliano, Alphawave, Portland, OR; John Shalf, NERSC, Berkeley, CA; Lihong Cao, ASE Holdings, Austin, TX; Elad Alon, Blue Cheetah Analog, Berkeley, CA

ADVANCED IN SILICON LIFECYCLE MANAGEMENT & TEST

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): EDA
Room: 3010, 3rd Floor

Session Chair: Jon Colburn (Synopsys)

Description: This session covers a wide range of silicon health challenges and proposes advanced solutions to address them. These include accurate Vmin prediction for better reliability; fault analysis for functional safety; green FPGAs for environmental sustainability; novel ATPG algorithms for neuromorphic chips; improving reliability of AI accelerators; and finally learning-based ATPG for higher quality and yield.

- **Data-Efficient Conformalized Interval Prediction of Minimum Operating Voltage Capturing Process Variations**
  Yuyuan Yin, Peng Li, University of California, Santa Barbara, CA; Rebecca Chen, Chen He, NXP Semiconductors, Austin, TX;
- **MENDNet: Just-in-time Fault Detection and Mitigation in AI Systems with Uncertainty Quantification and Multi-Exit Networks**
  Shamik Kundu, Mirazul Haque, Sanjay Das, Wei Yang, Kanad Basu, The University of Texas at Dallas, Richardson, TX;
- **Low-Complexity Algorithmic Test Generation for Neuromorphic Chips**
  Hsu-Yu Huang, Chu-Yun Hsiao, Tsung-Te Liu, James Li, National Taiwan University, Taipei, Taiwan;
- **GreenFPGA: Evaluating FPGAs as Environmentally Sustainable Computing Solutions**
  Chetan Choppali Sudarshan, Aman Arora, Vidya A. Chhabria, Arizona State University, Tempe, AZ;
- **SmartATPG: A Learning-based Automatic Test Pattern Generation with Graph Convolutional Network and Reinforcement Learning**
  Wenxing Li, Hongqin Lyu, Shengwen Liang, Tiancheng Wang, Huawei Li, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China;
- **Graph Learning-based Fault Criticality Analysis for Enhancing Functional Safety of E/E Systems**
  Sanjay Das, Shamik Kundu, Kanad Basu, The University of Texas at Dallas, Richardson, TX; Pooja Madhusoodhanan, Prasanth Viswanathan Pillai, Rubin Parekhji, Texas Instruments, Bengaluru, India; Arnab Raha, Intel, Santa Clara, CA; Suvadeep Banerjee, Suriya Natarajan, Intel, Santa Clara, CA

CHARTING A COURSE TO NAVIGATE IRREGULAR DATA ACCESS IN GRAPH NEURAL NETWORKS AND BEYOND!

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): AI
Room: 3003, 3rd Floor

Session Chairs: Andrey Ayupov (Google); Subhendu ROY (Cadence)

Description: This session presents state-of-the-art research in architecture design focusing on tackling irregular data access problems incurred in graph neural networks and accelerator architectures. One presentation deals with a Video Frame Interpolation accelerator whose energy efficiency surpasses a RTX 4090 GPU. The second half of the session offers a slew of Graph Neural Network (GNN) centric accelerators, dealing with the common irregular data access issues encountered in these GNNs.

- **DEFA: Efficient Deformable Attention Acceleration via Pruning-Assisted Grid-Sampling and Multi-Scale Parallel Processing**
  Yansong Xu, Dongxu Lyu, Zhenyu Li, Yuzhou Chen, Zilong Wang, Gang Wang, Zhican Wang, Haomin Li, Guanghui He, Shanghai Jiao Tong University, Shanghai, China;
- **Co-Via: A Video Frame Interpolation Accelerator Exploiting Codec Information Reuse**
  Haishuang Fan, Qichu Sun, Jingya Wu, Wenyan Lu, Xiaowei Li, Guihai Yan, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China;
- **GDR-HGNN: A Heterogeneous Graph Neural Networks Accelerator with Graph Decoupling and Recouping**
  Runzhen Xue, Dengke Han, Yihan Teng, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Mingyu Yan, Zhimin Tang, Xiaochun Ye, Dongrui Fan, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China;
- **SC-GNN: A Communication-Efficient Semantic Compression for Distributed Training of GNNs**
  Jihe Wang, Ying Wu, Danghui Wang, Northwestern Polytechnical University, Xi'an, China;
- **CDA-GNN: A Chain-driven Accelerator for Efficient Asynchronous Graph Neural Network**
  Hui Yu, Yu Zhang, Donghao He, Qikun Li, Jin Zhao, Xiaofei Liao, Hai Jin, Lin Gu, Haikun Liu, Huazhong University of Science and Technology, Wuhan, China;Ligang He, University of Warwick, Wolverhampton, United Kingdom;
- **RTGA: A Redundancy-free Accelerator for High-Performance Temporal Graph Neural Network Inference**
  Hui Yu, Yu Zhang, Andong Tan, Chenze Lu, Jin Zhao, Xiaofei Liao, Hai Jin, Haikun Liu, Huazhong University of Science and Technology, Wuhan, China

EDGEVOLUTION: TRANSFORMING EDGE COMPUTING PARADIGMS

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): Embedded Systems
Room: 3008, 3rd Floor

Session Chairs: Jingtong Hu (University of Pittsburgh); Pi-Cheng Hsiu (Academic Sinica)

Description: "Edgevolution" presents cutting-edge research driving the evolution of edge computing paradigms. Papers in this session present innovative solutions such as accelerating Simulink model simulations via code generation, parallelizing SystemC TLM-2.0 CPU models for high-performance virtual platforms, and maximizing accuracy in FinFET-based real-time computing. Additionally, the session introduces emerging applications, including collaborative user-driven recommendation systems for edge devices, on-device LLM personalization with selective synthetic data, and a physics-guided generative AI toolkit for geophysical monitoring on edge devices. These contributions collectively propel the advancement of edge computing, offering transformative solutions for enhanced acceleration and intelligence at the edge.

- **AccMoS: Accelerating Model Simulation for Simulink via Code Generation**
  Yifan Cheng, Ting Chen, Xiaosong Zhang, University of Electronic Science and Technology of China, Chengdu, China; Zehong Yu, Zhuo Su, Yu Jiang, Tsinghua University, Beijing, China;
- **Towards High-Performance Virtual Platforms: A Parallelization Strategy for SystemC TLM-2.0 CPU Models**
  Nils Bosbach, Niko Zurstraassen, Rebecca Pelke, Rainer Leupers, RWTH Aachen University, Aachen, Germany; Lukas Junger, Jan Weinstock, MachineWare GmbH, Aachen, Germany;
- **MAFin: Maximizing Accuracy in FinFET based Approximated Real-Time Computing**
  Shounak Chakraborty, Magnus Sjalander, Norwegian University of Science and Technology, Trondheim, Norway; Sangeet Saha, Klaus McDonald-Maier, University of Essex, United Kingdom;
- **Duet: A Collaborative User Driven Recommendation System for Edge Devices**
  Vidushi Goyal, Valeria Bertacco, Reetuparna Das, University of Michigan, Ann Arbor, MI;
- **Enabling On-Device Self-Supervised LLM Personalization with Selective Synthetic Data**
  Ruiyang Qin, Jun Xia, Zhenge Jia, Meng Jiang, Ahmed Abbasi, Yiyu Shi, University of Notre Dame, South Bend, IN; Peipei Zhou, Jingtong Hu, University of Pittsburgh, PA;
- **EdGeo: A Physics-guided Generative AI Toolkit for Geophysical Monitoring on Edge Devices**
  Junhuan Yang, Yi Sheng, Lei Yang, George Mason University, Fairfax, VA; Hanchen Wang, Los Alamos National Laboratory, Los Alamos, NM; Youzuo Lin, University of North Carolina, Chapel Hill, Chapel Hill, NC

EMPOWERING EDGE INTELLIGENCE: WHEN IOT DEVICES MEET AI

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): AI
Room: 3001, 3rd Floor

Session Chairs: Hongyang Jia (Tsinghua University); Grace Li Zhang (Technische Universit at Darmstadt)

Description: Real-life application scenarios raise three important demands on IoT devices: higher accuracy (smarter), higher performance (faster), and lower resource consumption (more efficient). This session explores the hardware-software co-optimization of intelligent algorithms for diverse IoT devices and application scenarios, making IoT devices smarter, faster, and more efficient. The papers address low-power data processing on edge devices, Processing-In-Memory architecture design, real-time DNN scheduling on MCUs, and a practical deployment of learning-based Heating, Ventilation, and Air Conditioning (HVAC) controllers.

- **Graph Neural Networks Automated Design and Deployment on Device-Edge Co-Inference Systems**
  Ao Zhou, Jianlei Yang, Tong Qiao, Yingjie Qi, Weisheng Zhao, Chunming Hu, Beihang University, Beijing, China; Zhi Yang, Peking University, Beijing, China;
- **LEAF: An Adaptation Framework against Noisy Data on Edge through Ultra Low-Cost Training**
  Zihan Xia, Mingu Kang, University of California, San Diego, CA;Jinwook Kim, SK hynix, Icheon, South Korea;
- **Deep Harmonic Finesse: Signal Separation in Wearable Systems with Limited Data**
  Mahya Saffarpour, Weitai Qian, Kourosh Vali, Begum Kasap, Herman Hedriana, Soheil Ghiasi, University of California, Davis, CA;
- **EPIM: Efficient Processing-In-Memory Accelerators based on Epitome**
  Chenyu Wang, Princeton University, Princeton, NJ; Zhen Dong, Kurt Keutzer, University of California, Berkeley, CA; Daquan Zhou, Jiashi Feng, ByteDance Inc., Singapore, Singapore; Zhenhua Zhu, Yu Wang, Tsinghua University, Beijing, China;
- **RT-MDM: Real-Time Scheduling Framework for Multi-DNN on MCU Using External Memory**
  Sukmin Kang, Seongtae Lee, Hyunwoo Koo, Jinkyu Lee, Sungkyunkwan University, Suwon-si, South Korea; Hoon Sung Chwa, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea;
- **Go Beyond Black-box Policies: Rethinking the Design of Learning Agent for Interpretable and Verifiable HVAC Control**
  Zhiyu An, Xianzhong Ding, Wan Du, University of California, Merced, CA

GETTING REAL IN REAL-TIME

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): Embedded Systems
Room: 3012, 3rd Floor

Session Chair: Corey Tessler (University of Nevada Las Vegas)

Description: Multimodal transformers get real-time performance boost using PIM-GPU collaboration. What's more, DNN inference tasks can be modeled as sporadic non-preemptive gang tasks. For parallel real-time applications on SoCs, an extra cache layer shared by a cluster improves latency. To protect CNNs, algorithm-based comprehensive fault tolerance can be used to "maintain sanity". Analysis of NN layers reveals that faults transitioning from 0 to 1 significantly impact classification outcomes. From the networking side, a real-time TSN end station design enables ultra-low latency and nanosecond-level transmission accuracy.

- **A Real-time Execution System of Multimodal Transformer through PIM-GPU Collaboration**
  Shengyi Ji, Chubo Liu, Yan Ding, Zhuo Tang, Hunan University, Changsha, China; Qing Liao, Harbin Institute of Technology, Shenzhen, China;
- **A Cache/Algorithm Co-design for Parallel Real-Time Systems with Data Dependency on Multi/Many-core System-on-Chips**
  Zhe Jiang, Southeast University, Nanjing, China; Shuai Zhao, Yiyang Gao, Sun Yat-Sen University, Guangzhou, China; Ran Wei, University of Cambridge, United Kingdom; Jing Li, New Jersey Institute of Technology, Newark, NJ;
- **Partitioned Scheduling and Parallelism Assignment for Real-Time DNN Inference Tasks on Multi-TPU**
  Binqi Sun, Marco Caccamo, Technical University of Munich, Germany;Tomasz Kloda, LAAS-CNRS, Toulouse, France; Chu-ge Wu, Beijing Institute of Technology, Beijing, China;
- **Maintaining Sanity: Algorithm-based Comprehensive Fault Tolerance for CNNs**
  Jinhyo Jung, Woobin Ko, Yebon Kim, Yohan Ko, Kyoungwoo Lee, Yonsei University, Seoul, South Korea; Hwisoo So, Sumedh Joshi, Aviral Shrivastava, Arizona State University, Tempe, AZ;
- **HTAG-eNN: Hardening Technique with AND Gates for Embedded Neural Networks**
  Wilfread Guilleme, INRIA, Rennes, France; Angeliki Kritikakou, Daniel Chillet, Universite de Rennes, France; Youri Helen, DGA MI, Bruz, France; Cedric Killian, Universite Jean Monnet, Saint-Etienne, France;
- **Towards Cost-Effective High-Throughput End Station Design for Time-Sensitive Networking (TSN)**
  Chuanyu Xue, Tianyu Zhang, Song Han, University of Connecticut, Storrs, CT

RACING AGAINST TIME: INNOVATIONS IN TIMING

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): EDA
Room: 3008, 3rd Floor

Session Chairs: Yibo Lin (Peking University); Qi Sun (Zhejiang University)

Description: This session showcases breakthroughs in timing, from timing prediction and analysis to its application. It begins with novel methods for timing prediction, moves through significant advancements in GPU-accelerated static timing analysis for rapid verification, introduces efficient techniques for critical path selection, and concludes with statistical modeling for yield estimation. This session encapsulates the forefront of timing, promising to elevate design accuracy and speed in the semiconductor industry.

- **Annotating Slack Directly on Your Verilog: Fine-Grained RTL Timing Evaluation for Early Optimization**
  Wenji Fang, Shang Liu, Hongce Zhang, Zhiyao Xie, Hong Kong University of Science and Technology, Hong Kong;
- **Disentangle, Align and Generalize: Learning A Timing Predictor from Different Technology Nodes**
  Xinyun Zhang, Binwu Zhu, Fangzhou Liu, Ziyi Wang, Peng Xu, Bei Yu, The Chinese University of Hong Kong; Hong Xu, City University of Hong Kong, Shatin, Hong Kong;
- **GCS-Timer: GPU-Accelerated Current Source Model Based Static Timing Analysis**
  Shiju Lin, Evangeline Young, Martin Wong, The Chinese University of Hong Kong, Hong Kong; Guannan Guo, University of Illinois at Urbana-Champaign, Champaign, IL; Tsung-Wei Huang, University of Wisconsin, Madison, WI; Weihua Sheng, Huawei, Hong Kong;
- **G-PASTA: GPU Accelerated Partitioning Algorithm for Static Timing Analysis**
  Boyang Zhang, University of Wisconsin, Madison, WI; Dian-Lun Lin, Che Chang, Cheng-Hsiang Chiu, Wan Luan Lee, Chih-Chun Chang, Tsung-Wei Huang, University of Wisconsin, Madison, WI; Bojue Wang, Rutgers University, Piscataway, NJ; Donghao Fang, Texas A&M University, College Station, TX;
- **Ink: Efficient Incremental k-Critical Path Generation**
  Che Chang, Tsung-Wei Huang, Dian-Lun Lin, University of Wisconsin, Madison, WI; Guannan Guo, University of Illinois at Urbana-Champaign, Champaign, IL; Shiju Lin, The Chinese University of Hong Kong, Hong Kong;
- **LVF2: A Statistical Timing Model based on Gaussian Mixture for Yield Estimation and Speed Binning**
  Junzhuo Zhou, University of California, Los Angeles, CA; Li Huang, Haoxuan Xia, University of Nottingham Ningbo China, Ningbo, China; Yihui Cai, Leilei Jin, Xiao Shi, Southeast University, Nanjing, China; Wei Xing, Lei He, Eastern Institute of Technology, Ningbo, China; Ting-Jung Lin, Ningbo Institute of Digital Twin, Eastern Institute of Technology / UNNC, Ningbo, China

TRANSFORMING TRANSFORMERS: ACCELERATING TRANSFORMER MODELS FOR VIT AND LLMS

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3002, 3rd Floor

Session Chair: Liu Ke (Tenstorrent), Ramtin Zand (University of South Carolina)

Description: The success of transformer models has been demonstrated across various ML-based services in the fields of natural language processing, computer vision, video processing, etc. Such versatile applications also introduce challenges stemming from their vast demand for computation, memory capacity, and memory bandwidth, alongside concerns regarding their implications for energy consumption and potential model misuse. This session presents technical solutions and scientific advancements through behavioral analysis of input tokens, novel quantization algorithms, hardware architecture techniques, and hardware-software co-design. The discussions aim to tackle the pressing issues faced by transformer models, making their operations more practical and efficient for real-world applications.

- **InterArch: Video Transformer Acceleration via Inter-Feature Deduplication with Cube-based Dataflow**
  Xuhang Wang, Zhuoran Song, Xiaoyao Liang, Shanghai Jiao Tong University, Shanghai, China;
- **TSAcc: An Efficient \underline{T}empo-\underline{S}patial Similarity Aware \underline{Acc}elerator for Attention Acceleration**
  Zhuoran Song, Chunyu Qi, Yuanzheng Yao, Xiaoyao Liang, Shanghai Jiao Tong University, Shanghai, China; Peng Zhou, Yanyi Zi, Nan Wang, Alibaba Group, Beijing, China;
- **QUQ: Quadruplet Uniform Quantization for Efficient Vision Transformer Inference**
  Xinkuang Geng, Honglan Jiang, Shanghai Jiao Tong University, Shanghai, China; Siting Liu, Shanghai Tech University, Shanghai, China; Leibo Liu, Tsinghua University, Beijing, China; Jie Han, University of Alberta, Edmonton, AB, Canada;
- **LLM-MARK: A Computing Framework on Efficient Watermarking of Large Language Models for Authentic Use of Generative AI at Local Devices**
  Shiyu Guo, Yuhao Ju, Xi Chen, Jie Gu, Northwestern University, Evanston, IL;
- **VITA: ViT Acceleration for Efficient 3D Human Mesh Recovery via Hardware-Algorithm Co-Design**
  Shilin Tian, Chase SzafranskiCe Zheng, Fan Yao, Chen Chen, Hao Zheng, University of Central Florida, Orlando, FL; Ahmed Louri, George Washington University, Washinton, DC;
- **OPAL: Outlier-Preserved Microscaling Quantization Accelerator for Generative Large Language Models**
  Dahoon Park, , Jaeha Kung, Korea University, Seoul, South Korea; Jahyun Koo, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea; Sangwoo Jung

QUANTUM COMPUTING: ACCOMPLISHMENTS, BOTTLENECKS, AND TIMELINES

Time: 10:30 AM – 12:00 PM
Session Type: Design
Topic Area(s): Research Panel
Room: 3014, 3rd Floor

Organizers: Robert Wille, Technical University Munich, Germany

Moderator: Robert Wille, Technical University Munich, Germany

Description: Quantum computers are a reality! In the recent years, the technology received a huge momentum fueled by numerous players (including established companies, an impressive number of start-ups, and plenty of research initiatives) who are working on the realization of corresponding machines, design flows, and applications. At the same time, however, there are still several questions: End-users and domain experts wonder for what applications quantum computing will be interesting (and when)? Designers and tool developers wonder what (physical) challenges and bottlenecks have to be addressed. And physicists wonder how they can address all these expectations while, at the same time, they are still trying to get decoherence times and errors under control

Hence, it is time for a discussion about where we are with quantum computing? To this end, this panel brings renowned panelists from industry and academia together to discuss the current status and future promise of this technology, from different perspectives. More precisely, we are going to cover:

- How should we assess the recent accomplishments in the different technologies (superconducting, ion-traps, neutral atoms, etc.)? Which technology is most promising? Are those just another step in a still long series of further steps needed or do they constitute the eventual breakthrough?
- What bottlenecks still have to be overcome: Can we re-use the established design flow for classical circuits and systems for quantum computing? How much quantum physics expertise is needed to work in that field? Do we have metrics/benchmarks that can guide us through the corresponding developments
- What are the practically relevant ecosystems? Will quantum computing replace conventional systems in entire fields or "only" extend the conventional computational capacities? Will there be "stand-alone" quantum computing applications or only quantum-classical co-design solutions?
- What are the timelines towards practically relevant quantum computing ecosystems.

In addition, the panelists will also be available to address dedicated questions from the design automation community. This and more will be covered in the panel

Panelists: Leon Stok, IBM, Mount Kisco, NY; Brad Lackey, Microsoft, Seattle, WA; Matthew Harrigan, Google, Mountain View, CA; Jamil Kawa, Synopsys, Mountain View, CA; Nadia Haider, Technische Universitat Delft, Netherlands

EDA FOR HETEROGENEOUS INTEGRATION: WHAT LIES AHEAD?

Time: 10:30 AM – 12:00 PM
Event Type: Special Session (Research)
Topic Area(s): EDA
Room: 3006, 3rd Floor

Session Chair: Iris Hui-Ru Jiang, National Taiwan University

Organizer: Tsung-Yi Ho, The Chinese University of Hong Kong; Chih-Ping Hung, Advanced Semiconductor Engineering

Description: Heterogeneous integration poses new challenges to electronic design automation (EDA) and packaging communities and demands innovative solutions that must be built together with tight-knit collaborations. This special session is focused on design, automation, and thermal management aspects of heterogeneous integration. These very important aspects are not very well explored and covered by the mainstream research on physical design and packaging, as presented in the regular paper tracks. Attendees will learn about exciting developments at the intersection of design automation, manufacturing, and architecture on heterogeneous integration. Attendees will also be presented with a set of design and integration challenges that lie ahead, as well as current state-of-the-art solutions to these problems.

- **Physical Design for Heterogeneous Integration: Challenges and Solutions**
  Yao-Wen Chang, National Taiwan University, Taipei, Taiwan;
- **The Role of EDA as Chips Transform Into 3D Systems**
  John Park, Cadence Design Systems, Inc., Boulder, CO;
- **Thermal Design and Management for Heterogeneous Integration**
  Tiwei Wei, Purdue University, West Lafayette, IN

STREAMLINING DESIGN COMPLEXITY WITH IP-CENTRIC DESIGN

Time: 11:15 AM – 11:45 AM
Event Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Semiconductor design complexity has increased exponentially in recent years. Teams have gone from building relatively simple designs across a handful of design centers to building platforms of staggering complexity across multiple, geographically dispersed, integrated design centers. Meanwhile, time to market pressures continue to intensify.

To face these challenges, organizations must increase efficiency across all aspects of the design lifecycle. One effective way to do this is through the Transformation Model for IP-Centric Design: a blueprint for improving IP reuse, end-to-end traceability, and collaboration at enterprise scale.

Currently, most teams employ a traditional, project-centric, "copy-and-modify" design methodology. While this approach worked well when projects and teams were smaller, today the inefficiencies of project-centric design are clear. Projects are siloed, so teams end up re-solving the same problems and manually tracking IP, project-by-project. This lack of centralized coordination makes it difficult to pool resources, meet compliance requirements, or scale design and development.

This is where an IP-centric design methodology comes into play.

IP-centric design creates a centralized system for design management across varied projects, cross-functional teams, and globally dispersed design centers. By transitioning to an IP-centric design methodology, organizations can achieve the goal of a streamlined, fully traceable, horizontally scaling, single source of truth for all design management needs across hardware, firmware, and software projects and platforms. The benefits include improved collaboration, accelerated design, more informed build vs. buy decisions, and a streamlining of efforts across design teams.

Presenters: Vishal Moondhra, Perforce Software

THE EVOLUTION OF THE DIGITAL TWIN FOR SEMICONDUCTOR AND HOW AI WILL EXPAND MANUFACTURING AWARE DESIGN

Time: 11:15 AM – 12:00 PM
Session Type: TechTalk
Room: DAC Pavilion, Level 2 Exhibit Hall

Description: Depending on who you talk with the Digital Twin is either the newest thing in semiconductor, or something that semiconductor has always had. The truth is that both are true. Semiconductor has long relied on domain specific Digital Twins of different aspects of the design in order to design, test, and integrate in the virtual world before committing to manufacture. Starting with the Siemens acquisition of EDA, but now being talked about more widely, we now talk about the Comprehensive Digital Twin of the design, which attempts to more completely capture the design and allow analysis using not only traditional EDA but also Multiphysics. This is just the beginning however, as we are already moving towards the merging of the Design Digital Twin, with the Manufacturing Digital Twin to enable closed loop manufacturing aware design.

This evolution brings with it new challenges of exponentially increasing complexity, and multiple disparate engineering domains that need to work together. It is here where AI is coming to the rescue to help guide where engineers need to focus their effort, encapsulate domain knowledge that they need to perform a task, and transform data between different domains either directly or via surrogate models.

In this presentation we will explore the way this evolution has affected IC and product design tools, the benefits it has brough to design teams, what the future holds, and how closed-loop manufacturing aware design will bring in a new era of design.

Presenter: Juan Rey, Siemens

TAKING 3DIC HETEROGENEOUS INTEGRATION MAINSTREAM

Time: 12:00 PM – 12:30 PM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Heterogeneous integration itself isn't new, but new design and manufacturing technologies, combined with new product demands from system integrators, means that heterogeneous integration and 3DIC are now becoming a necessity in mainstream design. This shift however is not without its challenges as 3D IC is not a simple extension of existing packaging solutions but creates a whole new set of Multiphysics integration considerations. The interaction of thermal, mechanical, reliability, test, and core semiconductor design increases complexity and requires disparate domains to seemly collaborate.

In this presentation we will explore the challenges introduced by 3D IC, the current state of the industry to address those challenges, the ecosystem needed to support 3DIC, and how users today can successfully adopt 3D IC leveraging new solutions, workflows, and 3D IC Design Kits (3DK) from Siemens EDA that are designed specifically with 3D IC in mind

Presenter: Tony Mastroianni, Siemens

NEW EDA METHODOLOGIES ARE TRANSFORMING ENGINEERING LIFECYCLE MANAGEMENT

Time: 1:00pm – 1:45pm
Session Type: SKYTalk
Topic: EDA
Room: DAC Pavilion, Level 2 Exhibit Hall

Description: This talk provides a broad, visionary perspective about the dynamic changes impacting electronic design automation tools and methodologies and their pivotal role in re-shaping engineering lifecycle management. It explains the trend toward convergence of EDA and CAE domains to address exploding system complexity and deliver multi-disciplinary solutions. Future workflows must incorporate digital threads that connect virtual prototypes and digital twins with physical systems. Predictive simulation and analysis across domains is key to accelerating engineering lifecycles.

Rapid industry adoption of AI, heterogeneous integrated circuits and chiplet technologies, software automation using scripting languages, and comprehensive data and intellectual property management tools is driving a seismic shift in design and verification methodologies. This talk covers how these EDA technologies contribute to more efficient and effective enterprise lifecycles. Application of these technologies must elevate RF, microwave, and mixed-signal design to an equal footing with digital design to achieve modernization of engineering workflows.

Presenters: Niels Fache, Keysight

ADVANCED VERIFICATION

Time: 1:30 PM – 3:00 PM
Session Type: Engineering Tracks
Topic Area(s): Front-End Design
Room: 2010, 2nd Floor

Session Chair: Dave Rich, Siemens

Description: Join us to learn about new strategies in the catch-up game verification engineers play daily with the increasing design complexity and tighter schedules. In this session, presenters will share their wisdom across HLS, FuSa and hardware/software verification.

- **Use UVM for AMS DFT through IEEE 1687 Procedural Description Language**
  Hitu Sharma, Rahul Lodwal, NXP Semiconductors, Delhi, India; Geert Seuren, NXP Semiconductors, Helmond, Netherlands;
- **Shift Left with Improved Power-Awareness in RTL Stage Design for Early Design Verification**
  Penchalkumar Gajula, Lakshmanan Balasubramanian, Gaurav Varshney, Sooraj Sekhar, Siddharth Sarin, Ruchi Shankar, Texas Instruments (India) Pvt. Ltd., Bengaluru, India;
- **Enhancing Quality and Reducing Verification Effort for RTL Implementations against High-Level C/C++ Models using Formal Equivalence**
  David Vincenzoni, Gianluca Rigano, STMicroelectronics, Agrate Brianza, Italy; Gaetano Raia, Maurizio Martina, Politecnico di Torino, Italy;
- **A Distributed Co-Simulation Environment and its Application in HW-FW Verification**
  Nitin Pundir, Viresh Paruthi, Ali El-Zein, Zoltan Hidvegi, IBM, Austin, TX; Pretty Jacob, Arun Joseph, Sandeep Korrapati, IBM, Bengaluru, India; Bodo Hoppe, IBM, Boblingen, Germany;
- **Who watches the watchman? FuSa Verification of DCLS configuration through Formal and Static checks**
  Sayandeep Sanyal, Avinash Pandey, Srobona Mitra, Sathish Manickam, Arunava Dutta, Qualcomm, Bengaluru, India; Deepak Baranwal, Qualcomm, Noida, India;
- **Systematic Flow on AC Scan Timing/ATPG Constraint Generation**
  Chen Yuan Kao, Yi Hsuan Chiu, Global UniChip Corp., Hsinchu, Taiwan

WHAT'S NEW IN IP VERIFICATION AND VALIDATION?

Time: 1:30 PM – 3:00 PM
Session Type: Engineering Tracks
Topic Area(s): IP
Room: 2012, 2nd Floor

Session Chair: Himanshu Sanghavi, Meta

Description: The increasing complexity of SoC designs, coupled with the high cost of a re-spin due to functional bugs, requires constant innovation in verifcation techniques and methodologies to ensure frst pass silicon success. This session discusses a collection of such techniques spanning automated methods to create simplifed test cases for tool bugs, use of symbolic simulation for the verifcation of interface IP, protocol validation of high speed serial links, power estimation and tracking using real world use cases, fast and efcient methodology for multi-PVT corner validation, and a formal verifcation framework for DDR5 power management features.

- **GPU Power Tracking and Optimization Using Emulation**
  Sandesh Saokar, Veera Dasari, Navid Farazmand, Intel, San Diego, CA;
- **AI-based High Sigma Verifcation Methodology for Multiple PVT Corners**
  Kwonchil Kang, Soonkeol Ryu, Seongkyun Shin, Samsung Electronics, Seoul, South Korea; Sungyoun Lee, Siemens, Seoul, South Korea;
- **Automated Design Scenario Extraction From A Large Design For Faster Debug Of Static Verifcation Tools**
  Gaurav Pratap, Vishal Keswani, Synopsys, Bengaluru, India; Sachin Bansal, Amit Goldie, Synopsys, Noida, India;
- **Watt's Up with DDR5: Formal Verifcation Framework for Robust DRAM Power Management**
  Pradip Prajapati, Intel, Bengaluru, India; Anshul Jain, Intel, Delhi, India; Mounica Kothi, Intel, San Diego, CA; Erin Rasmussen, Rocco Salvia, Intel, San Diego, CA;
- **Beyond Digital: Innovation in symbolic simulator to empower IO analog circuit validation**
  Pawan Verma, Manish Bansal, Anil-kumar Dwivedi, STMicroelectronics Pvt. Ltd., Noida, India; Amandeep Kaur Hari Sathianathan, Synopsys India Pvt. Ltd., Bengaluru, India;
- **Enabling Protocol Validation of High Speed Serial Links using SerDes to transfer data between PHY Chip and Link layer on FPGA**
  Priyanka Goel, Aashish Bhide, Vivek Uppal, Nitin Sharma, Synopsys, Bengaluru, India; Ameer Youssef, Synopsys, Toronto, ON, Canada

TECHNOLOGY AND IP SCALING BEYOND 5NM

Time: 1:30 PM – 3:00 PM
Session Type: Engineering Tracks
Topic Area(s): IP
Room: 2010, 2nd Floor

Organizer: Arif Khan, Cadence Design Systems, Inc.

Description: This session addresses the frontiers of technology scaling, examining the interplay between cost, performance, and power as designers navigate current limitations and future trends. Discussions will range from the evolution of process technology, such as FinFET to GAA, to the strategic use of DTCO and disaggregated designs in overcoming die size and cost-per-transistor challenges. Emphasizing the critical role of packaging in adopting chiplets, advances in interconnect and 3D-IC technologies will be explored. The collective insights aim to chart a course through the complexities of scaling in the more-than-Moore era, focusing on economic and technological viability.

Presenters: Gopi Ranganathan, Cadence Design Systems, Inc., Cupertino, CA; Nazar Zaidi, AMD, Saratoga, CA; Lluis Paris, TSMC, San Jose, CA

ADVANCED LOGIC SYNTHESIS - IMPROVING RUNTIME AND QUALITY

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): EDA
Room: 3004, 3rd Floor

Session Chair: Cunxi Yu (University of Maryland), Giovanni De Micheli (EPFL)

Description: This session includes six advanced logic synthesis works in addressing fundamental challenges of runtime efficiency and handling complex optimization objectives. The first two papers focus on high-performance parallel DAG-aware logic synthesis, exploring both GPU and CPU parallelism. The third and fourth presentations introduce and merge synthesis techniques in circuit-level architecture optimization, showcasing parallel prefix circuit design and pipelining. The fifth and sixth papers present novel formal methods, including Satisfiability and e-graphs, based on logic synthesis approaches to tackle complex optimization objectives in the conventional logic synthesis process.

- **Massively Parallel AIG Resubstitution**
  Yang Sun, Tianji Liu, Martin Wong, Evangeline Young, The Chinese University of Hong Kong, Hong Kong;
- **DACPara: A Divide-and-Conquer Parallel Approach for High-Quality Logic Rewriting in Large-Scale Circuits**
  Nanjiang Qu, Cong Tian, Zhenhua Duan, Xidian University, Xi' an, China;
- **Size-Optimized Depth-Constrained Large Parallel Prefix Circuits**
  Shiju Lin, Evangeline Young, The Chinese University of Hong Kong, Hong Kong;Bentian Jiang, Weihua Sheng, Huawei, Hong Kong, Hong Kong;
- **Revisiting Automatic Pipelining: Gate-level Forwarding and Speculation**
  Shuyao Cheng, Chongxiao Li, Zidong Du, Rui Zhang, Xing Hu, Xiaqing Li, Guanglin Xu, Yuanbo Wen, Qi Guo, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China;
- **E-Syn: E-Graph Rewriting with Technology-Aware Cost Functions for Logic Synthesis**
  Chen Chen, Guangyu Hu, Dongsheng Zuo, Yuzhe Ma, Hongce Zhang, The Hong Kong University of Science and Technology, Guangzhou, China; Cunxi Yu, University of Maryland, College Park, MD;
- **PONO: Power Optimization with Near Optimal SMT-based Sub-circuit Generation**
  Sunan Zou, Guojie Luo, Peking University, Beijing, China

EFFICIENT ACCELERATION STRATEGIES FOR TRANSFORMERS: FROM TOKEN SIMILARITY TO WEIGHT SPARSITY

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): AI
Room: 3003, 3rd Floor

Session Chair: Hyoukjun Kwon (University of California, Irvine)

Description: Recent advancement in transformer models led the performance improvement in language modeling and vision tasks. Transformers are equipped with the attention mechanism that extracts useful dependency information between input tokens. Due to the nature of sequential processing, running a transformer is bounded by off-chip memory bandwidth. For vision transformers, a feedforward network that follows after the attention module further incurs significant runtime overhead. In this session, many unique approaches and their associated hardware architecture are discussed, including proactively skipping computations for tokens with low probability, leveraging token similarities, bit-slice compression technique, and exploiting sparsity in transformers.

- **CSTrans-OPU: An FPGA-based Overlay Processor with Full Compilation for Transformer Networks via Sparsity Exploration**
  Yueyin Bai, Keqing Zhao, Yang Liu, Hongji Wang, Hao Zhou, Xiaoxing Wu, Jun Yu, Kun Wang, Fudan University, ShangHai, China;
- **FLAME: Fully Leveraging MoE Sparsity for Transformer on FPGA**
  Xuanda Lin, Huinan Tian, Wenxiao Xue, Lanqi Ma, Jialin Cao, Manting Zhang, Jun Yu, Kun Wang, Fudan University, Shanghai, China;
- **FNM-Trans: Efficient FPGA-based Transformer Architecture with Full N:M Sparsity**
  Manting Zhang, Jialin Cao, Kejia Shi, Keqing Zhao, Genhao Zhang, Jun Yu, Kun Wang, Fudan University, Shanghai, China;
- **ViT-slice: End-to-end Vision Transformer Accelerator with Bit-slice Algorithm**
  Dongjin Shin, Insu Choi, Joon-Sung Yang, Yonsei University, Seoul, South Korea;
- **SpARC: Token Similarity-Aware Sparse Attention Transformer Accelerator via Row-wise Clustering**
  Han Cho, Dongjun Kim, Seungeon Hwang, Jongsun Park, Korea University, Seoul, South Korea;
- **Token-Picker: Accelerating Attention in Text Generation with Minimized Memory Transfer via Probability Estimation**
  Junyoung Park, Myeonggu Kang, Yunki Han, Yang-Gon Kim, Jaekang Shin, Lee-Sup Kim, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea

HLS & EMERGING TECHNIQUES FOR SYNTHESIS

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): EDA
Room: 3010, 3rd Floor

Session Chairs: Alexandros Papakonstantinou (Intel); Evangeline Young (The Chinese University of Hong Kong)

Description: This session focuses on applying innovative methods in logic synthesis and HLS (high-level synthesis) of circuits. The first two papers work on memory partitioning and dynamic memory management in HLS to improve performance. The third and fourth papers present interesting methods to assist RTL debug and to make effective synthesis for superconducting circuits. The last two papers apply innovative VAE (variational autoencoder) and Bayesian Optimization to design and optimize circuits.

- **PMP: Pattern Morphing-based Memory Partitioning in High-Level Synthesis**
  Dajiang Liu, Decai Pan, Xiao Xiong, Jiaxing Shang, Chongqing University, Chongqing, China; Shouyi Yin, Tsinghua University, Beijing, China;
- **High-Performance and Resource-Efficient Dynamic Memory Management in High-Level Synthesis**
  Qinggang Wang, Long Zheng, Zhaozeng An, Haoqin Huang, Haoran Zhu, Yu Huang, Pengcheng Yao, Xiaofei Liao, Hai Jin, Huazhong University of Science and Technology, Wuhan, China;
- **Finding Bugs in RTL Descriptions: High-Level Synthesis to the Rescue**
  Baharealsadat Parchamdar, Benjamin Carrion Schaefer, The University of Texas at Dallas, Richardson, TX;
- **Synthesis of Resource-Efficient Superconducting Circuits with Clock-Free Alternating Logic**
  Jennifer Volk, University of California, Santa Barbara, CA; Panagiotis Papanikolaou, Georgios Zervakis, University of Patras, Greece; Georgios Tzimpragos, University of Michigan, Ann Arbor, MI;
- **CircuitVAE: Efficient and Scalable Latent Circuit Optimization**
  Jialin Song, NVIDIA, Pasadena, CA; Aidan Swope, Robert Kirby, Rajarshi Roy, Saad Godil, Bryan Catanzaro, NVIDIA, Santa Clara, CA; Jonathan Raiman, OpenAI, San Francisco, CA;
- **Knowing The Spec to Explore The Design via Transformed Bayesian Optimization**
  Donger Luo, Hang Zhou, China; Xinheng Li, Hao Geng, Shanghai Tech University, Shanghai, China; Qi Sun, Zhejiang University, Chen Bai, Bei Yu, The Chinese University of Hong Kong, Hong Kong

LEARN AND FUZZ!

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): EDA
Room: 3008, 3rd Floor

Session Chairs: Maheshwar Chandrasekar (Synopsys); Enrico Fraccaroli (University of Verona)

Description: By following this session you will discover how learning and fuzzing techniques allow to enhance verification. Learning approaches include reinforcement learning for the verification of complex integrated circuits, NN controllers used to synthesize barrier certificates, and natural language processing for security property generation. Fuzzing solutions are applied to test case generation, CPU verification and radiation effects simulation.

- **Advanced Reinforcement Learning Algorithms to Optimize Design Verification**
  Zahra Aref, Narayan Mandayam, Rutgers University, New Brunswick, NJ; Rohit Suvarna, Bill Huges, Sandeep Srinivasan, VerifAI, Palo Alto, CA;
- **Neural Barrier Certificates Synthesis of NN-Controlled Continuous Systems via Counterexample-Guided Learning**
  Hanrui Zhao, Niuniu Qi, Mengxin Ren, Zhengfeng Yang, East China Normal University, Shanghai, China; Xia Zeng, Southwest University, Chongqing, China; Zhenbing Zeng, Shanghai University, Shanghai, China;
- **NSPG: Natural language Processing-based Security Property Generator for Hardware Security Assurance**
  Xingyu Meng, Amisha Srivastava, Ayush Arunachalam, Yiorgos Makris, Kanad Basu, The University of Texas at Dallas, Richardson, TX;Avik Ray, Amazon, Sunnyvale, CA; Pedro Silva, Rafail Psiakis, Technology Innovation Institute, Abu Dhabi, United Arab Emirates;
- **CFTCG: Test Case Generation for Simulink Model through Code Based Fuzzing**
  Zhuo Su, Zehong Yu, Yu Jiang, Tsinghua University, Beijing, China; Dongyan Wang, Renmin University of China, Beijing, China; Rui Wang, Capital Normal University, Beijing, China; Yang Tao, Huawei, Shanghai, China;
- **PathFuzz: Broadening Fuzzing Horizons with Footprint Memory for CPUs**
  Yinan Xu, Sa Wang, Ninghui Sun, Yungang Bao, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Dan Tang, Beijing Institute of Open Source Chip, Beijing, China;
- **SSRE: Sensitivity-aware Single-particle Radiation Effects Simulation Framework in SoC Platforms based on SVM Algorithm**
  Meng Liu, Shuai Li, Ruijie Wang, Fei Xiao, Beijing University of Technology, Beijing, China; Chunxue Liu, Liang Wang, Beijing Microelectronics Technology Institute, Beijing, China

NEW FRONTIERS IN HARDWARE SECURITY

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): Security
Room: 3012, 3rd Floor

Session Chairs: Siddharth Garg (New York University); Daniel Dinu (Intel)

Description: Hardware security is crucial in the increasingly insecure cyberspace. The session presents advances in hardware security, spanning improved defenses against fault injection attacks and enhanced logic locking for DNNs to a novel approach to thwart cache side-channel attacks through high-level synthesis. Other presentations include a technique to fortify hardware-based malware detection against adversarial attacks and a demonstration of a software-based power side-channel attack on a commercial processor.

- **Uncovering Software-Based Power Side-Channel Attacks on Apple M1/M2 Systems**
  Nikhil Chawla, Chen Liu, Abhishek Chakraborty, Ke Sun, Intel, Hillsboro, OR; Igor Chervatyuk, Intel, Dublin, Ireland; Thais Moreira Hamasaki, Henrique Kawakami, Intel, Seatlle, WA;
- **HyCaMi: High-Level Synthesis for Cache Side Mitigation**
  Heiko Mantel,; Joachim Schmidt, Thomas Schneider, Maximilian Stillger, Tim Weiasmantel, Hossein Yalame, Technische Universitat Darmstadt, Darmstadt, Germany;
- **Evaluating the Security of Logic Locking on Deep Neural Networks**
  You Li, Guannan Zhao, Yunqi He, Hai Zhou, Northwestern University, Evanston, IL;
- **Plug Your Volt: Protecting Intel Processors against Dynamic Voltage Frequency Scaling based Fault Attacks**
  Nimish Mishra, Rahul Mool, Anirban Chakraborty, Debdeep Mukhopadhyay, Indian Institute of Technology, Kharagpur, India;
- **CDS: An Anti-Aging Calibratable Digital Sensor for Detecting Multiple Types of Fault Injection Attacks**
  Zhiyuan Chen, Kun Yang, Kui Ren, Zhejiang University, Hangzhou, China;
- **Beyond Conventional Defenses: Proactive and Adversarial-Resilient Hardware Malware Detection using Deep Reinforcement Learning**
  Zhangying He, Hossein Sayadi, California State University, Long Beach, CA;Houman Homayoun, University of California, Davis, CA

THE NEXT STEP TO EFFICIENT AI: NUMBER FORMATS, QUANTIZATION AND BEYOND

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): AI
Room: 3001, 3rd Floor

Session Chairs: Sarada Krithivasan (IBM); Igor Markov (Synopsys)

Description: The success of AI has been accompanied by an astronomical increase in computational requirements, while at the same time there is a drive to deploy complex AI algorithms on resource-constrained edge devices. The papers in this session explore new number formats, quantization techniques, and hardware-friendly algorithm design for deep neural networks including Large Language Models.

- **Algorithm-Hardware Co-Design of Distribution-Aware Logarithmic-Posit Encodings for Efficient DNN Inference**
  Akshat Ramachandran, Zishen Wan, Geonhwa Jeong, Tushar Krishna, Georgia Institute of Technology, Atlanta, GA; John Gustafson, Arizona State University, Tempe, AZ;
- **Genetic Quantization-Aware Approximation for Non-Linear Operations in Transformers**
- Pingcheng Dong, Yonghao Tan, Dong Zhang, Shi-Yang Liu, Xijie Huang, Kwang-Ting Cheng, Hong Kong University of Science and Technology, Hong Kong, Hong Kong; Tianwei Ni, Huaiyu Zhu, Yun Pan, Zhejiang University, Hangzhou, China; Xuejiao Liu, Yu Liu, Peng Luo, Luhong Liang, AI Chip Center for Emerging Smart System (ACCESS), Hong Kong, China; Fengwei An, Southern University of Science and Technology, Shenzhen, China;
- **RL-PTQ: RL-based Mixed Precision Quantization for Hybrid Vision Transformers**
- Eunji Kwon, Seokhyeong Kang, Pohang University of Science and Technology (POSTECH), Pohang-si, South Korea; Minxuan Zhou, Weihong Xu, Tajana Rosing, University of California, San Diego, CA;
- **APTQ: Attention-aware Post-Training Mixed-Precision Quantization for Large Language Models**
- Ziyi Guan, Ngai Wong, The University of Hong Kong, Hong Kong; Hantao Huang, Yupeng Su, Hong Huang, Hao Yu, Southern University of Science and Technology, Shenzhen, China;
- **EDGE-LLM: Enabling Efficient Large Language Model Adaptation on Edge Devices via Unified Compression and Adaptive Layer Voting**
- Zhongzhi Yu, Zheng Wang, Yuhan Li, Ruijie Gao, Sreenidhi Reddy Bommu, Yang (Katie) Zhao, Yingyan (Celine) Lin, Georgia Institute of Technology, Atlanta, GA;Xiaoya Zhou, University of California, Santa Barbara, CA

TRAPPED IONS NEUTRAL ATOMS FLYING ANCILLAS!

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3002, 3rd Floor

Session Chairs: Takashi Sato (Kyoto University); Kaitlin Smith (Northwestern University)

Description: Quantum computing has emerged as a leading computing model to solve scientific problems. A plethora of competing qubit technologies exist, each of which offer unique opportunities and trade-off options among various performance metrics. This session will cover distributed computing and tool development for some of the leading qubit technologies namely, adiabatic superconducting qubit, trapped-ion qubit, neutral atom qubit and quantum dot qubit.

- **TITAN: A Fast and Distributed Large-Scale Trapped-Ion NISQ Computer**
  Cheng Chu, Zhenxiao Fu, Fan Chen, Lei Jiang, Indiana University, Bloomington, IN;Yilun Xu, Gang Huang, Lawrence Berkeley National Lab, Berkeley, CA; Hausi Muller, University of Victoria, BC, Canada;
- **Hybrid Circuit Mapping: Leveraging the Full Spectrum of Computational Capabilities of Neutral Atom Quantum Computers**
  Ludwig Schmid, Technical University Munich, Germany; Sunghye Park, Pohang University of Science and Technology (POSTECH), Pohang-si, South Korea; Robert Wille, Technical University Munich, Germany;
- **Field Programmable Quantum Array Compilation with Flying Ancillas**
  Hanrui Wang, Song Han, Massachusetts Institute of Technology, Cambridge, MA; Bochen Tan, Jason Cong, University of California, Los Angeles, CA; Pengyu Liu, CMU, Pittsburgh, PA; Yilian Liu, Cornell University, Ithaca, NY; Jiaqi Gu, Arizona State University, Tempe, AZ;
- **Fast Virtual Gate Extraction For Silicon Quantum Dot Devices**
  Shize Che, Seongwoo Oh, Haoyun Qin, Yuhao Liu, Anthony Sigillito, Gushu Li, University of Pennsylvania, Philadelphia, PA;
- **RCGP: An Automatic Synthesis Framework for Reversible Quantum-Flux-Parametron Logic Circuits based on Efficient Cartesian Genetic Programming**
  Rongliang Fu, Tsung-Yi Ho, The Chinese University of Hong Kong, Hong Kong; Robert Wille, Technical University Munich, Germany

ASLEEP AT THE WHEEL? IN-CABIN MONITORING FOR AUTOMOTIVE SAFETY.

Time: 1:30 PM – 3:00 PM
Session Type: Research Panel
Topic Area(s): Autonomous Systems
Room: 3014, 3rd Floor

Organizers: Jude Angelo Ambrose, Seeing Machines, Canberra, Australia; Sri Parameswaran, University of Sydney, Sydney, Australia

Moderator: Sri Parameswaran, University of Sydney, Sydney, Australia

Description: According to data provided by the World Health Organization, it is a grim reality that more than 1.3 million people lose their lives annually due to the tragic outcomes of road traffic accidents, further exacerbating the situation with a staggering 20 to 50 million individuals being left with non-fatal injuries. These disheartening statistics serve as a stark reminder of the urgent need for improved safety measures in the automotive industry.

Historically driven by the pursuit of creating vehicles that captivate and exhilarate consumers, the automotive sector has increasingly shifted its focus toward fostering a robust safety culture. This transformation has only sometimes been an organic process, as governments worldwide have often found themselves leading the charge in pushing for more excellent vehicular safety through stringent regulations. These regulatory frameworks, which initially took root in Europe and China, have now been rapidly disseminated globally. Consequently, automakers have found themselves compelled to make safety an integral and non-negotiable facet of their automotive solutions.

The impending European Safety Regulations, set to become a standard in the industry, have been significantly motivated by the rapid evolution of automotive technology and an unwavering commitment to ensuring the safety of both drivers and passengers. A pivotal component of this technological revolution in the automotive realm is interior sensing. It plays a critical role in monitoring drivers for distractions and fatigue, as well as tracking the movements of vehicle occupants.

This distinguished panel of experts brings together some of the foremost sensor and System-on-chip (SoC) suppliers and in-cabin monitoring specialists who are pivotal in driving the burgeoning interior sensing market. Their collective aim is to deliberate on various topics, ranging from emerging technology trends to innovative packaging options, seamless connectivity, and integration points for Advanced Driver Assistance Systems (ADAS), including the transformative Driver and occupant Monitoring System technology.

Recognizing that human drivers are inherently prone to errors, safety technology providers adopt a holistic systems approach to assist, enhance, and even assume control of the driving task when necessary. In-cabin monitoring emerges as a crucial element within this overarching strategy. Overcoming challenges related to cost, packaging constraints, and system complexity, hardware and application vendors continually push the boundaries of innovation, seeking novel ways to optimize their designs to support efficient and cost-effective in-cabin monitoring solutions.

The panel discussion, featuring prominent figures from industry and University leaders such as Seeing Machines, Qualcomm, Texas Instruments, Ambarella, OmniVision, and TU Braunschweig, will delve deep into the dynamic Sensor and SoC market for in-cabin monitoring. They will explore critical issues, including how in-cabin monitoring technology underpins the global safety agenda, te preferences of suppliers regarding packaging locations, the pros and cons of various integration approaches, and the implications for Original Equipment Manufacturers (OEMs) who must ensure that safety and convenience remain paramount in their offerings. There are a variety of differing opinions, and it is these differing opinions that will be brought forth in this panel.

The panel is aimed at students, researchers, and practitioners. Students will understand the state of the art and the challenges. Researchers will be able to examine open industrial problems which are still open, and industry practitioners will be able to understand the available solutions and the industry trends.

The panel aims to engage in a comprehensive discussion surrounding critical questions, including but not limited to:

- How can we best support a low-cost and low-power consumption market?
- Which aspect or component of Sensor and SoC design should we prioritize for future advancements? What are the foremost challenges associated with Artificial Intelligence (AI) in designing sensors and SoCs?
- Where should we channel our Research and Development (R&D) efforts?
- Which packaging configurations are poised to dominate the automotive market?
- How vital is cybersecurity in this context?
- What obstacles do we face in implementing AI techniques for in-cabin monitoring?
- How are these cutting-edge designs rigorously tested to ensure their efficacy and safety?

Presenters: Jude Angelo Ambrose, Seeing Machines, Australia; Sumant Paranjpe, Qualcomm, USA; Robert Bloomquist, Amberalla, USA; Tomas Geurts, OmniVision, Belgium; Naehyuck Chang, Samsung, Korea

AI TECHNOLOGIES MEET QUANTUM COMPUTING

Time: 1:30 PM – 3:00 PM
Session Type: Special Session (Research)
Topic Area(s): AI
Room: 3006, 3rd Floor

Session Chair: Gushu Li, University of Pennsylvania

Organizer(s): Mitch Thornton, Southern Methodist University; Hanrui Wang, Massachusetts Institute of Technology

Description: This special session focuses on the cutting-edge domain of integrating Artificial Intelligence (AI) technologies with Quantum Computing. While research in quantum computing has predominantly been the purview of academia, we emphasize the critical need for industrial engagement to foster its application in the real world, thereby uncovering its latent commercial potential. Our objective is to bridge the gap between academic research and practical applications, increasing awareness of quantum computing's capabilities and ensuring its sustainable development. To this end, we have convened a panel of eminent experts from Argonne National Lab, JPMorgan Chase, and Tencent, leaders in the field of quantum computing. They will engage in an in-depth discussion, through three talks, on the synergy between quantum computing and AI technologies, and how this amalgamation manifests immense potential in diverse real-world applications such as chemistry, finance, and graph theory objects. We believe that such collaborative efforts will accelerate the advancement of quantum computing technology and lay a solid foundation for its application across various sectors. This contribution extends beyond the technological sphere, as the progression in quantum computing offers novel solutions to many of the global challenges we face today.

- **Machine Learning for Optimization of Quantum Compilation**
  Shengyu Zhang, Tencent Quantum Lab, Shenzhen, China
- **Graph Learning for Parameter Prediction of Quantum Approximate Optimization Algorithm**
  Ji Liu, Argonne National Laboratory, Lemont, IL
- **Challenges and Opportunities of Quantum Optimization in Finance**
  Marco Pistoia, JPMorgan Chase, New York, NY

LEVERAGING AI/ML FOR ELECTRONIC DESIGN AND SIMULATION

Time: 1:45pm-3:00pm
Session Type: Exhibitor Forum
Topic: Design
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: AI/ML is causing sweeping changes in almost every industry, and electronic design and simulation are no exceptions. EDA tools have a long history of using heuristics and numerical approximations to ensure designer productivity keeps pace with Moore's Law. This session will feature Ansys CTO Prith Banerjee joined by industry speakers to discuss today's practical application of AI/ML for electronic design and simulation, and how this trend will determine the direction of EDA in the future.

Presenters: Prith Banerjee, Ansys; Sanjay Choudhry, NVIDIA

BLACKOUT – MANAGING KW POWER BUDGETS

Time: 2:00 PM – 2:45 PM
Session Type: DAC Pavilion Panel
Room: DAC Pavilion, Level 2 Exhibit Hall

Moderator: Ed Sperling, Semiconductor Engineering

Description: SoCs designed for compute-intensive workloads, such as AI training and inferencing, continue to grow and power budgets are increasing geometrically. Handling these power budgets from an SoC and system perspective requires rigorous tools, flows, and methodologies. The question that remains is how these burgeoning power budgets impact broader systems and system-of-system effects, and what role does silicon IP play in shaping these outcomes.

2.5D and 3D solutions are emerging as potential mitigators for the expanding power budgets, but the extent of their effect is yet to be fully understood. Additionally, with the constant evolution and growth in technology, there is a looming question: will power budgets level off or continue on a path of exponential growth? The influence of silicon IP in directing this trajectory is a topic of keen interest.

A significant player in this dynamic is the role of next-generation VRMs. With their potential to regulate voltage and hence influence power, they might hold the answer to managing the surge in power budgets. This conference seeks to explore their impact, dissect the role of silicon IP, and generate insightful discussions on the future of power consumption within technology. Together, we will answer some of the following questions from an EDA, system, IP, and SoC design perspective:

- What are the primary factors driving the immense leaps in on-die power?
- What tools, flows, and methodologies are required to manage SoC and system power budgets? o What are the system and system-of-system effects of ballooning power budgets?
- What effect will 2.5D and 3D solutions have on growing power budgets?
- Will we see a leveling off in power budgets or will they keep growing exponentially? And why? o What is the role of next-generation VRMs

Panelists: Joe Davis, Siemens; Mo Faisal, Movelius; Trey Roessig, Empower; Dean Wallace, Marvell; Hans Yeager, Tenstorrent

ADVANCING CHIP SECURITY TO MEET HEIGHTENED REQUIREMENTS

Time: 3:00 PM – 3:45 PM
Session Type: DAC Pavilion Panel
Room: DAC Pavilion, Level 2 Exhibit Hall

Moderator: Ann Mutschler, Semiconductor Engineering

Description: Semiconductor security is increasingly crucial due to the increasing number of chip vulnerabilities and initiatives regulating cybersecurity assurance for electronic products and systems. Various industry and regulatory bodies have implemented standards and regulations to address cybersecurity concerns across both software and hardware, such as the ISO/SAE 21434 cybersecurity standard for automotive, and the recently released European Union (EU) Cyber Resilience Act. This panel of industry experts will delve into the current state of cybersecurity assurance for semiconductor chips, and how the emerging security standards and growing threat landscape will continue to accelerate the need for more rigorous cybersecurity measures across all sectors.

Panelists: Andreas Kuehlmann, Cycuity; Neeraj Paliwal, Rambus; Victoria Coleman, US Air Force; Vivek Tiwari, Intel;

AUTODV: AI-GENERATED HDL WITH DESIGN VERIFICATION IN-THE-LOOP

Time: 3:30 PM – 4:00 PM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Artificial Intelligence (AI), particularly Large Language Models (LLMs), has revolutionized the landscape of Hardware Description Language (HDL) generation in digital design. This breakthrough technology holds immense promise for streamlining design processes and accelerating innovation. However, the probabilistic nature of LLMs poses unique challenges in HDL generation, frequently leading to inaccurate code predictions. This is a crucial concern in hardware design, where precision is paramount.

To address this critical challenge, we introduce AutoDV, an innovative LLM-based architecture designed to enhance the precision and reliability of AI-generated HDL code. At its core lies a system of interconnected, specialized, and compact LLMs, each meticulously crafted to handle specific aspects of the HDL generation process. This approach not only enables AutoDV to leverage the collective strengths of individual LLMs, but also fosters synergistic interactions among them.

AutoDV's groundbreaking capabilities stem from its two key components: the capability of automatically interfacing with external verification tools and a comprehensive library of pre-defined IPs. By seamlessly interfacing with established verification tools, AutoDV ensures rigorous Design Verification (DV), minimizing the risk of propagating errors to subsequent design stages. Additionally, AutoDV's IP library empowers LLMs to directly access and utilize these well-established and rigorously verified design components, significantly elevating the accuracy of the generated HDL code.

In this presentation, we will explore the technical underpinnings of AutoDV, beginning with an overview of its architecture and then examining the synergism between its components. The presentation will conclude with a practical demonstration.

Speaker: Valerio Tenace, PrimisAI

WHAT IS THE FUTURE OF DESIGN VERIFICATION? UVM, PSS, FORMAL, VIP, AI & BEYOND

Time: 3:30 PM – 5:00 PM
Session Type: Engineering Tracks
Topic Area(s): Front-End Design
Room: 2010, 2nd Floor

Organizers: Ambar Sarkar, NVIDIA, Boston, MA

Moderator: Cliff Cummings, Sunburst Design, Provo, UT

Description: Are existing verification methodologies running out of steam? Are some newer technologies still finding acceptance and adoption? Are some technologies, such as AI, being over-hyped? Are there too many tools to choose from and are they only affordable to large development teams?

Industry-expert panelists will discuss their views on existing industry-standard verification methodologies, (UVM, PSS, Formal, VIP) and future trends towards improved verification (AI and Beyond) and offer their perspectives on the viability of these various tools and trends. Panelists will address potential future improvements to existing tools or new technologies to accelerate verification.

Do not expect the panelists to be in complete agreement on these topics!

Presenters: Dave Rich, Siemens; Mark Glasser, Astera Labs; Arturo Salz, Synopsys; Keith Reeder, BAE Systems; Dave Kelf, Breker Verification Systems Inc.; Joe Costello, Inpho

DEMYSTIFYING FAILURE MECHANISMS AT ADVANCED NODES

Time: 3:30 PM - 5:00 PM
Session Type: Engineering Tracks
Topic Area(s): IP
Room: 2012, 2nd Floor

Organizers: Pawini Mahajan, Synopsys

Description: Silicon is inherently unreliable, and silicon at advanced nodes is most susceptible. DFX at advanced nodes calls for new strategies. This invited session will explore failure-mechanism driven techniques to enable reliable advanced node silicon. Key topics will include safety, security, reliability and SLM (Silicon Lifecycle Management) methodologies and frameworks that are necessary to ensure reliable silicon.

Presenters: Pawini Mahajan, Yervant Zorian, Synopsys; Amr Haggag, Arm Ltd.; Dimitris Gizopoulos, University of Athens

GOING VERTICAL. CHALLENGES OF THE AUTOMOTIVE SILICON ECOSYSTEM

Time: 3:30 PM – 5:00 PM
Session Type: Engineering Tracks
Topic Area(s): IP
Room: 2008, 2nd Floor

Organizers: Joerg Seitter, Infineon

Description: The increasing dynamics of automotive use-cases lead to novel challenges given the rigid requirements on dependability of these systems. While Advanced Driver Assistance use-cases call for more and more compute performance other use-cases raise the need for flexible and frequent integration of updates and upgrades. In this context, we see contradicting paradigms: on one hand, to optimize for specific dedicated hardware targets, thus rendering the application dependent on this hardware, and on the other hand to make hardware a commodity that is easy to change with a proclaimed decoupling of hardware and software.

At the same time, the multi-year turnaround cycles from OEMs down to Tier2 suppliers make it harder to predict the required functionality and optimal split between general purpose and dedicated hardware.

This leads to significant challenges along the vertical supply chain:

- Where are the right places to introduce abstractions to decouple functional layers? Where shall we avoid that to allow for optimizations?
- Which technology layers need what grade of standardization to warrant successful adoption and still foster competition through USPs?
- How can we shorten the turnaround cycles by integrating tools of standardized interfaces?

New technologies and advancements seem to be promising, e.g., chiplet technology, but must stand the test of automotive qualification which raises additional open questions.

In this session we will go along the vertical and bring together esteemed industry leader to give an insight into the challenges on each level.

Presenters: Christian Pacha, Infineon Technologies AG, Munich, Germany; Arne Hamann, Robert Bosch GmbH, Renningen, Germany; Douglas Patullo, TSMC, San Jose, CA; Kamal Desai, Synopsys, Aachen, Germany

STCO FOR EMBEDDED COMPUTE IN MEMORY DEVICES AND CIRCUITS

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): Embedded Systems
Room: 3003, 3rd Floor

Session Chair: Tae Hyoung Kim (Nanyang Technological University); Dayane Reis (University of South Florida)

Description: Compute in Memory (CIM) is a promising approach to mitigate the data movement energy and latency costs in modern data-intensive workload applications. This session brings in recent developments in emerging embedded memory devices, circuits, design methodologies, and their impact on the system-level power performance metrics for various workloads.

- **Series-Parallel Hybrid SOT-MRAM Computing-in-Memory Macro with Multi-Method Modulation for High Area and Energy Efficiency**
  Weiliang Huang, Jinyu Bai, Wang Kang, Zhaohao Wang, Kaihua Cao, He Zhang, Weisheng Zhao, Beihang University, Beijing, China; Hongxi Liu, Truth Memory Corporation, Beijing, China;
- **EasyACIM: An End-to-End Automated Analog CIM with Synthesizable Architecture and Agile Design Space Exploration**
  Haoyi Zhang, Jiahao Song, Xiaohan Gao, Xiyuan Tang, Yibo Lin, Runsheng Wang, Ru Huang, Peking University, Beijing, China;
- **Improving the Efficiency of In-Memory-Computing Macro with a Hybrid Analog-Digital Computing Mode for Lossless Neural Network Inference**
  Qilin Zheng, Ziru Li, Jonathan Ku, Yitu Wang, Brady Taylor, Yiran Chen, Duke University, Durham, NC; Deliang Fan, Johns Hopkins University, Baltimore, MD;
- **Synthesis of Compact Flow-based Computing Circuits from Boolean Expressions**
  Sven Thijssen, Muhammad Rashedul Haq Rashed, Rickard Ewetz, University of Central Florida, Orlando, FL; Sumit Jha, Florida International University, Miami, FL;
- **CAP: A General Purpose Computation-in-memory with Content Addressable Processing Paradigm**
  Zhiheng Yue, Shaojun Wei, Yang Hu, Shouyi Yin, Tsinghua University, Beijing, China;
- **ModSRAM: Algorithm-Hardware Co-Design for Large Number Modular Multiplication in SRAM**
  Jonathan Ku, Junyao Zhang, Haoxuan Shan, Qilin Zheng, Ziru Li, Yiran Chen, Duke University, Durham, NC; Saichand Samudrala, Jiawen Wu, Jeyavijayan Rajendran, Texas A&M University, College Station, TX;
- **Compact and Efficient CAM Architecture through Combinatorial Encoding and Self-Terminating Searching for In-Memory-Searching Accelerator**
  Weikai Xu, Jin Luo, Qianqian Huang, Ru Huang, Peking University, Beijing,
- **Dyn-Bitpool: A Two-sided Sparse CIM Accelerator Featuring a Balanced Workload Scheme and High CIM Macro Utilization**
  Xujiang Xiang, Zhiheng Yue, Yuxuan Li, Liuxin Lv, Shaojun Wei, Yang Hu, Shouyi Yin, Tsinghua University, Beijing, China

ACCELERATORS AND CACHE MEMORIES MEET HETEROGENEOUS ARCHITECTURES

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3012, 3rd Floor

Session Chairs: Dimitrios Soudris (National Technical University of Athens); George Tzimpragos (University of Michigan)

Description: This session presents significant advancements in the design of application-specific accelerators and cache memory challenges. This session presents accelerators for sparse matrix multiplication through a novel co-design approach, a reformulated Winograd convolution, a Bayes Neural Networks as well as for mitigation of manufacturing security risks owing to the design of a novel ASIC. Additionally, novel results of a ultra-fast, knowledge-based HLS design optimization method and a coarse-grained reconfigurable architecture (CGRA) acceleration framework for end-to-end homomorphic applications are presented. Regarding the cache memory challenges, advancements on the development of a shared memory expansion method for GPU and two novel sub-prefetchers are provided.

- **SpaHet: A Software/Hardware Co-design for Accelerating Heterogeneous-Sparsity based Sparse Matrix Multiplication**
  Haoqin Huang, Pengcheng Yao, Zhaozeng An, Yufei Sun, Ao Hu, Peng Xu, Long Zheng, Xiaofei Liao, Hai Jin, Huazhong University of Science and Technology, Wuhan, China;
- **WinoGen: A Highly Configurable Winograd Convolution IP Generator for Efficient CNN Acceleration on FPGA**
  Mingjun Li, Pengjia Li, Shuo Yin, Shixin Chen, Beichen Li, Chong Tong, Tinghuan Chen, Bei Yu, The Chinese University of Hong Kong, Hong Kong; Jianlei Yang, Beihang University, Beijing, China;
- **Data-driven HLS optimization for reconfigurable accelerators**
  Aggelos Ferikoglou, Andreas Kakolyris, Vasilis Kypriotis, Dimosthenis Masouros, Dimitrios Soudris, Sotirios Xydis, National Technical University of Athens, Greece;
- **Hardware-Aware Neural Dropout Search for Reliable Uncertainty Prediction on FPGA**
  Zehuan Zhang, Hao (Mark) Chen, ; Wayne Luk, Imperial College London, United Kingdom; Hongxiang Fan, Lukasz Dudziak, Samsung Electronics, Cambridge, United Kingdom
- **FHE-CGRA: Enable Efficient Acceleration of Fully Homomorphic Encryption on CGRAs**
  Miaomiao Jiang, Yilan Zhu, Honghui You Lei Ju, Shandong University, Qingdao, China; Cheng Tan, Google, Mountain View, CA; Zhaoying Li, National University of Singapore, Singapore; Jiming Xu, Ant Group, Shenzhen, China;
- **SMILE: LLC-based Shared Memory Expansion to Improve GPU Thread Level Parallelism**
  Tianyu Guo, Sun Xuanteng Huang, Kan Wu, Xianwei Zhang, Nong Xiao, Sun Yat-Sen University, GuangZhou, China;
- **Planaria: Full Pattern Directed Heterogeneous Hardware Prefetcher with Efficient Bypass**
  Yuhang Liu, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Mingyu Chen, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China;
- **An IP-Agnostic Foundational Cell Array Offering Supply Chain Security**
  Christopher Talbot, Deepali Garg, Lawrence Pileggi, Kenneth Mai, Carnegie Mellon University, Pittsburgh, PA

AI EFFICIENCY FROM FAR MEMORY TO CROSS-PLATFORM PERFORMANCE

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): AI
Room: 3001, 3rd Floor

Session Chairs: Xiaoxuan Yang (University of Virginia, Stanford University); Hongxiang Fan (Samsung AI Center Cambridge)

Description: This session charts a multifaceted exploration of how to optimize AI system efficiency. Presentations will explore dynamic voltage and frequency scaling for deep neural networks, dissect server overheads during DNN inference, and describe the use of active learning for Design-Technology Co-optimization (DTCO). The session will additionally address optimization of tensor programs, analytical cost-models for cross-platform performance prediction, advanced graph representation learning for performance modeling, and accelerating training of physics-informed neural networks.

- **Sharry: An Efficient and Sharing Far Memory System**
  Chen Chen, Yuhang Huang, Shuiguang Deng, Jianwei Yin, Xinkui Zhao, Zhejiang University, HangZhou, China;
- **PowerLens: An Adaptive DVFS Framework for Optimizing Energy Efficiency in Deep Neural Networks**
  Jiawei Geng, Zongwei Zhu, Weihong Liu, Xuehai Zhou, Boyu Li, University of Science and Technology of China, Hefei, China;
- **Beyond Inference: Performance Analysis of DNN Server Overheads for Computer Vision**
  Ahmed AbouElhamayed, Mohamed Abdelfattah, Cornell University, New York, NY; Susanne Balle, Intel, Hudson, NH; Deshanand Singh, Intel, Toronto, ON, Canada;
- **Accelerating DTCO with a Sample-Efficient Active Learning Framework for TCAD Device Modeling**
  Chanwoo Park, Junghwan Park, Premkumar Vincent, Hyunbo Cho, Alsemy Inc., Seoul, South Korea;
- **A Holistic Functionalization Approach to Optimizing Imperative Tensor Programs in Deep Learning**
  Jinming Ma Yueqian Zhang, Minxi Jin, Lijuan Jiang, Shanghai Artificial Intelligence Laboratory, Shanghai, China; Xiuhong Li, Shengen Yan, Yun (Eric) Liang, Chao Yang, Peking University, Beijing, China; Zihan Wang, Yuting Chen, Shanghai Jiao Tong University, Shanghai, China; Xingcheng Zhang, SenseTime, Shanghai, China; Dahua Lin, The Chinese University of Hong Kong, Hong Kong;
- **Crop: An Analytical Cost Model for Cross-Platform Performance Prediction of Tensor Programs**
  Xinyu Sun, Yu Zhang, Shuo Liu, Yi Zhai, University of Science and Technology of China, Hefei, China;
- **G2PM: Performance Modeling for ACAP Architecture with Dual-Tiered Graph Representation Learning**
  Tuo Dai, Bizhao Shi, Guojie Luo, Peking University, Beijing, China;
- **SGM-PINN: Sampling Graphical Models for Faster Training of Physics-Informed Neural Networks**
  John Anticev, Ali Aghdaei, Wuxinlin Cheng, Zhuo Feng, Stevens Institute of Technology, Hoboken, NJ

MULTIVERSE OF EMERGING TECHNOLOGIES FOR COMPUTING AND OPTIMIZATION

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3002, 3rd Floor

Session Chairs: Dharanidhar Dang (The University of Texas at San Antonio); Jiyong Woo (Kyungpook National University)

Description: The landscape of computing has witnessed a surge in emerging device technologies, encompassing ferroelectric, resistive, superconducting, and oxide semiconductor devices. These cutting-edge technologies offer promising avenues for efficiently addressing specialized computational tasks, including but not limited to in-memory computing, Bayesian inference, combinatorial optimization, and associative processing. This session will explore the latest advancements in these diverse device platforms, shedding light on their potential to revolutionize the computational paradigm and enable transformative applications across various domains

- **FeBiM: Efficient and Compact Bayesian Inference Engine Empowered with Ferroelectric In-Memory Computing**
  Chao Li, Xunzhao Yin, Zhejiang University, Hangzhou, China; Zhicheng Xu, Ruibin Mao, Can Li, The University of Hong Kong, Hong Kong; Bo Wen, Hong Kong University, Hong Kong; Thomas Kampfe, Fraunhofer IPMS, Dresden, Germany; Kai Ni, University of Notre Dame, South Bend, IN;
- **Energy Efficient Dual Designs of FeFET-Based Analog In-Memory Computing with Inherent Shift-Add Capability**
  Zeyu Yang, Qingrong Huang, Yu Qian, Xunzhao Yin, Zhejiang University, Hangzhou, China; Kai Ni, University of Notre Dame, South Bend, IN; Thomas Kampfe, Fraunhofer IPMS, Dresden, Germany;
- **STAGGER: Enabling All-in-One Subarray Sensing for Efficient Module-level Processing in Open-Bitline ReRAM**
  Chengning Wang, Dan Feng, Yuchong Hu, Wei Tong, Jingning Liu, Huazhong University of Science and Technology, Wuhan, China;
- **C-Nash: A Novel Ferroelectric Computing-in-Memory Architecture for Solving Mixed Strategy Nash Equilibrium**
  Yu Qian, Cheng Zhuo, Xunzhao Yin, Zhejiang University, Hangzhou, China; Kai Ni, University of Notre Dame, South Bend, IN; Thomas Kampfe, Fraunhofer IPMS, Dresden, Germany;
- **Hyb-Learn: A Framework for On-Device Self-Supervised Continual Learning with Hybrid RRAM/SRAM Memory**
  Fan Zhang, Deliang Fan, Johns Hopkins University, Baltimore, MD;Li Yang, University of North Carolina, Charlotte, Charlotte, NC;
- **Unleashing the Power of T1-cells in SFQ Arithmetic Circuits**
  Rassul Bairamkulov, Mingfei Yu, Giovanni De Micheli, Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland;
- **HyCiM: A Hybrid Computing-in-Memory QUBO Solver for General Combinatorial Optimization Problems with Inequality Constraints**
  Yu Qian, Zeyu Yang, Xunzhao Yin, Zhejiang University, Hangzhou, China;Kai Ni, University of Notre Dame, South Bend, IN; Alptekin Vardar, Thomas Kampfe, Fraunhofer IPMS, Dresden, Germany;
- **4-Transistor Ternary Content Addressable Memory Cell Design using Stacked Hybrid IGZO/Si Transistors**
  Munhyeon Kim, Jae-Joon Kim, Seoul National University, Seoul, South Korea

WHERE ANALOG, DIGITAL, AND ML/AI MEET!

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3004, 3rd Floor

Session Chairs: Yu Cao (University of Minnesota); Xin Zhang (IBM Research)

Description: This interdisciplinary session showcases advances in low-power, high-performance architecture and circuit design for AI/ML and imaging applications, and the use of AI/ML in analog and digital circuit design. It starts with a low-power architecture for high-resolution image sensing. The second paper optimizes memory, power, and security for hyperdimensional computing. The third paper improves performance prediction of circuit topologies within learning-based analog circuit optimization. The fourth paper introduces ChatCPU, an LLM-based hardware design and verification platform. The next two papers aim to accelerate model training and inference with reduced-circuit-size and low-power architecture designs. The seventh paper proposes a Generative AI and ML-based framework to drive automated analog layout synthesis. The session concludes with a hardware accelerator design to handle the unique computational requirements of neural volume rendering.

- **CEDAR: Computing-in-pixel Edge-aware Detection and Reconstruction Architecture for High-resolution 3D Imaging**
  Bu Chen, Zhangcheng Huang, Qi Zheng, Weiyi Tang, Jingyi Wang, Hankun Lv, Chixiao Chen, Jianlu Wang, Qi Liu, Fudan University, Shanghai, China;
- **VAE-HDC: Efficient and Secure Hyper-dimensional Encoder Leveraging Variation Analog Entropy**
  Boyang Cheng, Jianbo Liu, Steven Davis, Zephan Enciso, Yiyang Zhang, Ningyuan Cao, University of Notre Dame, South Bend, IN;
- **Graph-Transformer-based Surrogate Model for Accelerated Converter Circuit Topology Design**
  Shaoze Fan, Haoshu Lu, Jing Li, New Jersey Institute of Technology, Newark, NJ; Shun Zhang, IBM, Cambridge, MA; Ningyuan Cao, University of Notre Dame, South Bend, IN; Xin Zhang, IBM, Yorktown Heights, NY;
- **ChatCPU: An Agile CPU Design and Verification Platform with LLM**
  Xi Wang, Gwok-Waa Wan, Sam-Zaak Wong, Layton Zhang, Tianyang Liu, Qi Tian, Jianmin Ye, Southeast University, Nanjing, China;
- **Energy-efficient SNN Architecture using 3nm FinFET Multiport SRAM-based CIM with Online Learning**
  Lucas Huijbregts, Technische Universitat Delft, Netherlands; Hsiao-Hsuan Liu, Paul Detterer, Amirreza Yousefzadeh, imec, Eindhoven, Netherlands; Said Hamdioui, Rajendra Bishnoi, Delft University of Technology, Delft, Netherlands;
- **AdderNet 2.0: Optimal FPGA Acceleration of AdderNet with Activation-Oriented Quantization and Fused Bias Removal based Memory Optimization**
  Yunxiang Zhang, Omar Kailani, Wenfeng Zhao, Binghamton University, Vestal, NY;
- **CDLS: Constraint Driven Generative AI Framework for Analog Layout Synthesis**
  Prasanth Mangalagiri, Lynn Qian, Farrukh Zafar, Phoebe Chang, Saripalli Vinay, Intel, Santa Clara, CA; Praveen Mosalikanti, Intel, Hillsboro, OR; Arun Kurian, Intel, Fairfax, VA;
- **ZeroTetris: A Spacial Feature Similarity-based Sparse MLP Engine for Neural Volume Rendering**
  Haochuan Wan, Linjie Ma, Antong Li, Pingqiang Zhou, Jingyi Yu, Xin Lou, Shanghai Tech University, Shanghai, China

BUCKLE UP FOR NEXT GENERATION COMPUTING MODELS AND HARDWARE

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3010, 3rd Floor

Session Chairs: Qingxue Zhang (Purdue School of Engineering & Technology) Sudhakar Pamarti, University of California, Los Angeles

Description: This session comprises 8 captivating papers that tackle challenges and opportunities across various domains of emerging computing. The first paper addresses hardware acceleration of nonparametric statistical operations in big data analysis. The second paper introduces an optical near-sensor accelerator designed for efficient image processing. Focusing on neuromorphic computing, the third paper explores simulation techniques integrating device-level non-linearity. The next two papers aim to accelerate the Ising model using compute-in-memory or column decomposition techniques. The sixth paper offers insights into enhancement techniques for Hyperdimensional Computing. Concluding the session, the last two papers delve into non-CMOS based computing paradigms, encompassing DNA storage and microfluidic multiplexer technologies.

- **Hynify: A High-throughput and Unified Accelerator for Multi-Mode Nonparametric Statistics**
  Kaihong Huang, Dian Shen, Zhaoyang Wang, Juntao Yang, Beilun Wang, Southeast University, Nanjing, China;
- **Lightator: An Optical Near-Sensor Accelerator with Compressive Acquisition Enabling Versatile Image Processing**
  Mehrdad Morsali, Deniz Najafi, Shaahin Angizi, New Jersey Institute of Technology, Newark, NJ; Brendan Reidy, Ramtin Zand, University of South Carolina, Columbia, SC; Sepehr Tabrizchi Arman Roohi, University of Nebraska, Lincoln, Lincoln, NE; Mohsen Imani, University of California, Irvine, CA; Mahdi Nikdast, Colorado State University, Fort Collins, CO;
- **TraiNDSim: A Simulation Framework for Comprehensive Performance Evaluation of Neuromorphic Devices for On-Chip Training**
  Donghyeok Heo, Hyeonsu Bang, Jong Hwan Ko, Sungkyunkwan University, Suwon, South Korea;
- **Digital CIM with Noisy SRAM Bit: A Compact Clustered Annealer for Large-Scale Combinatorial Optimization**
  Anni Lu, Junmo Lee, Yuan-Chun Luo, Shimeng Yu, Georgia Institute of Technology, Atlanta, GA; Hai Li, Ian Young, Intel, Hillsboro, OR;
- **Efficient Approximate Decomposition Solver using Ising Model**
  Weihua Xiao, Xingyue Qian, Weikang Qian, Shanghai Jiao Tong University, Shanghai, China; Tingting Zhang, Jie Han, University of Alberta, Edmonton, AB, Canada;
- **Bitwise Adaptive Early Termination in Hyperdimensional Computing Inference**
  Wei-Chen Chen, Sara Achour, H.-S. Philip Wong, Stanford University, Stanford, CA;
- **Triplet Network-Based DNA Encoding for Enhanced Similarity Image Retrieval**
  Takefumi Koike, Hiromitsu Awano, Takashi Sato, Kyoto University, Kyoto, Japan;
- **LaMUX: Optimized Logic-Gate-Enabled High-Performance Microfluidic Multiplexer Design**
  Siyuan Liang, Tsung-Yi Ho, The Chinese University of Hong Kong, Hong Kong; Yushen Zhang, Mengchu Li, Tsun-Ming Tseng, Ulf Schlichtmann, Technical University Munich, Muenchen, Germany; Rana Altay, Hudson Gasvoda, Ismail Araci, Santa Clara University, Santa Clara, CA

FROM CONCEPTION TO DEPLOYMENT, A JOURNEY IN CPS AND IOT DESIGN

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3008, 3rd Floor

Session Chairs: Francesco Regazzoni (University of Amsterdam, Universit a della Svizzera italiana) Chen Liu, Intel

Description: Cyber-physical systems and IoT devices are pervading every aspect of our lives, including critical infrastructures. Because of this, these systems need to be built considering several functional and non-functional requirements (e.g., low power, safety, etc.), making CPS/IoT design and operations extremely challenging. This session covers several aspects of the design, deployment, and management of CPS and IoT, including synthesis, acceleration, scheduling, and thermal management.

- **DeepRIoT: Continuous Integration and Deployment of Robotic-IoT Applications**
  Meixun Qu, Jie He, Zlatan Tucakovic, Haris Isakovic, Radu Grosu, Vienna University of Technology, Vienna, Austria; Ezio Bartocci, Technische Universitat Wien, Vienna, Austria; Dejan Nickovic, Austrian Institute of Technology, Vienna, Austria;
- **SPARK: An Efficient Hybrid Acceleration Architecture with Run-Time Sparsity-Aware Scheduling for TinyML Learning**
  Mingxuan Li, Qinzhe Zhi, Yanchi Dong, Le Ye, Tianyu Jia, Peking University, Beijing, China;
- **MTL-Split: Multi-Task Learning for Edge Devices using Split Computing**
  Luigi Capogrosso, Enrico Fraccaroli, Franco Fummi, Marco Cristani, University of Verona, Italy; Samarjit Chakraborty, University of North Carolina, Chapel Hill, NC;
- **VVIP: Versatile Vertical Indexing Processor for Edge Computing**
  Hyungjoon Bae, Wanyeong Jung, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea; Da Won Kim, Columbia University, New York, NY;
- **LOTUS: Learning-based Online Thermal and Latency Variation Management for Two-stage Detectors on Edge Devices**
  Yifan Gong, Yushu Wu, Pu Zhao, Zheng Zhan, Yanzhi Wang, Northeastern University, Boston, MA; Liangkai Liu, University of Michigan, Ann Arbor, MI; Chao Wu, Chinese Academy of Sciences, Beijing, China; Xulong Tang, University of Pittsburgh, Pittsburgh, PA;
- **Enabling Low Latency for ECQF based Flow Aggregation Scheduling in Time-Sensitive Networking**
  Ping Liu, Xiaoqin Feng, Yanying Ma, Fengyuan Ren, Lanzhou University, Lanzhou, China; Tong Zhang, Nanjing University of Aeronautics and Astronautics, Nanjing, China;

- **Safe Controller Synthesis for Nonlinear Systems via Reinforcement Learning and PAC Approximation**
  Xia Zeng, ; Zhiming Liu, Southwest University, Chongqing, China; Banglong Liu, Zhengfeng Yang, East China Normal University, Shanghai, China; Zhenbing Zeng, Shanghai University, Shanghai, China;
- **SAS - A Framework for Symmetry-based Approximate Synthesis**
  Niklas Jungnitz, Oliver Keszocze, Friedrich-Alexander-Universitat Erlangen-Nurnberg (FAU), Erlangen, Germany

GENERATIVE AI FOR CHIP DESIGN: GAME CHANGER OR DAMP SQUIB

Time: 3:30 PM – 5:30 PM
Session Type: Research Panel
Topic Area(s): AI
Room: 3014, 3rd Floor

Organizer: Siddharth Garg, New York University, USA

Moderator: Paul Franzon, North Carolina State University, Raleigh, USA

Description: Generative AI (GenAI) technologies for modalities including text, image, speech etc., are poised for huge practical impact in a range of industries. How will GenAI impact the EDA business, and perhaps conversely, does EDA have a role to play in advancing GenAI? Recent results suggest GenAI can indeed play a transformative role across the design flow from chip specification and verification, to pre- and post-silicon test, physical design and design for manufacturability, thereby improving designer productivity, time-to-market and design quality. Conversely, EDA can play a crucial role in addressing the massive training and inference costs of state-of-art trillion parameter or more GenAI models via pruning, specialization and acceleration. The panel will seek to address several key questions the about the role of GenAI and EDA namely:

1. Can GenAI design a full chip? Intentionally provocative, panelists will be asked whether GenAI methods alone, or with limited supervision, can translate natural language design intent to high-quality GDSII, along with test and verification procedures? What role will human expertise, experience and intuition play in a GenAI driven flow, and which parts can be truly automated? In sum, what are the killer applications for GenAI in chip design?
2. Specialized vs. general-purpose foundation models for chip design? Generalized foundation models like GPT-4, Bard etc. have shown exceptional abilities to generalize to unseen tasks, including potentially RTL code and EDA script generation. Will these massive foundation models suffice or do we need smaller and specialized foundation models for hardware design? Specialized models can improve performance on hardware=-specific tasks, in addition to having manageable training and inference costs.
3. Open- vs. closed-sourced datasets and models for hardware? Many semiconductor companies have massive internal datasets that can be used to train foundation models for hardware, but these models will likely not be released publicly due to IP issues. Unlike for software, open datasets of hardware are scarce—for example, Verilog is only 0.004% of the code on GitHub. Are there avenues for training large open-source GenAI models for chip design, or do we expect these models to be internal and/or black-boxed?
4. Regulatory, legal, safety and robustness issues? The recent Executive Order by the Biden administration requires, amongst other things, the development of " standards, tools, and tests to help ensure that AI systems are safe, secure, and trustworthy." What does this mean for GenAI models in the EDA context? Models trained on open-source datasets must additionally worry about copyright and IP violation issues, user privacy and the “right to be forgotten" and additional concerns about inadvertent or malicious backdoors in ML models.

Presenters: Vidya A. Chhabria, Arizona State University, Tempe, AZ; Subhasish Mitra, Stanford University, Stanford, CA; Amir Yazdanbakhsh, Google, Mountain View, CA; Erik Berg, Microsoft, Portland, OR; Stelois Diamantidis, Synopsys, Sunnyvale, CA; Yong Liu, Cadence Design Systems, Inc., Cupertino, CA

DESIGN AUTOMATION FOR AUTONOMOUS SYSTEMS

Time: 3:30 PM – 5:30 PM
Session Type: Special Session (Research)
Topic Area(s): Autonomous Systems
Room: 3006, 3rd Floor

Session Chair: Yanzhi Wang, Northeastern University

Organizer(s): Jie Gu, Northwestern University

Description: Autonomous systems are poised to transform many application domains, such as manufacturing, transportation, healthcare, agriculture, space and ocean exploration, and retail and services. However, their designs face tremendous challenges across heterogeneous components and multiple system layers. At the function level, the integration of sensing, computing and communication is critical for a successful mission. At the performance metric level, the existence of multiple factors, such as efficiency, cost, safety and security call for different optimization and trade-off strategies in practice. At the technology level, full stack integration, including programming, operating system, architecture and hardware, is required to form a functional autonomous agent. At the algorithm level, multiple choices for different processing stages co-exist and are available in different practical applications. At the computing platform level, CPU, GPU, ASIC, and FPGA play different roles in varying scenarios. Such heterogeneity from different aspects leads to a huge design space for autonomous systems, and it is becoming increasingly more complex with the adoption of advanced machine learning techniques. This brings a precious research opportunity for the Design Automation community. To efficiently design autonomous systems with multifaceted nature, interdisciplinary knowledge and collaboration is fundamentally required. Meanwhile, unlike the electronics industry, to date there lacks principled methodologies for design space exploration of autonomous system design. The EDA-style toolset that is critical for the scalable growth of semiconductor technology, is missing for autonomous machines. This special session invites four confirmed speakers with extensive expertise in autonomous system design. The speakers will discuss pressing challenges and promising solutions across the design of algorithm, software, and hardware layers, with focus on system efficiency, cost, safety, and robustness.

- **Algorithm and Hardware Co-Design for Energy-Efficient Neural SLAM**
  Qi Zhu, Northwestern University
- **Using Causal Information to Enable More Efficient Robot Operation**
  R. Iris Bahar, Colorado School of Mines
- **The Magnificent Seven Challenges and Opportunities in Domain-Specific Accelerator Design for Autonomous Systems**
  Vijay Janapa Reddy, Harvard University
- **Automatic Hardware/Software Design for High-Speed Autonomous Unmanned Aerial Vehicles Guided by a Flight Model**
  Hongyang Jia, Tshinghua University

EMERGING CHIPLET ECOSYSTEMS ENABLE OPTIMIZED MULTI-VENDOR DESIGNS

Time: 4:15 PM – 4:45 PM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Many hardware and silicon designers consider chiplets a critical enabler for more capable and cost-efficient systems. Chiplets are well established amongst large players that control all components/aspects of a design (i.e., single vendor), and the allure of a "plug and play" chiplet market has garnered significant attention and investment from the industry. Although the industry needs to address some technical and business hurdles before that vision comes to fruition, OEMs and chipmakers can realize most of the benefits of chiplet-based designs today. Specifically, small groups of companies with aligned product strategies and (typically) complementary expertise are forming multi-vendor ecosystems. Within these ecosystems, the companies can coordinate the functionality, requirements, and interfaces of each chiplet (and, of course, the die-to-die interconnects that glue them together) to meet the needs of a specific product or product family. This talk describes chiplet interconnect solutions—die-to-die PHY and link layer—that support all three use cases (single-vendor, multi-vendor ecosystem, and plug-and-play). It outlines how OEMs and chip makers can successfully navigate a multi-vendor ecosystem approach to implement chiplet-based designs today.

Speakers: Elad Alon, John Lupienski, Ronen Shoham, Blue Cheetah Analog

ON CLOUD SEMICONDUCTOR VIRTUAL TWIN EXPERIENCE UNIVERSE

Time: 5:00 PM – 5:30 PM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Global semiconductor chips shortage disrupted the production in recent years affecting a wide range of industries. Despite the prevailing difficulties in keeping up with demand, and geo-politics that require moving from a global to sovereign supply chain. The semiconductor ecosystem is actively pursuing future solutions, including establishing new manufacturing sites and preparing the upcoming workforce. All these solutions are time taking and costly. In this scenario virtual twin, experience looks like a plus which can help companies bring down the cost and efforts. In this session, we will explain our cloud based semiconductor virtual twin experience to highlight how it can enable end-to-end digital continuity from chips to fab. This approach is applicable to the entire semiconductor ecosystem from design, to manufacturing, to material, to process, to equipment, to cleanroom/fab, which scales collaborative innovation across all the stages and all stakeholders. The following scenarios are covered by our solutions:

- from chips to systems
- project planning, requirement, system architecture and validation
- from lab to fab
- material, manufacturing process, equipment, process flow and operation

We will present how digital continuity and traceability utilize the data analytics and advanced cutting edge modeling techniques to enhance decision-making and minimize potential risks in semiconductor virtual twin experience universe. In addition, we will see how a model based innovation platform on IP secure cloud enables

- Virtualization of physical experimentation and tests
- Industry ecosystem collaboration, fostering private-public partnership between different IDM, OEM, Foundry, fabless, academia, research, assembly and test, to work together

Speakers: Manuel Rei, John Maculley, Smriti Joshi, Dassault Systemes

TUESDAY ENGINEERING TRACKS POSTERS RECEPTION

Time: 5:00 PM – 6:00 PM
Session Type: Engineering Tracks Posters
Room: Exhibit Hall, 2nd Floor

ACCELERATED DESIGN RULE LEARNING FOR SILICON PHOTONICS

Apoorva Vakil, Romain Feuillette, GlobalFoundries, Clifton Park, NY

ACCELERATING IO LIBERTY GENERATION THROUGH ML BASED SOLUTION

Pawan Verma, Anil-kumar Dwivedi, Saurabh Srivastava, STMicroelectronics Pvt. Ltd., Bengaluru, India; Ajay Kumar, Siemens, London, United Kingdom, Wei-Lii Tan, Siemens, Austin, TX

ADVANCED STATIC METHODOLOGY FOR COMPLETE CONNECTIVITY AND GLITCH SIGNOFF

Abhishek Ghate, HCL Technologies; Saurav Choudhary, Vikas Sachdeva, Real Intent Inc.

ADVANCEMENTS IN SOURCE SYNCHRONOUS DESIGN IMPLEMENTATION: AN EDA PERSPECTIVE

Keshavkumar Durgakeri, Subba Ramkumar Reddy Annapalli, Ponnada Naidu, Intel, Bengaluru, India

AI-ENHANCED AUTOMATED OPTIMIZATION WORKFLOW FOR HBM INTERCONNECT ON INTERPOSER

Shineng Ma, Hao Hu, Bin Yu, Keqing Ouyang, Sanechips Technology Co.,Ltd, Shenzhen, China; Rodger Luo, Ansys, Shanghai, China

ANALYSIS OF RARE FAILURE EVENTS: AN IMPROVED SCALED-SIGMA SAMPLING METHOD

Ning Lu, IBM, Yorktown Heights, NY

ARCHITECTURE AREA EVALUATION TOOL

Ashishkumar Pal, Adarsh TR, Texas Instruments (India) Pvt. Ltd., Bengaluru, India; Kavithaa Rajagopalan, Eindhoven University of Technology, Eindhoven, Netherlands

ASK-EDA: A CONVERSATIONAL AGENT FOR TOOLS, METHODOLOGY, TECHNOLOGY AND DESIGN PROBLEMS

Michael Kazda, Bradley Sears, Nicholas Shropshire, Luyao Shi, IBM Research, Yorktown Heights, NY

AUTO GROUPING AND IMPROVEMENT OF IR CRITICAL REGIONS USING UNSUPERVISED LEARNING

Arpan Bhowmik, Abhishek Mahesh Chinchani, Rishikanth Mekala, Samsung, Goda Ananth Somayaji, Samsung, Bengaluru, India

AUTOMATED CONSTRAINT PROMOTION METHODOLOGY FROM IP TO SOC FOR COMPLEX DESIGNS

Mallik Devulapalli, Rimpy Chugh, Synopsys

AN AUTOMATED SOLUTION FOR STREAMLINING QUALIFICATIONS OF CONNECTIVITY AND DRC ACROSS DIVERSE 3DIC PACKAGING TECHNOLOGIES

Taehyung Lee, Woonggyu Lee, Minkyung Kim, Jihoon Park, Hyojin Kim, Changyoon Shin, Jiseon Lee, Yoojeong Yang, Seungjae Jung, Jongkoo Kang, Samsung, Seoul, South Korea; Ahmed Saleh, Siemens, Richmond, VA

AUTONOMOUS POWER SEQUENCE VALIDATION SOLUTION FOR I/O USING SOLIDO DESIGN ENVIRONMENT

Rravinder Kumar, STMicroelectronics Pvt. Ltd., Bengaluru, India; Fouad Mkalech, Eric Mammi, Siemens, Grenoble, France; Vani Priya, Siemens, Delhi, India

AVOIDING CDC BUGS INTRODUCED DURING SYNTHESIS OPTIMIZATIONS AND NETLIST TRANSFORMATIONS

Suresh Barla, Paras Mal Jain, Gunjan Mamania, Kenneth Trejos, Synopsys, Santa Clara, CA; Harish Aepala, Anshul Bansal, Meta, Sunnyvale, CA;

TUESDAY ENGINEERING TRACKS POSTERS RECEPTION (CONTINUED)

CHALLENGES AND IMPROVEMENTS IN STANDARDCELL OPENACCESS CONTENT FOR ANALOG DESIGN

Anuradha Ray, STMicroelectronics, Noida, India; Frederic Avellaneda, STMicroelectronics, Grenoble, France; Stephan Weber, STMicroelectronics, Bayern, Germany

CHALLENGES FACED IN FORMAL BASED MSI: TACKLE FORMAL PROBLEM WITH A FORMAL SOLUTION

Abhinav Parashar, Ayush Jodh, Parthasarathy Ramesh, Harish Maruthiyodan, Texas Instruments (India) Pvt. Ltd., Bengaluru, India;

COVERAGE-BASED FV SIGNOFF – THE COMPLETE CLEANUP METHODOLOGY

Gilboa Alin. Daher Kaiss, Anmol Patel, Aarti Gupta, Gavriel Gavrielov, Intel

CRITICAL CORNERS SELECTION FOR STANDARD CELLS LVF CHARACTERIZATION USING AI

Aravind Radhakrishnan Nair, Infineon Technologies, Munich, Germany, Ajay Kumar, Siemens, Wilsonville, OR

DASHBOARD MODEL FOR FOUNDRY EARLY NODE ASSESSMENTS USING SYNOPSYS DESIGN.DA

Luna Kang, Jayson Seo, Ann-Woo Lee, James Ban, Synopsys, Seoul, South Korea

A DATA-DRIVEN AUTOMATION METHOD OF LIBERTY MODEL CHARACTERIZATION FOR CUSTOM CELLS

Dongsub Yoon, Youngjin Ju, Hyojin Choi, Samsung, Seoul, South Korea

DESIGN METHODOLOGIES FOR MINIMIZING LOCAL ROUTING CONGESTIONS IN LOW-LEVEL METAL LAYERS

Daeyeon Kim, Hongseok Choi, Minkook Kim, Sangyun Kim, Samsung, Seoul, South Korea

DIGITAL CONTINUITY FROM SEMICONDUCTOR EBOM TO MBOM AND BILL OF PROCESS

Smriti Joshi, Manuel Rei, Dassault Systèmes, Paris, France

DVD-AWARE STA AND ITS SILICON CORRELATION RESULTS ON 10NM TEST CHIP

Jongyoon Jung, Hyun-seung Seo, Byunghyun Lee, Samsung, Seoul, South Korea; Rajat Kukreja, Ajay Sahoo, Ji-Hun Kim, Dae-Hun Jung, Aniket Deshmukh, Cadence Design Systems, Inc., Bengaluru, India

EARLY DETECTION OF LOW POWER RELATED ISSUES USING FORMAL VERIFICATION

Andrea Lopinto, Paola Baldrighi, STMicroelectronics, Torino, Italy

EARLY VALIDATION OF RANDOM TB USING FORMAL TECHNOLOGY

Euibong Jung, Samsung, Seoul, South Korea

AN EFFECTIVE HIERARCHICAL TOP SCOPE SIGNAL EM FLOW FOR CLOSING LARGE SOC DESIGNS

Adish Mehta, Umberto Garofano, Marvell, Cupertino, CA; Rakesh Reddy, Marvell, Bengaluru, India; Ratnakar Bhatnagar, Cadence Design Systems, Inc., Bengaluru, India; Steve Harvey, Cadence Design Systems, Inc., San Jose, CA

AN EFFICIENT EARLY THERMAL MANAGEMENT SOLUTION IN 3DIC DESIGN

Ping Ding, Guohua Zhou, Keqing Ouyang, Sanechips Technology Co.,Ltd, Shenzhen, China; Li Zou, Shuqiang Zhang, Ansys, Shanghai, China

AN EFFICIENT QA METHODOLOGY FOR SRAM LIBRARIES

Hiroaki Koizumi, Shuji Katayama, Renesas Electronics Corporation, Tokyo, Japan; Siddharth Ravikumar, Siemens, Tokyo, Japan;

ELEVATING BFM CAPABILITIES:

Krunal Patel, Shubham Agarwal, Cadence Design Systems, Inc., Bengaluru, India;

EMPOWERING CDC ANALYSIS METHODOLOGY WITH ROOT CAUSE ANALYSIS

Abdul Moyeen, Siemens, Austin, TX; Manish Bhati, Siemens, Delhi, India
Enhancing and Accelerating Verification with Ad-hoc Python Scripting
Edoardo Bollea, Davide Sanalitro, STMicroelectronics, Torino, Italy

FLASH-BASED STORAGE SYSTEMS EXPLOITING THE DATA PERIOD FOR PERFORMANCE AND SECURITY ENHANCEMENT

Jung-Hoon Kim, Suhwan Kim, Daeun Oh, Samsung, Seoul, South Korea

FORMAL TOOL KIT – A QUICK SETUP SOLUTION FOR FORMAL ANALYSIS

Phanindra Ramanujapuram, Rathnakar Madhukar Yerraguntla, NXP Semiconductors, Delhi, India

FUTURE PROOFING CHIPLET TESTBENCHES: RESILIENCE IN MULTIPROTOCOL ERA

Kilaru Vamsikrishna, Anunay Bajaj, Shaikh Salehabibi, Cadence Design Systems, Inc., Bengaluru, India;

GPU ACCELERATED HARMONIC BALANCE SPICE SIMULATION

Qikun Xue, NVIDIA, San Jose, CA; Chen Zhao, Empyrean Technology, Santa Clara, CA

HETEROGENEOUS 3DIC MULTI VOLTAGE TIMING SIGNOFF

Tusharkant Mishra, Ranjith V R, Damodaran Trikkadeeri, Samsung, Bengaluru, India; Santosh Varanasi, Synopsys, Noida, India

A HEURISTIC-BASED ROUTING METHODOLOGY FOR BLOCK-LEVEL MEMORY LAYOUT ROUTABILITY ENHANCEMENT

Sichan Kim, Seunghwan Lee, Samsung, Seoul, South Korea

TUESDAY ENGINEERING TRACKS POSTERS RECEPTION (CONTINUED)

HIGH COVERAGE QA FOR PROCESS VARIABILITY COMPENSATION IN LVS RULE DECK

Heejae Lim, Jaeyoung So, Minho Jung, Jimin Yeo, Yunseong Lee, Bonhyuck Koo, Yongseok Lee, Samsung, Seoul, South Korea; Ahmed Saleh, Siemens, Richmond, VA; Mohamed Alimam, Siemens, Tokyo, Japan

IMPLEMENTING WORLD'S FIRST FULLY INTEGRATED SOC SOLUTION FOR DIRECT-TO-SATELLITE IOT CONNECTIVITY

Sushanta Sarmah, Orca Radio Systems Pvt Ltd, Bengaluru, India; Alpesh Kothari, Siemens, Delhi, India; Raghu Ram Gude, Siemens, Austin, TX

INTEGRATED CALCULATION OF CAPACITANCES FOR IMAGE SENSOR ARRAYS AND OTHER PERIODIC DESIGNS

Valery Axelrad, SEQUOIA Design Systems. Inc., Woodside, OR; Ognjen Milic, Independent, Bengaluru, India

LINKED LIST PROOF ACCELERATOR

Arjun Kumar, Broadcom, San Jose, CA

MACHINE LEARNING OPTIMIZATION SWITCH CELLS.

Sungsu Byun, Samsung, Seoul, South Korea

MACHINE LEARNING-BASED FEASIBILITY ESTIMATION OF DIGITAL BLOCKS FOR IMPROVED PRODUCTIVITY IN ANALOG-ON-TOP BACK-END DESIGN FLOWS

Gabriele Faraone, Eugenio Serianni, Dario Licastro, Nicola DiCarolo, Michelangelo Grosso, Giovanna Franchino, STMicroelectronics, Torino, Italy

MATCHED PLACEMENT AND ROUTING USING SYNCHRONIZED UNIT CELL ARRAY

Priyanka Madaan, Avinash Tripathi, NXP Semiconductors, Delhi, India; Akshita Bansal, Ashwani Sanwal, Cadence Design Systems, Inc., Bengaluru, India

MODEL BASED SYSTEM SEMICONDUCTOR ENGINEERING

Smriti Joshi, Rosa Gragossian, Dassault Systèmes, Paris, France

A MODULE BASED AUTOMATION FOR AXI PERFORMANCE MONITORING, PERFORMANCE EXTRACTION AND PROTOCOL CHECKING

Naveen Srivastava, Amresh Lenka, Sekhar Dangudubiyyam, Samsung, Bengaluru, India

NAVIGATING INSTRUCTION LENGTH DECODE: TAP INTO IP USING THREE PRONGED FV TRIDENT

Vedprakash Mishra, Intel, Bengaluru, India; Aarti Gupta, Intel, Cupertino, CA

A NEW APPROACH TO EFFICIENT PRELIM PACKAGE GENERATION FOR FASTER SOC IMPLEMENTATION

Bhupendra Singh, Shoikat Das, Saurabh Srivastava, Anil Dwivedi, STMicroelectronics, Noida, India

NEW SOC CREATION FLOW BASED ON EXTRACTION AND RECREATING FROM PREVIOUS SOC

Maël Rabé, Chouki Aktouf, Defacto Technologies, Grenoble, France

NEXT-GEN COMPREHENSIVE IR ANALYSIS WITH ANSYS SIGMAAV

Pranav Ranganathan, Medha Kulkarni, Chip Stratakos, Microsoft, Mountain View, CA; Veshal Sridhar, Mallik Vusirikala, Ansys, San Jose, CA

A NOVEL AUTOMATION FLOW TO GENERATE SV-UVM TESTBENCH WITH INTEGRATED BFMS

Parthasarathy Ramesh, Sagar Jogur, Raminder Kaur, Atul Lele, Texas Instruments

A NOVEL FLOW TO VERIFY SOC INTEGRATION WITH FORMAL PROPERTY VERIFICATION

David Vincenzoni, Marcello Dusini, STMicroelectronics, Torino, Italy

NOVEL PREPROCESSING TECHNIQUE FOR DATA EMBEDDING IN ENGINEERING CODE GENERATION USING LARGE LANGUAGE MODELS

Yu-Chen Lin, Jyh-Shing Jang, National Taiwan University, Taipei, Taiwan; Akhilesh Kumar, Norman Chang, Wen-liang Zhang, Muhammad Zakir, Ansys, San Jose, CA;

PEAK POWER OPTIMIZATION USING ACTIVE DATAPATH OPERATOR PROFILING

Vijay Tayal, Sanchita Gupta, Amit Dey, Anil Mishra, Mohammad Saif Ansari, Manish Kumar, Siemens, Delhi, India; Hicham Anbar, Siemens, Marrakech, Morocco

PHYSICAL DESIGN WITH INTELLIGENCE

Bindu Rao, Jagadeesh Gnanasekaran, Prasenjit Ray, Sai Prashant, Anand Kumaraswamy, Srinivas Jammula, Intel, Bengaluru, India

PLUG-N-PLAY TESTBENCH ENVIRONMENT FOR ARM CORESIGHT SOC-400

Sowmya V M, Dhaval Panchal, Lalithraj Mailappa, Subramanian R, Naveen Srivastava, Sekhar Dangudubiyyam, Samsung, Bengaluru, India

POWERDASH: A COMPREHENSIVE FRAMEWORK FOR SOC POWER ANALYSIS AND TRACKING

Vivek Joshi, Atman Kar, Texas Instruments (India) Pvt. Ltd., Bengaluru, India

A PVT-ROBUST DESIGN

Chaerin Hong, Luca Ramini, Marco Fiorentino, Raymond Beausoleil, Hewlett Packard Enterprise, Santa Clara, CA; Ahsan Alam, Zeqin Lu, Ansys, Vancouver, Canada;

RDL AND BUMP AUTOMATION FOR EARLY EMIR ANALYSIS IN 2.5D, 3D AND SINGLE DIE DESIGNS USING REDHAWK-SC DESIGN ECO'S

Arpan Bhowmik, Samsung, Bengaluru, India; Raja Rama Chandra Rao, Samsung, Bengaluru, India; Rishikanth Mekala, Samsung, Bengaluru, India; Goda Ananth Somayaji, Samsung, Bengaluru, India

WORK-IN-PROGRESS POSTERS (CONTINUED)

RESOLVING THE SEED PROMOTION DUE TO DEVICE LAYERS DERIVATION
Prachi Mrudula, Atul Bhargava, STMicroelectronics, Noida, India; Gazal Singla, Siemens, Delhi, India

RISK MANAGEMENT IN VOLUME DIAGNOSTICS
Pitchumani Guruswamy, Silicon Support Solutions (OPC) Private Limited, Bengaluru, India; Vishnu Raj, Independent, Bengaluru, India

*ROW-BASED PLACEMENT AND LEGALIZATION FOR MIXED SIGNAL POWER DELIVERY IP IN MEMORY
Jeongyoon Lee, Kyeongrok Jo, Seunghwan Lee, Seungkwang Hong, Heejin Bae, Jiwon Woo, Youngwook Kim, Jungyun Choi, Samsung, Seoul, South Korea

SAFEGUARDING DATAPATH SECURITY REQUIREMENTS THROUGH FORMAL VERIFICATION
Nicolae Tusinschi, Keerthi Devarajegowda, SEDA, Nuremberg, Germany

SCALABLE MODELING OF DYNAMIC VOLTAGE COMPRESSION ON TIMING
Tim Helvey, Marvell, Cupertino, CA

SIMULATION AND MEASUREMENT OF MOMCAP BREAKDOWN RISK BASED ON TCAD
Kun Zhou, Jian Wang, Tingting Hun, Guohua Zhou, Keqing Ouyang, Sanechips Technology Co.,Ltd, Shenzhen, China

SOLVING THE ANTENNA DEBUG CHALLENGE IN PHYSICAL DESIGN VERIFICATION
Rahul Sai T Govindaswamy, Google, Mountain View, CA; Nermeen Hossam, Siemens, Cairo, Egypt, Anish Padhi, Gurpreet Lamba, Siemens, Delhi, India; Karishma Qureshi, Rakesh Reddy Katukuri, Google, Hyderabad, India

SSN AND EMA BUS PATH AUTOMATION
Greg Ford, Trinath Harikrishna, Marvell, Cupertino, CA

A SOLUTION FOR OPTIMIZING CUSTOMERIZED-MMB
Feilong Pan, Minqiang Peng, Keqing Ouyang, Guohua Zhou, Fengfeng Tang, Synopsys, Shanghai, China

TAPEOUT DATA PRESERVATION AND AUTOMATIC ARCHIVAL TAGGING FOR OPTIMAL DISK SPACE MANAGEMENT
Yamini Ravishankar, Marvell, Cupertino, CA

TIMING TAKEDOWN REPORTS 3
Lukas Pettersson, Marvell, Cupertino, CA

TOWARDS A MEMORY-ADDRESS TRANSLATION REPRESENTATION SCHEME
Rathnakar Madhukar Yerraguntla, NXP Semiconductors, Delhi, India

TRUE-HYBRID SAAS CLOUD ARCHITECTURES FOR EDA WORKLOADS
Ravi Poddar, Amazon Web Services; Amit Varde, Nupur Bhonge, Keysight Technologies

AN UPTICK ON AUTOMOTIVE SAFETY SOLUTIONS USING CADENCE IMPLEMENTATION TOOLS
Jitendra Jain, Ashwin Ramamurthy, Cadence Design Systems, Inc., Bengaluru, India

VIRTUAL INSTRUMENTATION BASED PREDICTIVE CHECKS FOR SHIFT-LEFT LOW POWER VERIFICATION
Sachin Bansal, M.Vaishnavi Reddy, Nupur Gupta, Vishal Keswani, Amit Goldie, Manish Goel, Synopsys, Noida, India; Yi Liu, Synopsys, Shanghai, China; Vijay Poosa, Synopsys, Santa Clara, CA;

WATSONX AND DDB FOR AI BASED DESIGN ANALYTICS AND VISUALIZATION
Kerim Kalafala, Nathaniel Hieter, Douglas Keller, IBM, Yorktown Heights, NY

WORK-IN-PROGRESS POSTERS

Time: 6:00 PM – 7:00 PM
Session Type: Work-in-Progress Posters
Room: 2nd Floor Lobby

ADAPTIVE NEUROSURGEON: DNN COMPUTING LATENCY MINIMIZATION FOR MOBILE EDGE INTELLIGENCE
Gang Wu, Qianru Wang, Biao Hu, China Agricultural University, Beijing, China

ADDITIVE PARTIAL SUM QUANTIZATION
Pingcheng Dong, Yonghao Tan, Dong Zhang, Yongkun Wu, Xijie Huang, Shi-Yang Liu, Kwang-Ting Cheng, Hong Kong University of Science and Technology, Hong Kong, Hong Kong; Yu Liu, Xuejiao Liu, Peng Luo, Luhong Liang, AI Chip Center for Emerging Smart System (ACCESS), Hong Kong, China; Fengwei An, Southern University of Science and Technology, Shenzhen, China;

ADDRESSING THE DIVERSITY IN AI COMPUTING: AN ON-CHIP PROGRAMMABLE ACCELERATOR
Gopikrishnan Raveendran Nair, Yu Cao, University of Minnesota, Minneapolis, MN ; Fengyang Jiang, Jeff Zhang, Arizona State University, Tempe, AZ; Jae-sun Seo, Cornell Tech, New York, NY;

AIDAC: A LOW-COST IN-MEMORY COMPUTING ARCHITECTURE WITH ALL-ANALOG MULTIBIT COMPUTE AND INTERCONNECT
Zihao Xuan, Song Chen, Kang Yi, University of Science and Technology of China; Hefei, China

AMARETTO: ENABLING EFFICIENT QUANTUM ALGORITHM EMULATION ON LOW-TIER FPGAS
Christian Conti, Deborah Volpe, Mariagrazia Graziano, Maurizio Zamboni, Giovanna Turvani, Politecnico di Torino, Italy

AN ANALYTICAL FIDELITY MODEL FOR READOUT CIRCUITRY WITH MULTIPLE CO-EXISTING NON-IDEALITIES FOR SUPERCONDUCTING QUANTUM COMPUTING
Yao Tong, Quan Chen, Southern University of Science and Technology, Shenzhen, China

WORK-IN-PROGRESS POSTERS (CONTINUED)

ANALYTICAL MODELING AND ELECTRO-THERMAL BENCHMARKING OF 2.5D/3D HETEROGENEOUS INTEGRATION FOR AI COMPUTING

Zhenyu Wang, Jingbo Sun, Vidya A. Chhabria, Jeff Zhang, Chaitali Chakrabarti, Arizona State University, Tempe, AZ; A. Alper Goksoy, Umit Ogras, University of Wisconsin, Madison, WI; Sumit Mandal, Indian Institute of Science, Bangalore, India; Jae-sun Seo, Cornell Tech, New York, NY; Yu Cao, University of Minnesota, Minneapolis, MN

AN APPLICATION OF INFORMATION FLOW TRACKING TO HARDWARE TROJAN DETECTION

Ryoichi Isawa, Nobuyuki Kanaya, Daisuke Inoue, National Institute of Information and Communications Technology, Koganei, Japan

APPROX-T: DESIGN METHODOLOGY FOR APPROXIMATE MULTIPLICATION UNITS VIA TAYLOR-EXPANSION

Shang-shang Yao, Qing-jie Lang, Li Shen, Kai Lu, National University of Defense Technology, Changsha, China

ARCHITECTURAL EXPLORATION OF APPLICATION-SPECIFIC RESONANT SRAM COMPUTE-IN-MEMORY (RCIM)

Dhandeep Challagundla, Riadul Islam, University of Maryland, Baltimore, MD; Ignatius Bezzam, Rezonent Inc., Milpitas, CA;

ARE ADVERSARIAL EXAMPLES SUITABLE TO BE TEST SUITES FOR TESTING DEEP NEURAL NETWORKS

Wei Kong, AOMS, Nanjing, China

ATHENA: ADD MORE INTELLIGENCE TO RMT-BASED NETWORK DATA PLANE WITH LOW-BIT QUANTIZATION

Yunkun Liao, Hanyue Lin, Jingya Wu, Wenyan Lu, Xiaowei Li, Guihai Yan, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

AUTOFLOW: INFERRING MESSAGE FLOWS FROM SYSTEM COMMUNICATION TRACES

Bardia Nadimi, Hao Zheng, University of South Florida, Tampa, FL

Bayesian Learning-driven Memory Design Exploration with Automated Circuit Variant Generation

Dongho Kim, Seokhun Kim, Junseo Lee, Hongwon Kim, Sangheon Lee, Jihwan Park, Hanwool Jeong, Kwangwoon University, Seoul, South Korea

B-RING:AN EFFICIENT INTERLEAVED BIDIRECTIONAL RING ALL-REDUCE ALGORITHM FOR GRADIENT SYNCHRONIZATION

Ruixing Zong, Jiapeng Zhang, Guoqing Xiao, Zhuo Tang, Kenli Li, Hunan University, Changsha, China

CDA: COLLABORATIVE COMPUTING USING CENTRALIZED-DISTRIBUTED ARCHITECTURE FOR SMART SENSING

Erxiang Ren, Li Luo, Beijing Jiao Tong University, Beijing, China; Cheng Qu, The Chinese University of Hong Kong, Shenzhen, China; Yonghua Li, Beijing University of Posts and Telecommunications, Beijing, China; Zheyu Liu, Qi Wei, Fei Qiao, Tsinghua University, Beijing, China; Xinghua Yang, Beijing Forestry University, Beijing, China;

CELLREJUVO: RESCUING THE AGING OF 3D NAND FLASH CELLS WITH DENSE-SPARSE CELL REPROGRAMMING

Han-Yu Liao, Yi-Shen Chen, Jen-Wei Hsieh, National Taiwan University of Science and Technology, Taipei, Taiwan; Yuan-Hao Chang, Academia Sinica, Taipei, Taiwan; Hung-Pin Chen, Innodisk Corporation, New Taipei, Taiwan

COOLING THE CHAOS: MITIGATING THE EFFECT OF THRESHOLD VOLTAGE VARIATION IN CRYOGENIC CMOS MEMORIES

Rakshith Saligram, Suman Datta, Arijit Raychowdhury, Georgia Institute of Technology, Atlanta, GA; Amol Gaidhane, Arizona State University, Tempe, AZ; Yu Cao, University of Minnesota, Minneapolis, MN;

DEPUTY NOC: A CASE OF LOW COST NETWORK-ON-CHIP FOR NEURAL NETWORK ACCELERATIONS ON GPUS

Khoa Ho, Siamak Biglari, Justin Garrigus, Hui Zhao, University of North Texas, Denton, TX

AN EFFECTIVE TIMING DRIVEN PLACEMENT WITH ACCURATE DIFFERENTIABLE TIMING APPROXIMATION INTEGRATION

Xu He, Renjun Zhao, Chenjing Yang, Yushan Wang, Hunan University, Changsha, China; Yao Wang, National University of Defense Technology, Changsha, China; Peiyu Liao, Bei Yu, The Chinese University of Hong Kong, Hong Kong; Yibo Lin, Peking University, Beijing, China;

EFFICIENT SYNAPTIC DELAY ACCELERATION IN DIGITAL EVENT-DRIVEN NEUROMORPHIC PROCESSORS

Roy Meijer, Interuniversity Microelectronics Centre, Eindhoven, Netherlands; Paul Detterer, Amirreza Yousefzadeh, Guangzhi Tang, Yingfu Xu, Mario Konijnenburg, Manolis Sifalakis, imec, Eindhoven, Netherlands; Alberto Patiño-Saucedo, Instituto de Microelectrónica de Sevilla, Spain, Kanishkan Vadivel, Manil Dev Gomony, Federico Corradi, Eindhoven University of Technology, Eindhoven, Netherlands;

ELF: EFFICIENT LOGIC SYNTHESIS BY PRUNING REDUNDANCY IN REFACTORING

Dimitrios Tsaras, Lei Chen, Xing Li, Weihua Sheng, Mingxuan Yuan, Huawei, Hong Kong, Hong Kong; Zhiyao Xie, Hong Kong University of Science and Technology, Hong Kong, Hong Kong;

ENABLING FAST 2-BIT LLM ON GPUS: MEMORY ALIGNMENT, SPARSE OUTLIER, AND ASYNCHRONOUS DEQUANTIZATION

Jinhao Li, Jiaming Xu, Shan Huang, Jun Liu, Yaoxiu Lian, Guohao Dai, Shanghai Jiao Tong University, Shanghai, China; Shiyao Li, Yu Wang, Tsinghua University, Beijing, China;

ENHANCING PERFORMANCE OF DEEP NEURAL NETWORKS WITH A REDUCED RETENTION-TIME MRAM-BASED MEMORY ARCHITECTURE

Munhyung Lee, Taehan Lee, Junwon Yeo, Hyukjun Lee, Sogang University, Seoul, South Korea

ESCAPING LOCAL OPTIMA IN GLOBAL PLACEMENT

Ke Xue, Xi Lin, Yunqi Shi, Chao Qian, Nanjing University, Nanjing, China; Shixiong Kai, Siyuan Xu, Huawei, Hong Kong, Hong Kong,

WORK-IN-PROGRESS POSTERS (CONTINUED)

ESFA: AN EFFICIENT SCALABLE FFT ACCELERATOR DESIGN FRAMEWORK ON VERSAL AI ENGINE

Hao Yang, Linfeng Du, Wei Zhang, Hong Kong University of Science and Technology, Hong Kong, Hong Kong

EXPLORING DISTRIBUTED CIRCUIT DESIGN USING SINGLE-STEP REINFORCEMENT LEARNING

Jiayu Li, Syracuse University, Syracuse, NY; Masood Mortazavi, Ning Yan, Futurewei Technologies, Santa Clara, CA;

FASTSAMPLE: ACCELERATING DISTRIBUTED GRAPH NEURAL NETWORK TRAINING FOR BILLION-SCALE GRAPHS

Hesham Mostafa, Intel, San Diego, ; Adam Grabowski, Intel, Lower Silesia, Poland, Md Asadullah Turja, University of North Carolina, Chapel Hill, NC; Juan Cervino, Alejandro Ribeiro, University of Pennsylvania, Philadelphia, PA; Nageen Himayat, Intel, Fremont, CA

FEI: FUSION PROCESSING OF SENSING ENERGY AND INFORMATION FOR SELF-SUSTAINABLE INFRARED SMART VISION SYSTEM

Xin Hong, Junkai Huang, Jinan University, Guangzhou, China; Haijin Su, Li Luo, Beijing Jiao Tong University, Beijing, China; Maimaiti Nazhamaiti, Tsinghua University, Beijing, China; Ce Zhang, Beihang University, Beijing, China; Yuzhao Yang, Guangdong University of Technology, Guangzhou, China; Qi Wei, Tsinghua University, Beijing, China; Zheyu Liu, MakeSens AI, Beijing, China; Fei Qiao, Beijing National Research Center for Information Science and Technology, Beijing, China

FROM RTL TO PROMPT: AN LLM-ASSISTED VERIFICATION METHODOLOGY FOR GENERAL PROCESSOR

Yifei Deng, Renzhi Chen, Jingyue Zhao, Huadong Dai, Lei Wang, Weixia Xu, Academy of Military Sciences; University of Electronic Science and Technology of China; Beijing, China; Chao Xiao, Zhijie Yang, Yuanfeng Luo, Yuhua Tang, National University of Defense Technology, Changsha, China;

FROM RTL TO SVA: LLM-ASSISTED GENERATION OF FORMAL VERIFICATION TESTBENCHES

Marcelo Orenes-Vera, Margaret Martonosi, David Wentzlaff, Princeton University, Princeton, NJ

A GENERAL PURPOSE IMC ARCHITECTURE WITH ADC-AWARED NEURAL NETWORKS

Min-Gwon Song, Shin-Uk Kang, Min-Seong Choo, Hanyang University, Ansan, South Korea

GNN-OPT: ENHANCING AUTOMATED CIRCUIT DESIGN OPTIMIZATION WITH GRAPH NEURAL NETWORKS

Kazuya Yamamoto, Nobukazu Takai, Kyoto Institute of Technology, Kyoto, Japan

GPU-ACCELERATED BFS FOR DYNAMIC NETWORKS

Filippo Ziche, Rosalba Giugno, Nicola Bombieri, University of Verona, Italy; Federico Busato, NVIDIA, San Jose, CA;

HARDWARE-ACCELERATED OPTIMIZATION OF DSP-BASED EQUALIZER IN HIGH-SPEED ADC-BASED RECEIVERS

Yoona Lee, Hanseok Kim, Jin-Seok Heo, Woo-Seok Choi, Seoul National University, Seoul, South Korea

A HARDWARE-AWARE FRAMEWORK FOR PRACTICAL QUANTUM CIRCUIT KNITTING

Xiangyu Ren, Antonio Barbalace, University of Edinburgh, United Kingdom; Mengyu Zhang, Shengyu Zhang, Yicong Zheng, Tencent Quantum Lab, Shenzhen, China;

HPA: A NOVEL IS-WS HYBRID DATA FLOW FOR PIM ARCHITECTURES

Yun Zhao, Sheng Ma, Heng Liu, Li Huang, Li Wu, Jian Zhang, Chun Zhang, Tie Li, National University of Defense Technology, ChangSha, China

A HIERARCHICAL DATAFLOW-DRIVEN HETEROGENEOUS ARCHITECTURE FOR WIRELESS BASEBAND PROCESSING

Limin Jiang, Yi Shi, Haiqin Hu, Qingyu Deng, Siyi Xu, Yintao Liu, Feng Yuan, Si Wang, Yihao Shen, Fangfang Ye, Shan Cao, Zhiyuan Jiang, Shanghai University, Shanghai, China

A HIGH-THROUGHPUT, ENERGY-EFFICIENT, AND CONSTANT-TIME IN-SRAM AES ENGINE WITH MASSIVELY-PARALLEL BIT-SERIAL EXECUTION

Andrew Dervay, Wenfeng Zhao Binghamton University, Binghamton, NY;,

HYFT: A RECONFIGURABLE SOFTMAX ACCELERATOR WITH HYBRID NUMERIC FORMAT FOR BOTH TRAINING AND INFERENCE

Tianhua Xia, Independent, San Diego, CA; Sai Qian Zhang, New York University, New York, NY

INTEGRATED MAC-BASED SYSTOLIC ARRAYS: DESIGN AND PERFORMANCE EVALUATION

Dantu Nandini Devi, Gandi Ajay Kumar, Bindu G Gowda, Madhav Rao, International Institute of Information Technology, Bangalore, India

INTERACTIVE VISUAL PERFORMANCE SPACE EXPLORATION OF ANALOG ICS WITH NEURAL NETWORK SURROGATE MODELS

Yannick Uhlmann, Till Moldenhauer, Jürgen Scheible, Reutlingen University, Reutlingen, Germany

LABIDUS: PRODUCTIVE ACCELERATOR DEVELOPMENT VIA CONFIGURABLE SOFT PROCESSORS

Gongjin Sun, Seongyoung Kang, Jane He, Sang-Woo Jun, University of California, Irvine, CA

LEAP: LAYOUT AWARE ESTIMATION OF ANALOG DESIGN PARASITICS

Prasanth Mangalagiri, Intel, Santa Clara, CA; Siddhartha Joshi, Intel, Hillsboro, ORON

LEARNED INDEX ACCELERATION WITH FPGAS: A SMART APPROACH

Geetesh More, University of New Brunswick, Canada

WORK-IN-PROGRESS POSTERS (CONTINUED)

LIBRA: COLLABORATING WITH BASIS-INVERTED CIRCUITS TO MITIGATE STATE-DEPENDENT ERRORS ON NISQ PROGRAMS

Enhyeok Jang, Youngmin Kim, Won Woo Ro, Yonsei University, Seoul, South Korea

MATHE: A NEAR-MAT PROCESSING IN-MEMORY ACCELERATOR FOR FULLY HOMOMORPHIC ENCRYPTION

Minxuan Zhou,; Yujin Nam, Pranav Gangwar, Weihong Xu, Arpan Dutta, Tajana Rosing, University of California, San Diego, CA; Chris Wilkerson, Intel, Hillsboro, OR; Rosario Cammarota, Intel, San Diego, CA; Saransh Gupta, IBM Research, San Jose, CA;

METHODOLOGY OF CONFIGURABLE MEMORY CONFLICT-FREE NUMBER THEORETIC TRANSFORM ACCELERATOR FOR FPGA PLATFORM

Xiangchen Meng, Yangdi Lyu, Hong Kong University of Science and Technology, Hong Kong, Hong Kong

MULTI-MODAL SIGNAL APPLIED NEUROMORPHIC PROVEN SNN MODEL FOR STRESS DETECTION

Ajay BS, Intel Technology India. Pvt. Ltd, Bangalore, India; Madhav Rao, International Institute of Information Technology, Bangalore, India

NAVIGATING THE CHALLENGES OF STATISTICAL FAULT INJECTION IN SRAM-FPGA

Trishna Rajkumar, Johnny Oberg, KTH Royal Institute of Technology, Stockholm, Sweden

NEUCORE: A NOVEL NEUROMORPHIC PROCESSOR ARCHITECTURE WITH ON-CHIP EVENT-DRIVEN LEARNING

Yi Wei, Zhijie Yang, Xun Xiao, Xiangyu Wang, Junbo Tie, Weixia Xu, Yuhua Tang, National University of Defense Technology, Changsha, China; Jingyue Zhao, Lei Wang, Huadong Dai, Defense Innovation Institute, AMS, Beijing, China; Zhenhua Zhu, Tsinghua University, Beijing, China

NEUROSTEINER: A GRAPH TRANSFORMER FOR WIRELENGTH ESTIMATION

Sahil Manchanda, Indian Institute of Technology, Delhi, India; Dana Kianfar, Markus Peschl, Romain Lepert, Michael Defferrard, Qualcomm, Amsterdam, Netherlands

A NOVEL METHOD TO ANALYSIS THE WAFER DEFECT PATTERNS USING AN IMAGE MATCHING ALGORITHM BASED ON DEEP NEURAL NETWORKS

Youngwook Kwon, Sumin Oh, HyunJin Kim, Dankook University, Yongin, South Korea

NVMXR: DESIGN SPACE EXPLORATION OF NON-VOLATILE MEMORY ARCHITECTURES FOR EDGE-XR SYSTEMS

Zihan Zhang, Marco Donato, Tufts University, Medford, MA

ODILO: ON-DEVICE INCREMENTAL LEARNING VIA LIGHTWEIGHT OPERATIONS

Qing Wang, Shengfa Miao, Mingxiong Zhao, Yunnan University, Kunming, China; Di Liu, Norwegian University of Science and Technology, Trondheim, Norway;

OPERATIONAL SAFETY IN HUMAN-IN-THE-LOOP HUMAN-IN-THE-PLANT AUTONOMOUS SYSTEMS

Ayan Banerjee, Aranyak Maity, Imane Lamrani, Sandeep Gupta, Arizona State University, Tempe, AZ

OPTIMAL TOFFOLI-DEPTH QUANTUM ADDER

Siyi Wang, Nanyang Technological University, Singapore, Ankit Mondal, Indian Institute of Technology, Delhi, India; Anupam Chattopadhyay, Nanyang Technological University, Singapore, Singapore

ON OPTIMIZATION OF ROBUSTNESS OF INTER- AND INTRA-CHIPLET INTERCONNECTION TOPOLOGY FOR MULTI-CHIPLET SYSTEMS

Miao Xu, South China University of Technology, Guangzhou, China; Xiaohang Wang, Zhejiang University, Hangzhou, China; Amit Kumar Singh, University of Essex, United Kingdom; Yingtao Jiang, Mei Yang, University of Nevada, Las Vegas, NV

OPTIMIZING HOMOMORPHIC CONVOLUTION FOR PRIVATE CNN INFERENCE

Hyeri Roh, Woo-Seok Choi, Seoul National University, Seoul, South Korea

A PARALLEL-TRIAL DOUBLE-UPDATE ANNEALING ALGORITHM FOR ENABLING HIGHLY-EFFECTIVE STATE TRANSITION ON ANNEALING PROCESSORS

Akira Hyodo, Satoru Jimbo, Daiki Okonogi, Genta Inoue, Thiem Chu, Masato Motomura, Kazushi Kawamura, Tokyo Institute of Technology, Yokohama, Japan

PIANIST: EFFICIENT QUANTUM CIRCUIT SIMULATION USING COMMERCIAL PROCESSING-IN-MEMORY SYSTEM

Dongin Lee, Enhyeok Jang, Seungwoo Choi, Junwoong An, Cheolhwan Kim, Won Woo Ro, Yonsei University, Seoul, South Korea

PIXELPRUNE: SPARSE OBJECT DETECTION FOR AIOT SYSTEMS VIA IN-SENSOR SEGMENTATION AND ADAPTIVE DATA TRANSFER

MohammadReza Mohammadi, Brendan Reidy, Ramtin Zand, University of South Carolina, Columbia, SC; Mehrdad Morsali, Shaahin Angizi, New Jersey Institute of Technology, Newark, NJ; Sepehr Tabrizchi, Arman Roohi, University of Nebraska, Lincoln, NE; Mohsen Imani, University of California, Irvine, CA;

THE POWER OF GRAPH SIGNAL PROCESSING FOR CHIP PLACEMENT

Yiting Liu, Fan Yang, Xuan Zeng, Li Shang, Fudan University, Shanghai, China; Hai Zhou, Northwestern University, Evanston, IL; Jia Wang, Illinois Institute of Technology, Chicago, IL;

PRE-SILICON POWER SIDE-CHANNEL LEAKAGE ASSESSMENT OF CRYSTALS-KYBER

Nashmin Alam, Tao Zhang, Farimah Farahmandi, University of Florida, Gainesville, FL

PRINCIPLES FOR ENABLING TEES ON DOMAIN-SPECIFIC ACCELERATORS

Aritra Dhar, Renzo Andri, Huawei, Zurich, Switzerland; Supraja Sridhara, Shweta Shinde, Srdjan Capkun, ETH Zürich, Zurich, Switzerland;

WORK-IN-PROGRESS POSTERS (CONTINUED)

PUSHING COMPUTING-IN-MEMORY TOWARDS COMPUTATIONAL STORAGE TO ACCELERATE IN-ORBIT REMOTE SENSING SATELLITE IMAGE PROCESSING

Hongyang Hu, Kai Xi, Jinshan Yue, Dashan Shang, Xiaoxin Xu, Jing Liu, Chunmeng Dou, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China; Shengwen Liang, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Zizhen Liu, Chinese Academy of Sciences, Beijing, China; Ming Liu, Fudan University, Shanghai, China

QUANTIFYING THE ENERGY EFFICIENCY BENEFITS OF MONOLITHIC 3D REFRESHLESS EMBEDDED-DRAM

David Kong, Shvetank Prakash, Georgios Kyriazidis, Vijay Janapa Reddi, Gage Hills, Harvard University, Cambridge, MA; Yasmine Omri, Harvard University, Cambridge, MA; Jedrzej Kufel, David Verity, Emre Ozer, Pragmatic, Cambridge, United Kingdom;

QUANTIZATION NOISE CANCELLATION THROUGH MODELLING OF NON-LINEARITIES IN SIGMA DELTA MODULATORS

Stijn Ringeling, Marco Fattori, Shagun Bajoria, Lucien Breems, Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, Netherlands Robert Rutten, NXP Semiconductors, Eindhoven, Netherlands;

A QUANTUM SOLVER FOR THE BOOLEAN MATCHING PROBLEM

Marco Venere, Alessandro Barenghi, Gerardo Pelosi, Politecnico di Milano, Italy

QUBOUND: AN EFFICIENT WORKFLOW ENABLING PREDICTION OF PERFORMANCE BOUNDS UNDER UNPREDICTABLE QUANTUM NOISE

jinyang li, Weiwen Jiang, George Mason University, Fairfax, VA; Samudra Dasgupta, University of Tennessee, Knoxville, TN; Travis Humble, Oak Ridge National Laboratory, Oak Ridge, TN;

RADAR: A SKEW-RESISTANT AND HOTNESS-AWARE ORDERED INDEX DESIGN FOR PROCESSING-IN-MEMORY SYSTEMS

Yifan Hua, Shengan Zheng, Weihan Kong, Cong Zhou, Kaixin Huang, Ruoyan Ma, Yifeng Hui, Linpeng Huang, Shanghai Jiao Tong University, Shanghai, China

REPRESENTATION-INDEPENDENT RESUBSTITUTION FOR AREA-ORIENTED LOGIC OPTIMIZATION

Andrea Costamagna, Alessandro Tempia Calvino, Siang-Yun Lee, Giovanni De Micheli, École Polytechnique Fédérale de Lausanne, Switzerland; Alan Mishchenko, University of California, Berkeley, CA; Satrajit Chatterjee, Kepler AI, Palo Alto, CA;

RESET DOMAIN CROSSING DESIGN VERIFICATION CLOSURE USING ADVANCED DATA ANALYTICS TECHNIQUES

Reetika Reetika, Sulabh Khare, Siemens, Noida, India

SASDYNABLE: A COMPACT TRANSFORMER INFERENCE ARCHITECTURE WITH SATURATION-APPROXIMATE SOFTMAX ENABLING DYNAMIC-MAPPING BASED LAYER-FUSION EXECUTION

Liu He, Zongle Huang, Yujin Wang, Shupei Fan, Tang Chen, Huazhong Yang, Yongpan Liu, Hongyang Jia, Tsinghua University, Beijing, China

SCALABLE MULTI-TASK DEEP INFERENCE ON RESOURCE CONSTRAINED ENERGY HARVESTING SYSTEM

Sahidul Islam, Chen Pan, Mimi Xie, The University of Texas at San Antonio, San Antonio, TX; Bin Lei, Shanglin Zhou, Caiwen Ding, University of Connecticut, Storrs, CT;

SCALER-FFT: A SCALABLE FPGA-BASED FFT ACCELERATOR VIA GENERAL MATRIX MULTIPLICATION

Song Zhang, Zhiyuan Ma, Zexu Zhang, Yueyin Bai, Kun Wang, Fudan University, Shanghai, China

SFQ COUNTER-BASED PRECOMPUTATION FOR LARGE-SCALE CRYOGENIC VQE MACHINES

Yosuke Ueno, Yutaka Tabuchi, RIKEN, Wako-shi, Japan; Satoshi Imamura, Fujitsu Limited, Kawasaki, Japan; Yuna Tomida, Hiroshi Nakamura, The University of Tokyo, Japan; Teruo Tanimoto, Koji Inoue, Kyushu University, Fukuoka, Japan; Masamitsu Tanaka, Nagoya University, Nagoya, Japan;

SI-AWARE WIRE TIMING PREDICTION AT PRE-ROUTING STAGE WITH MULTI-CORNER CONSIDERATION

Xu He, Yushan Wang, Renjun Zhao, Hunan University, Changsha, China; Yao Wang, Chang Liu, Yang Guo, National University of Defense Technology, Changsha, China

SOCURELLM: AN LLM-DRIVEN APPROACH FOR LARGE-SCALE SYSTEM-ON-CHIP SECURITY VERIFICATION AND POLICY GENERATION

Shams Tarek, Dipayan Saha, Sujan Kumar Saha, Mark Tehranipoor, Farimah Farahmandi, University of Florida, Gainesville, FL

SPHINCSLET - A LIGHTWEIGHT IMPLEMENTATION OF SPHINCS+

Sanjay Deshpande, Jakub Szefer, Yale University, New Haven, CT; Yongseok Lee, Cansu Karakuzu, Yunheung Paek, Seoul National University, Seoul, South Korea

A SYNTHESIS METHODOLOGY FOR INTELLIGENT MEMORY INTERFACES IN ACCELERATOR SYSTEMS

Ankur Limaye, Vito Giovanni Castellana, Andres Marquez, Antonino Tumeo, Pacific Northwest National Laboratory, Richland, WA; Nicolas Bohm Agostini, Northeastern University, Boston, MA; Claudio Barone, Michele Fiorito, Fabrizio Ferrandi, Politecnico di Milano, Italy;

TDM: TIME AND DISTANCE BASED METRIC FOR QUANTIFYING INFORMATION LEAKAGE VULNERABILITIES IN SOCS

Avinash Ayalasomayajula, Hasan Al-Shaikh, Henian Li, Sujan Saha, Farimah Farahmandi, University of Florida, Gainesville, FL

WORK-IN-PROGRESS POSTERS (CONTINUED)

TINYSEG: MEMORY-EFFICIENT IMAGE SEGMENTATION FOR SMALL EMBEDDED SYSTEMS

Byungchul Chae, Jiae Kim, Seonyeong Heo, Kyung Hee University, Yongin, South Korea

TRIFP-DCIM: A TOGGLE-RATE-IMMUNE FLOATING-POINT DIGITAL COMPUTE-IN-MEMORY DESIGN WITH ADAPTIVE-ASYMMETRIC COMPUTE-TREE

Xing Wang, Tianhui Jiao, Yuchen Ma, Zhican Zhang, Zhichao Liu, Xi Chen, Xin Si, Southeast University, Nanjing, China

TRIPARTITE SERVER MUTUAL ATTESTATION: TEE-BASED BFT FOR BOOSTING SERVER RELIABILITY IN FEDERATED LEARNING

Yusen Wu, Phuong Nguyen, Yelena Yesha, University of Miami, FL

UNDERSTANDING THE UPPER BOUNDS OF ENERGY EFFICIENCY IN A COMPUTING-IN-MEMORY PROCESSOR AND HOW TO APPROACH THE LIMIT

Zhaori Cong, Jinshan Yue, Shengzhe Yan, Zhuoyu Dai, Zeyu Guo, Zhihang Qian, Chunmeng Dou, Feng Zhang, Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China; Yifan He, Sun Wenyu, Yongpan Liu, Tsinghua University, Beijing, China

VISIONHD: REVISITING HYPERDIMENSIONAL COMPUTING FOR IMPROVED IMAGE CLASSIFICATION

Fatemeh Asgarinejad, Tajana Rosing, University of California, San Diego, CA; Justin Morris, Baris Aksanli, San Diego State University, San Diego, CA

WHERE AND HOW TO CHARGE: EFFECTIVE CHARGING WITH MOBILE AGENT IN WIRELESS POWERED CPS

Chenchen Fu, Zining Zhou, Sujunjie Sun, Weiwei Wu, Southeast University, Nanjing, China; Song Han, University of Connecticut, Storrs, CT

BIRDS OF A FEATHER

Time: 6:30 PM – 9:30 PM
Session Type: Birds of a Feather
Room: 3001, 3rd Floor

OPEN-SOURCE EDA, DATA AND BENCHMARKING SUMMIT

https://open-source-eda-birds-of-a-feather.github.io/
Contact: Andrew B. Kahng, abk@ucsd.edu

AI AND THE INTELLIGENT EDGE

Time: 8:45 AM – 9:45 AM
Session Type: Keynote
Room: 3007, 3rd Floor

Description: Artificial intelligence is changing the world around us, but most of the focus has been on large models running on immense compute servers. There is a critical need for AI in edge applications to decrease latency and power consumption. Fulfilling this need requires new approaches to meet the constraints of future industrial, automotive, and consumer platforms at the intelligent edge.

Speaker: Alan Lee, Analog Devices, Inc. (ADI)

CHIPLETS – THE NEXT GENERATION CHIP DESIGN TREND BEYOND MOORE'S LAW

Time: 10:15 AM – 11:00 AM
Session Type: Analyst Presentation
Room: DAC Pavilion, Level 2 Exhibit Hall

Description: The next stage of integrated circuit manufacturing is disaggregation or breaking up the design of large chips into smaller units. These smaller units typically represent a unique function. The advantages are shorter design time, lower cost, easier drop-in inclusion of already available designs, increased modularity and scalability, and fewer manufacturing defects. This technique is especially well suited for leveraging the heterogeneous nature of large processors, coprocessors, system on chip (SoC) and integrated memory solutions, but the evolution of this trend is likely to spread throughout IC design.

This presentation is designed to provide a brief introduction to the nature of chiplet design and why it is so important at this time. The technical details will be presented in moderation including teardown examples of current chiplet solutions and which end-systems include them. The presentation will touch on technology advances that need to evolve to facilitate this approach. We will provide a market penetration and a five-year forecast for chiplet-based design strategies. We will provide longer views of the evolution to include such ICs as graphics, AI, and other accelerators, FGPAs, microcontrollers and other processors. We will conclude with why we think this trend is essential to the future of the semiconductor industry and design automation.

Speaker: Tom Hackenberg, Yole Group

GENERATIVE AI FOR SEMICONDUCTOR DESIGN AND VERIFICATION

Time: 10:30 AM – 11:00 AM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: The emergence of generative AI presents tremendous opportunities for advancing technical and business processes for high tech and semiconductor industries. From optimizing complex system design processes and accelerating time-to-market for new products to augmenting human capabilities, improving engineering and manufacturing methodologies and processes with applied generative AI has unlimited potential. Generative design methodologies powered by AI can automatically design chips and electronic subsystem given the right prompts and desired parameters and constraints without intensive engineering efforts and freeing up resources. Or generative Engineering Assistants can help a new engineers become up to 2X more productive by interacting with design tools using natural language. For process improvements that directly impact project timelines and business outcomes, generative AI can facilitate rapid development of product datasheets, technical manuals, and associated documentation customized to target audience and markets. Further efficiency gains can be realized by using engineering assistants for research and providing engineers contextual recommendations, thereby assisting human teams to quickly address critical research problems. We will discuss generative AI services on AWS and how some of these services can be leveraged to build a generative AI Engineering Assistant for semiconductor design.

Speaker: Karan Sing, Amazon

EDGE INTELLIGENCE & GENAI: EXPLORING CHALLENGES AND ETHICS

Time: 10:30 AM – 12:00 PM
Session Type: Engineering Track
Topic Area(s): Embedded Systems
Room: 2012, 2nd Floor

Organizer: Shankar Hemmady, Blue Horizons

Moderator: Shankar Hemmady, Blue Horizons

Description: The convergence of the Internet of Things (IoT), Heterogeneous Computing Architectures, Artificial Intelligence (AI), Machine Learning (ML), and Generative AI (GenAI) is ushering in a new era of computation and analysis. Our panelists will explore a deeper understanding of the intricate interplay between Edge Intelligence and GenAI, with a focus on the technical hurdles and ethical considerations.

By processing data closer to its source, edge computing can harness the power of AI-ML in real-time. This paradigm shift is redefining the capabilities of IoT and computational architectures. Join us as we explore the practical challenges involved in integrating GenAI into edge computing such as limited computational resources, latency reduction, and the development of lightweight AI models.

Edge computing, fortified by GenAI, is changing the game in critical sectors like healthcare, manufacturing, automotive, smart cities, and semiconductor design and manufacturing. Real-time data processing is enhancing decision-making, improving efficiency, and even saving lives. Through case studies and examples, we'll discuss how engineers and researchers are at the forefront of developing solutions that drive these innovations.

While the technical aspects are fascinating, with great power comes great responsibility. The ubiquity of edge computing and GenAI raises crucial ethical questions. How can we ensure data privacy and security at the edge? What safeguards can be put in place to mitigate bias in AI algorithms? Who is accountable when autonomous systems make critical decisions?

Our panel comprises seasoned experts who have grappled with these questions in academic research, policy making, product and infrastructure design and deployment as well as investing and mentoring. We invite you to be a part of the conversation that is shaping the future of technology.

Panelists: Lav Varshney, University of Illinois at Urbana-Champaign; Robert Mains, CHIPS Alliance / Linux Foundation; Eustace Asanghanwa, Microsoft; Michael Boone, NVIDIA

INDUSTRY TRENDS IN THE FRONT END

Time: 10:30 AM – 12:00 PM
Session Type: Engineering Track
Topic Area(s): Front-End Design
Room: 2010, 2nd Floor

Session Chairs: Vikas Sachdeva, Real Intent Inc.

Description: Emergence of AI has fueled an arms race to design new kinds of hardware to run them optimally and that in turn is accelerating innovation in design and verification methodologies. Come and learn the latest industry trends in front-end design, from Co-pilots in design and verification to improving PPA using AI.

- **AI-Powered High-Sigma Automated Full Library Verification Methodology for Standard Cells**
  Chengcheng Liu, NVIDIA, Sunnyvale, CA; Mohamed Atoua, Siemens, San Francisco, CA;
- **The Era of Copilots for Silicon Design and Verification**
  Erik Berg, Microsoft, Portland, OR;
- **Improving Power Efficiency using Workload-aware PPA Analysis for AI Engine**
  Seokjoong Kim, Alex Hao, Reza Sajadiany, Pantelis Sarais, Tim Tuan, AMD, San Francisco, CA;
- **Augmenting IP/SOC Verification Exhaustiveness with BER Transformer infused Deep Learning Model**
  Anil Deshpande, Somasunder Sreenath, Mukesh Barnwal, Rohan R, Swapnil Singh, Samsung Semiconductor, Bengaluru, India;
- **Shift Left Detection and Root Cause Analysis of Synthesis Optimized Registers at RTL Level**
  Sathappan Palaniappan, Broadcom, San Francisco, CA; Kartik Agarwal, Himanshu Kathuria, Jaskaran Ajimal, Amit Jalota, Harsha Somashekar, Synopsys, Mountain View, CA;
- **Design Constraint Strategy For Dealing With Cascaded Clock MUX Structures**
  Anish Keshava, Nitesh S, Satyanarayana Patnala, Sridharr S, Synopsys, Bengaluru, India; Aakarshak Nandwani, Synopsys, Pune, India

ELECTRON SIGNATURES FOR PREDICTING THE DIAGNOSIS!

Time: 10:30 AM – 12:00 PM
Session Type: Engineering Track
Topic Area(s): Back-End Design
Room: 2010, 2nd Floor

Session Chair: Badhri Uppiliappan, Analog Devices, Inc.

Description: Enhance your work to identify the signatures underlying high bandwidth interfaces, chip package board co-design or just closing optical and silicon robustness from leaking secrets to the outside world.

- **UCIe-A 32GT/s power distributed network design-optimization at organic interposer with localized integrated passive decoupling capacitors**
  Sheng-Fan Yang, Global Unichip Corporation
- **Die, Package and PCB Co-design for Low Area, High Signal to Power Pin Ratio in High Frequency SOC designs**
  Shipei Qu, Xiaolin Zhang, Chi Zhang, Dawu Gu, Shanghai Jiao Tong University, Shanghai, China;
- **Si Backside Side-Channel Leakage and Simulation of Cryptographic IC Chips**
  Rikuu HasegawaKazuki MontaTakuya WadatsumiTakuji MikiMakoto NagataLang LinSreeja ChowdhuryAkhilesh KumarNorman Chang
- **System Aware IO Integrity Signoff**
  Anubhav JohriBijaya Dash
- **Pre-Silicon Photon Emission Modeling and Optical Side-Channel Simulation**
  Henian LiLang LinNorman ChangSreeja ChowdhuryKazuki MontaMakoto NagataMark Tehranipoor

LOOK BOTH WAYS BEFORE YOU CROSS

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): Security
Room: 3012, 3rd Floor

Session Chairs: Soheil Salehi (University of Arizona)

Description: Security is critical in every facet of system design. One slight security misstep will leave your system vulnerable to attack. This session addresses cross-layer security weaknesses, vulnerabilities, and mitigations. Attendees will learn how to safely navigate security at the intersection of processor architectures, operating systems, and firmware, ensuring a safe and secure journey to the other side.

- **Trapped by Your WORDs: (Ab)using Processor Exception for Generic Binary Instrumentation on Bare-metal Embedded Devices**
  Shipei Qu, Xiaolin Zhang, Chi Zhang, Dawu Gu, Shanghai Jiao Tong University, Shanghai, China;
- **TATOO: A Flexible Hardware Platform for Binary-Only Fuzzing**
  Jinting Wu, Haodong Zheng, Yu Wang, Tai Yue, Fengwei Zhang, Southern University of Science and Technology, Shenzhen, China;
- **SPECRUN: The Danger of Speculative Runahead Execution in Processors**
  Chaoqun Shen, Jiliang Zhang, Hunan University, Changsha, China;Gang Qu, University of Maryland, College Park, MD;
- **Look Before You Access: Efficient Heap Memory Safety for Embedded Systems on ARMv8-M**
  Jeonghwan Kang, Jaeyeol Park, Donghyun Kwon, Pusan National University, Busan, South Korea; Jiwon Seo, Korea Automotive Technology Institute, Cheonan, South Korea;
- **Effectively Sanitizing Embedded Operating Systems**
  Jianzhong Liu, Yuheng Shen, Yiru Xu, Yu Jiang, Tsinghua University, Beijing, China; Hao Sun, ETH Zurich, Zurich, Switzerland; Heyuan Shi, Central South University, Changsha, China;
- **Laser Shield: a Physical Defense with Polarizer against Laser Attack**
  Qingjie Zhang, Chao Zhang, Han Qiu, Tsinghua University, Beijing, China;Lijun Chi, Mounira Msahli, Gerard Memmi, Telecom Paris, France; Di Wang, Beijing University of Posts and Telecommunications, Beijing, China; Tianwei Zhang, Nanyang Technological University, Singapore

AI PARADIGMS BEYOND DEEP NEURAL NETWORKS

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): AI
Room: 3001, 3rd Floor

Session Chairs: Parivesh Choudhary (Synopsys Inc); Anca Molnos (CEA-LIST)

Description: As hardware performance slows in the post-Moore era, we need to explore new computing paradigms to improve the energy efficiency of AI. This session delves into cutting-edge algorithm research beyond DNNs and its practical applications. The presentations in this session discuss Optical Neural Networks, Random Forests, Hyper-Dimensional Computing, Approximate Nearest Neighbor Search, and Graph Neural Networks.

- **Zeroth-Order Optimization of Optical Neural Networks with Linear Combination Natural Gradient and Calibrated Model**
  Hiroshi Sawada, Kazuo Aoyama, Kohei Ikeda, NTT Corporation, Atsugi, Japan;
- **Order-Preserving Cryptography for the Confidential Inference in Random Forests: FPGA Design and Implementation**
  Rupesh Karn, New York University Abu Dhabi, United Arab Emirates; Kashif Nawaz, Technology Innovation Institute, Abu Dhabi, United Arab Emirates; Ibrahim (Abe) Elfadel, Khalifa University, Abu Dhabi, United Arab Emirates;
- **SMORE: Similarity-Based Hyperdimensional Domain Adaptation for Multi-Sensor Time Series Classification**
  Junyao Wang, Mohammad Al Faruque, University of California, Irvine, CA;
- **Leanor: A Learning-Based Accelerator for Efficient Approximate Nearest Neighbor Search via Reduced Memory Access**
  Yi Wang, Huan Liu, Jianan Yuan, Jiaxian Chen, Tianyu Wang, Chenlin Ma, Rui Mao, Shenzhen University, Shenzhen, China;
- **GNNavigator: Towards Adaptive Training of Graph Neural Networks via Automatic Guideline Exploration**
  Tong Qiao, Jianlei Yang, Yingjie Qi, Ao Zhou, Weisheng Zhao, Chunming Hu, Beihang University, Beijing, China; Chen Bai, Bei Yu, The Chinese University of Hong Kong, Shatin, Hong Kong;
- **Less is More: Hop-Wise Graph Attention for Scalable and Generalizable Learning on Circuits**
  Chenhui Deng, Zichao Yue, Zhiru Zhang, Cornell University, Ithaca, NY; Cunxi Yu, University of Maryland, College Park, MD; Gokce Sarar, Ryan Carey, Rajeev Jain, Qualcomm, San Diego, CA

ANALOG DESIGN VERIFICATION AND LAYOUT SYNTHESIS RETHOUGHT

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): EDA
Room: 3010, 3rd Floor

Session Chairs: Ahmet Budak (Analog Devices Inc.); Weidong Cao (George Washington University)

Description: This session solves core EDA problems for analog circuit design. The first five papers improve verification starting with advanced simulation methods for complex (extracted) circuits: simulations are empowered by a memory-efficient solution for sparse matrices and a powerful graph sparsification algorithm; an efficient capacitance approximation methodology is proposed to enhance parasitic extraction while PCB-S-parameters are modeled by an AI-driven estimator; and a gradient descent approach improves equivalence checking. Finally, an AI approach tackles the analog layout synthesis problem with 3DGNNs.

- **MASC: A Memory-Efficient Adjoint Sensitivity Analysis through Compression Using Novel Spatiotemporal Prediction**
  Chenxi Li, Yongqiang Duan, Yang Li, Weifeng Liu, Zhou Jin, China University of Petroleum, Beijing, China; Boyuan Zhang, Dingwen Tao, Indiana University, Bloomington, IN; Zuochang Ye, Tsinghua University, Beijing, China;
- **inGRASS: Incremental Graph Spectral Sparsification via Low-Resistance-Diameter Decomposition**
  Ali Aghdaei, Zhuo Feng, Stevens Institute of Technology, Hoboken, NJ;
- **Enhancing 3-D Random Walk Capacitance Solver with Analytic Surface Green's Functions of Transition Cubes**
  Jiechen Huang, Wenjian Yu, Tsinghua University, Beijing, China;
- **TraceFormer: S-parameter Prediction Framework for PCB Traces based on Graph Transformer**
  Doyun Kim, Jaemin Park, Youngmin Oh, Bosun Hwang, Samsung Electronics, Suwon, South Korea;
- **Efficient Equivalence Checking of Nonlinear Analog Circuits using Gradient Ascent**
  Kemal Caglar Coskun, Muhammad Hassan, ; Rolf Drechsler, University of Bremen, Germany; Lars Hedrich, Goethe University Frankfurt, Germany
- **Performance-driven Analog Routing via Heterogeneous 3DGNN and Potential Relaxation**
  Peng Xu, Guojin Chen, Keren Zhu, Tinghuan Chen, Tsung-Yi Ho, Bei Yu, The Chinese University of Hong Kong, Hong Kong

MEMORIES HAVE A MIND OF THEIR OWN

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3002, 3rd Floor

Session Chairs: Yannan Nellie Wu (Google); Win-San Vince Khwa (TSMC)

Description: Computing-in-memory (CIM) continues to advance energy efficiency for deep learning with breakthroughs in architecture, circuitry, and devices. The first paper introduces a tri-gear heterogeneous digital CIM for flexible data reuse in Diffusion models. The second paper unveils a fine-grained digital CIM with hessian trace-based quantization and approximate computing. The third paper presents a hybrid-domain SRAM CIM macro, harmonizing accuracy and energy efficiency through digital-analog computing synergy. The next two papers harness RRAM and IGZO in CIM applications. The final paper presents a drop-in-replacement design allowing fine-grained interleaving of processing-in-memory accesses and host accesses.

- **AIG- A Scalable Chiplet Module with Tri-Gear Heterogeneous Compute-in-Memory for Diffusion Acceleration**
  Yiqi Jing, Meng Wu, Jiaqi Zhou, Yiyang Sun, Yufei Ma, Ru Huang, Tianyu Jia, Le Ye, Peking University, Beijing, China;
- **FDCA: Fine-grained Digital-CIM based CNN Accelerator with Hybrid Quantization and Weight-Stationary Dataflow**
  Bo Liu, Qingwen Wei, Yang Zhang, Xingyu Xu, Zihan Zou, Xinxiang Huang, Xin Si, Hao Cai, Southeast University, Nanjing, China;
- **Addition is Most You Need: Efficient Floating-Point SRAM Compute-in-Memory by Harnessing Mantissa Addition**
  Weidong Cao, George Washington University, Washington, DC; Jian Gao, Xuan Zhang, Northeastern University, Boston, MA; Xin Xin, University of Central Florida, Orlando, FL;
- **IG-CRM: Area/Energy-Efficient IGZO-Based Circuits and Architecture Design for Reconfigurable CIM/CAM Applications**
  Zeyu Guo, Jinshan Yue, Shengzhe Yan, Zhuoyu Dai, Xiangqu Fu, Zhaori Cong, Zening Niu, Ke Hu, Lihua Xu, Jiawei Wang, Lingfei Wang, Guanhua Yang, Di Geng, Ling Li, Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China;
- **RWriC: A Dynamic Writing Scheme for Variation Compensation for RRAM-based In-Memory Computing**
  Yucong Huang, Jingyu He, Tim Cheng, Chi Ying Tsui, Hong Kong University of Science and Technology, Hong Kong; Terry Ye, Southern University of Science and Technology, Shenzhen, China;
- **HAIL-DIMM: Host Access Interleaved with Near-Data Processing on DIMM-based Memory System**
  Minkyu Lee, Sang-Seol Lee, Kyungho Kim, Eunchong Lee, Sung-Joon Jang, Korea Electronics Technology Institute, Seongnam-si, South Korea

OPTIMIZING BOTH DIRECTIONS: BETTER AI ALGORITHM FOR SYSTEMS AND BETTER SYSTEMS FOR AI

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): AI
Room: 3008, 3rd Floor

Session Chairs: Lei Yang (George Mason University), Sean Lee (Intel)

Description: While modern high-performance computing systems enable and seamlessly infuse AI/ML into our work and daily lives, AI/ML can also be applied to improve the operational efficiency and robustness in computing reciprocally. Optimization occurs in both directions to continuously elevate the quality of AI services and the performance of systems running AI, creating a positive cycle. This session presents such a category of techniques, including memory optimization for DNN on tiny devices, enhancement for adversarial robustness, an adaptive federated learning scheme, adaptive multi-tensor fusion, optimization for edge ML, and an auto-tuning framework for real-time vision tasks.

- **MoteNN: Memory Optimization via Fine-grained Scheduling for Deep Neural Networks on Tiny Devices**
  Renze Chen, Zijian Ding, Size Zheng, Meng Li, Yun (Eric) Liang, Peking University, Beijing, China;
- **Garrison: A High-Performance GPU-Accelerated Inference System for Adversarial Ensemble Defense**
  Yan Wang, Xingbin Wang, Zechao Lin, Yulan Su, Sisi Zhang, Rui Hou, Dan Meng, Institute of Information Engineering, Chinese Academy of Sciences, Beijing, China;
- **AdaptiveFL: Adaptive Heterogeneous Federated Learning for Resource-Constrained AIoT Systems**
  Chentao Jia, Zekai Chen, Yanxin Yang, East China Normal University, Shanghai, China; Mingsong Chen, East China Normal University, Shanghai, China; Ming Hu, Yang Liu, Nanyang Technological University, Singapore; Xiaofei Xie, Singapore Management Univerisity, Singapore;
- **Enabling Multi-Tensor Fused Dataflow for Transformer Models on Spatial Accelerators**
  Lei Xu, Zhiwen Mo, Qin Wang, Jianfei Jiang, Naifeng Jing, Shanghai Jiao Tong University, Shanghai, China;
- **HiRISE: High-Resolution Image Scaling for Edge ML via In-Sensor Compression and Selective ROI**
  Brendan Reidy, ohammadReza Mohammadi, Ramtin Zand, University of South Carolina, Columbia, SC; Sepehr Tabrizchi, Arman Roohi, University of Nebraska, Lincoln, NE; MShaahin Angizi, New Jersey Institute of Technology, Newark, NJ;
- **Auto-ISP: An Efficient Real-Time Automatic Hyperparameter Optimization Framework for ISP Hardware System**
  Jiaming Liu, Fudan University, Shanghai, China; Zihao Liu, Alibaba Group, Shanghai, China; Xuan Huang, Fudan University, Shanghai, China; Ruoxi Zhu, Fudan University, Shanghai, China; Qi Zheng, Fudan University, Shanghai, China; Zhijian Hao, Fudan University, Shanghai, China; Tao Liu, Lawrence Technological University, Southfield, MI; Jun Tao, Fudan University, Shanghai, China; Yibo Fan, Fudan University, Shanghai, China

QUANTUM REAL PROBLEM SOLVER

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3003, 3rd Floor

Session Chairs: Kanad Basu (The University of Texas);

Description: This session will exemplify application of quantum computers and Ising machines to solve various scientific problems such as geophysical analysis, ground energy estimation of molecules, subset-sum problem, Boolean pattern matching problem and combinatorial optimization problems

- **QuGeo: An End-to-end Quantum Learning Framework for Geoscience --- A Case Study on Full-Waveform Inversion**
  Weiwen Jiang, George Mason University, Fairfax, VA; Youzuo Lin, University of North Carolina, Chapel Hill, NC;
- **Combining Parameterized Pulses and Contextual Subspace for More Practical VQE**
  Zhiding Liang, Yiyu Shi, University of Notre Dame, South Bend, IN; Zhixin Song, Georgia Institute of Technology, Atlanta, GA; Jinglei Cheng, Purdue University, West Lafayette, IN; Hang Ren, University of California, Berkeley, CA; Tianyi Hao, University of Wisconsin, Madison, WI; Rui Yang, Tongyang Li, Peking University, Beijing, China;
- **Design of a Quantum Walk Circuit to Solve the Subset-Sum Problem**
  Giacomo Lancellotti, Simone Perriello, Alessandro Barenghi, Gerardo Pelosi, Politecnico di Milano, Italy;
- **Boolean Matching Reversible Circuits: Algorithm and Complexity**
  Tian-Fu Chen, Jie-Hong Roland Jiang, National Taiwan University, Taipei, Taiwan;
- **A High-Performance Stochastic Simulated Bifurcation Ising Machine**
  Tingting Zhang, Jie Han, University of Alberta, Edmonton, Canada;Hongqiao Zhang, Zhengkun Yu, Siting Liu, Shanghai Tech University, Shanghai, China

WHERE PROCESSING-IN-MEMORY FITS BEST IN THE SYSTEM

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3003, 3rd Floor

Session Chairs: Seokhyeong Kang (Pohang University of Science and Technology (POSTECH)); Giacomo Pedretti (Hewlett Packard Labs)

Description: Processing-in-memory (PIM) greatly improves performance and efficiency, but only when coupled with thorough considerations from the perspective of the entire system. The first two papers suggest solutions to accelerate recommendation models using PIM hardware. The third paper presents a near-data computing method to accelerate Mixture-of-Experts LLM inference, followed by the fourth paper which introduces a framework for efficiently realizing bulk bitwise operations in NVMs. The last two papers discuss SRAM-NVM hybrid designs, each aimed at accelerating transformer models and on-device learning.

- **Towards Redundancy-Free Recommendation Model Training via Reusable-aware Near-Memory Processing**
  Haifeng Liu, Long Zheng, Yu Huang, Haoyan Huang, Xiaofei Liao, Jin Hai, Huazhong University of Science and Technology, Wuhan, China;
- **UpDLRM: Accelerating Personalized Recommendation using Real-World PIM Architecture**
  Sitian Chen, Amelie Chi Zhou, Hong Kong Baptist University, Hong Kong, Hong Kong; Haobin Tan, Shenzhen University, Shenzhen, China; Yusen Li, Nankai University, Tianjin, China; Pavan Balaji, Meta, San Francisco, CA;
- **MoNDE: Mixture of Near-Data Experts for Large-Scale Sparse Models**
  Taehyun Kim, Kwanseok Choi, Youngmock Cho, Jaehoon Cho, Hyuk-Jae Lee, Jaewoong Sim, Seoul National University, Seoul, South Korea;
- **SHERLOCK: Scheduling Efficient and Reliable Bulk Bitwise Operations in NVMs**
  Hamid Farzaneh, Joao Paulo De Lima, Asif Ali Khan, Jeronimo Castrillon, Technische Universitat Dresden, Germany; Ali Nezhadi Khelejani, Mahta Mayahinia, Mehdi Tahoori, Karlsruhe Institute of Technology, Karlsruhe, Germany;
- **HEIRS: Hybrid Three-Dimension RRAM- and SRAM-CIM Architecture for Multi-task Transformer Acceleration**
  Liukai Xu, Shuai Yuan, Dengfeng Wang, Yanan Sun, Shanghai Jiao Tong University, Shanghai, China; Yiming Chen, Xueqing Li, Tsinghua University, Beijing, China;
- **Efficient Memory Integration: MRAM-SRAM Hybrid Accelerator for Sparse On-Device Learning**
  Fan Zhang, Deliang Fan, Johns Hopkins University, Baltimore, MD; Amitesh Sridharan, Arizona State University, Tempe, AZ; Wilman Tsai, Shan Wang, Stanford University, Stanford, CA; Yiran Chen, Duke University, Durham, NC

WHY IS EDA PLAYING CATCHUP TO DISRUPTIVE TECHNOLOGIES LIKE AI? WHAT CAN WE DO TO CHANGE THIS?

Time: 10:30 AM – 12:00 PM
Session Type: Research Panel
Topic Area(s): EDA
Room: 3014, 3rd Floor

Organizers: Sandeep Srinivasan, VerifAI, Palo Alto, CA

Moderator: Brian Bailey, SemiEngineering.com, Beaverton, OR

Description: The panel will candidly discuss if and why EDA misses disruptive innovation and chooses incremental advancements.

The EDA industry claims to have the maximum number of PhDs. Still, the last disruptive innovation from EDA was Logic Synthesis, P&R, Logic Simulation, and Formal Methods, invented decades ago.

This panel will attempt to answer the elements required to create bold disruptions. Does the EDA industry need a collective goal, like in other sectors? Does the EDA business duopoly hinder startup innovation?

The discussion will cover the following topics:

1. Current State of EDA and AI

   The panel will be discussing the current state of AI . They will cover topics such as LLMs, RAG, and RL, and the next steps for these technologies.

2. Efficiency versus Discovery and Innovation

   The panel will discuss the tension between efficiency, discovery, and innovation in the EDA and Semi industry. They will discuss how to balance these competing goals and how to create an environment that encourages both.

3. Closed-Form Solution Mindset

   The panel will discuss the challenge of getting beyond the “closed-form solution” mindset. They will explore how this mindset can limit the potential of the EDA industry and how to break free from it.

4. Impact of AI on Workforce

   Will AI change the nature of work in the EDA and Semiconductor industries? If so, how can we prepare the workforce for these changes?

5. Fostering Disruptive Innovation

   Finally, the panel will discuss how to foster disruptive innovation in the EDA and Semi industry. They will explore the necessary factors for disruptive innovation to occur and how to create an environment that encourages it.

Presenters: Prith Banerjee, Ansys, Palo Alto, CA; Jan Rabaey, University of California, Berkeley, CA; Samir Mittal, Micron, Palo Alto, CA; James Scapa, Altair, Atherton, CA; Charles Alpert, Cadence Design Systems, Inc., San Jose, CA

REVOLUTIONIZING EDGE AUTONOMY WITH COGNITIVE MULTISPECTRAL SENSING

Time: 10:30 AM – 12:00 PM
Session Type: Special Session (Research)
Topic Area(s): Design
Room: 3006, 3rd Floor

Organizer: Sara Garcia Sanchez, IBM Research, Yorktown Heights, NY

Session Chair: Roman Caudillo, Semiconductor Research Corporation

Description: This special session presents the overview of ongoing research in SRC/DARPA-funded JUMP2.0 center "CogniSense." The safe and efficient operation of autonomous systems relies on clear, unobstructed perception. Traditional sensing methods, particularly those using high-dimensional sensors like LiDAR and RADR, generate vast amounts of data, leading to what is known as an "analog data deluge." This results in excessive data transmission and computational demands, affecting the decision-making capabilities at the edge such as in Internet-of-Things and Internet-of-Bodies. We discuss a novel Cognitive Multispectral Sensing paradigm to address this key challenge. Cognitive Sensing involves dynamic adjustments in sensing mode (such as sensing spectrum from RADAR, LiDAR to Visual), precision (such as signal-to-noise ratio, downstream processing quantization), and focus (such as through multispectral beamforming) to minimize resource usage while maintaining high predictive accuracy. This new sensing paradigm represents a generalization of attention mechanisms, emulating how different parts of input data are weighted and selectively processed to extract relevant information and ensure that less important inputs are ignored. Early efforts in this direction include recurrent attention models that extract only portions of the input domain, similar to human visual attention. Recent advancements have expanded this concept, introducing novel approaches like reinforcement learning-based sensing policy, adaptive masking, and precision-adjusted sensing.

Key aspects of this special session, moderated by SRC with a mix of industry and academic perspectives, include:

- Developing new sensing frameworks that allow dynamic adjustment of sensing mode, spectrum, and focus.
- Creating machine learning algorithms for dynamic resource allocation in sensing, optimizing resource usage while ensuring high accuracy.
- Discussing applications in platforms such as Internet-of-Bodies for seamless human-machine cooperation and real-time AI.

The session aims to consolidate this emerging trend, bridging the gap between sensing and information processing in a context-adaptive and dynamic framework.

- **Overview of Cognitive Multispectral Sensing**
  Saibal Mukhopadhyay, Georgia Institute of Technology, Atlanta, GA
- **Enabling AI-based Sensing with 5G Networks at the Edge**
  Sara Garcia Sanchez, IBM Research, Yorktown Heights, NY
- **Lightweight Uncertainty Quantification at the Edge: Know When Your AI Model Doesn't**
  Amit Ranjan Trivedi, University of Illinois, Chicago, IL
- **Internet of Bodies for Seamless Human-Machine Co-operation and Real-time AI**
  Shreyas Sen, Purdue University, West Lafayette, IN

OBJECT ORIENTED EMBEDDED HARDWARE FOR OPERATIONAL EXCELLENCE

Time: 11:15 AM – 11:45 AM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Object-oriented software has made its mark in the industry. It has helped create large software systems. Coming from Software-industry it has been adopted by hardware verification in the form of languages like SystemVerilog and SystemC and methodologies like UVM. But what about embedded hardware?

This presentation will discuss how embedded hardware can be presented in an object-oriented way to firmware and lower levels of system software. We will review the industry standards and non-standard formats that are currently prevalent in this space.

The benefits of this approach will be presented and finally we will discuss the roadmap to get to this level of operational excellence.

Speakers: Anupam Bakshi, Freddy Nunez, Neena Chandrawale, Agnisys Inc.

FROM DESIGN TO DEFENSE: SHAPING THE FUTURE OF MICROELECTRONICS SECURITY

Time: 11:15am – 12:00pm
Session Type: DAC Pavilion Panel
Topic: Security
Room: DAC Pavilion, Level 2 Exhibit Hall

Description: The semiconductor attack surface is increasingly susceptible to threats and malicious inclusion. New attack vectors are emerging, most recently through directed software attacks that exploit hardware vulnerabilities.

Efforts to create a more secure and resilient semiconductor supply chain – the backbone of critical infrastructure – are gaining traction in the US and the EU. Private industry and public agencies recognize that a rigorous and tightly coupled security design sign-off is essential to achieve that goal.

The integration of microelectronic security into the semiconductor life cycle is uncharted territory for conventional semiconductor design flows. Solutions range from incremental improvements of existing verification processes to disruptive new design methodologies aimed at cyber-hardening and embedding resilience against attacks into the components' DNA.

Our panel will discuss strategies and trade-offs in advancing trusted and cyber-resilient microelectronics from cradle to grave. The panel will highlight the vital role of collaboration within the semiconductor and EDA industries as well as with security researchers. We are delighted to have the leading voices in the semiconductor industry join us to discuss the crucial challenges facing cybersecurity in microelectronics designs.

Moderator: Nitin Dahad, embedded.com

Panelists: Cayley Rice, Leidos; Margaret Schmitt, Amida Technology Solutions; Mark Tehranipoor, University of Florida; Simha Sethumadhavan, Columbia University/Chip Scan Inc.

HOW AI IS CHANGING EVERY ASPECT OF EDA, STARTING FROM TRANSISTOR-LEVEL SIMULATION

Time: 12:00 PM – 12:30 PM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: There is a lot of hype in the industry around AI, but behind the hype there is the reality. That reality is that AI really is impacting virtually every aspect of semiconductor design. However, its not as simple as taking general purpose AI solutions and hoping they work for EDA, the risks are too high and when dealing with parts per billion (or trillion) in acceptable errors, hallucinations are not acceptable. What is needed are Verifiable AI solutions that deliver results that users can trust and that reduce the overall resources needed to complete a task. At Siemens EDA we have been able to leverage Verifiable AI to accelerate virtually every aspect of the design and verification process.

In this presentation we will explore the requirements for, and state of the art of, AI in EDA application. We will explore AI's impact on every aspect of d

Speakers: Jeff Dyck, Siemens

AI ACCELERATION ROADMAP: CO-DESIGNING ALGORITHMS, HARDWARE, AND SOFTWARE

Time: 1:00pm – 1:45pm
Session Type: SKYTalk
Topic: AI
Room: DAC Pavilion, Level 2 Exhibit Hall

Description: Deep Neural Networks (DNNs) have become state-of-the-art in a variety of machine learning tasks spanning domains across vision, speech, and machine translation. Deep Learning (DL) achieves high accuracy in these tasks at the expense of 100s of ExaOps of computation. Hardware specialization and acceleration is a key enabler to improve operational efficiency of DNNs, in turn requiring synergistic cross-layer design across algorithms, hardware, and software.

In this talk I will present this holistic approach adopted in the design of a multi-TOPs AI hardware accelerator. Key advances in the AI algorithm/application-level exploiting approximate computing techniques enable deriving low-precision DNNs models that maintain the same level of accuracy. Hardware performance-aware design space exploration is critical during compilation to map DNNs with diverse computational characteristics systematically and optimally while preserving familiar programming and user interfaces. The opportunities to co-optimize the algorithms, hardware, and the software provides the roadmap to continue to deliver superior performance over the next decade

Presenters: Viji Srinivasan, IBM Thomas J. Watson Research Center

DESIGN AUTOMATION ADVANCEMENT IN THE ANALOG DOMAIN

Time: 1:30 PM – 3:00 PM
Session Type: Engineering Track
Topic Area(s): Back-End Design
Room: 2008, 2nd Floor

Organizers: Sabya Das, Synopsys, Sunnyvale, CA

Moderator: Badhri Uppiliappan, BAE Systems, Boston, MA

Description: Today's high-performance and low-power, state-of-the-art designs are getting more complex with a significant presence of Analog and Mixed-Signal blocks. As a result, continuous innovation in the Analog Design Automation space is becoming crucial. This session focuses on various aspects of that domain. The first talk is about the power/signal/thermal/reliability integrity challenges for three emerging 3D Heterogeneous designs. The second talk describes the recent developments in an open-source analog layout automation flow that has been applied to various design types and technology nodes. The third presentation will attempt to predict if and when analog chip design can become wholly autonomous. Final speaker will review Siemens EDA's latest production-proven methods for transistor-level verification that are used to create consistently accurate AI-derived answers for measuring chip variability and for generating timing models.

Presenters: Norman Chang, Ansys, San Jose, CA; Sachin S. Sapatnekar, University of Minnesota, Minneapolis, MN; Vuk Borich, Synopsys, San Jose, CA; Jeff Dyck, Siemens, Saskatoon, Canada

ADVANCES IN MIXED SIGNAL IP DESIGN

Time: 1:30 PM – 3:00 PM
Session Type: Engineering Tracks
Topic Area(s): IP
Room: 2012, 2nd Floor

Session Chair: Vidyasagar Ganesan, AMD

Description: Design automation has been the holy grail of mixed signal analog design. Unlike digital P&R design, mixed signal design has many challenges to overcome for automation and efciency. In this section we present a collection of papers that improve simulation, test, and validation using AI/ML techniques.

- **Bringing Digital IP Development into the 21st Century**
  Warren Savage, Rocksavage Technology, Inc., San Jose, CA; Prahlad Menon, Fraunhofer USA, Plymouth, MI;
- **CDC Multimode Signoff Methodology**
  Navneet Chaurasia, Amit Goldie, Sanjeev Chaudhri, Synopsys, Noida, India; Deepak Ahuja, Synopsys, New Delhi, India; Paras Mal Jain, Synopsys, San Francisco, CA;
- **Droop! There it is!**
  Michael Durr, Movellus, San Jose, CA;
- **Accelerating Timing Closure for Network on Chips (NoCs) using Physical Awareness**
  Andy Nightingale, Arteris, Cambridge, United Kingdom; Guillaume Boillet, Arteris, Cupertino, CA;
- **Samsung's IP QA methodology using Solido Crosscheck**
  Peter Park, Samsung, Seoul, South Korea; Siddharth Ravikumar, Siemens, Walnut Creek, CA

EMBEDDED SYSTEMS AND SOFTWARE

Time: 1:30pm – 3:00pm
Session Type: Embedded Systems and Software
Topic: Embedded Systems and Software
Room: 2012, 2nd Floor

Session Chair: Natraj Ekambaram, NXP Semiconductors

Description: Embedded Software is a critical differentiator in today's designs, and its close relationship with hardware aspects specifcally impacts hardware/software flows and development methodologies. This session will discuss aspects like accuracy enhancements for virtualization to enable early software development, system design aspects of power, frmware verifcation, reinforcement learning for test optimization, automotive AUTOSAR software aspects, and mapping challenges of software to computing resources.

- **No-Code Power and Clock System Design**
  WHoyeon Jeon, Ahchan Kim, Ingyu Kim, ITDA Semiconductor Co., Ltd., Hwasung-si, South Korea; Jongbae Lee, BOS Semiconductor Co., Ltd., Seoul, South Korea;
- **Functional Accuracy Enhancement of In-House Virtual Platform using Commercial IP Model**
  Jooho Wang, Dongyoung Lee, Myeongjin Kim, Sangwoo Han, Seungik Ha, Jinbeom Kim, Jaeyeong Jeon, Songyi Park, Jongseong Park, Kyungsu Kang, Jaewoo Im, Samsung Electronics, Seoul, South Korea;
- **Complex Application Mapping to Heterogeneous Compute Resources**
  Wesley Skefngton, AMD, Schenectady, NY; Surya Chongala, AMD, Gurgaon, India; Deepak Shankar, Mirabilis Design Inc., Chennai, India; • Automated Generation of SSD Stress Tests Using Ofine Reinforcement Learning Sunghee Lee, Samsung Electronics, Seoul, South Korea;
- **Development of SystemC-based Security VP for In-House SED SSD Firmware Verifcation and Application of libFuzzer**
  Changwon Kim, Samsung Electronics, Seoul, South Korea;
- **Open Source AUTOSAR Classic Platform**
  Moisés Urbina Fuentes, ALTEN Group, Cologne, Germany

CHALLENGING THE AUTONOMY CHALLENGES

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): Autonomous Systems
Room: 3001, 3rd Floor

Session Chairs: Hokeun Kim (Arizona State University), Qi Zhu (Northwestern University)

Description: This session brings together novel methods aimed at fortifying the resilience of autonomous vehicles against multifaceted vulnerabilities, encompassing both systemic faults and deliberate adversarial threats. The papers in this session address critical challenges such as safeguarding against corrupted sensor values and mitigating the detrimental effects of video hazing on perception systems. Additionally, novel approaches to counteract malicious perception poisoning attacks and Byzantine faults are explored, emphasizing the importance of ensuring the integrity and reliability of autonomous vehicle operations in the face of sophisticated adversarial tactics.

- **MaxiMals: A Low-cost and Effective Technique for Corrupted Values Correction in Vision Transformers**
  Lucas Roquet, Angeliki Kritikakou, Universite de Rennes, France; Fernando Fernandes dos Santos, Marcello Traiola, Olivier Sentieys, INRIA, Rennes, France; Paolo Rech, University of Trento, Italy;
- **Conclave - Secure and Robust Cooperative Perception for Connected Autonomous Vehicle Using Authenticated Consensus and Trust Scoring**
  Edward Andert, Francis Mendoza, Hans Behrens, Aviral Shrivastava, Arizona State University, Phoenix, AZ;
- **Ev-Edge: Efficient Execution of Event-based Vision Algorithms on Commodity Edge Platforms**
  Shrihari Sridharan, Surya Selvam, Kaushik Roy, Anand Raghunathan, Purdue University, West Lafayette, IN;
- **SPFuzz: Stateful Path based Parallel Fuzzing for Protocols in Autonomous Vehicles**
  Junze Yu, Zhengxiong Luo, Yanyang Zhao, Yu Jiang, Tsinghua University, Beijing, China; Fangshangyuan Xia, Heyuan Shi, Central South University, Changsha, China;
- **Fake Node-Based Perception Poisoning Attacks against Federated Object Detection Learning in Mobile Computing Networks**
  Xiong Xiao, Mingxing Duan, Yingjie Song, Zhuo Tang, Hunan University, Changsha, China; Wenjing Yang, National University of Defense Technology, Changsha, China;
- **A HW/SW Co-Design of Video Dehazing Accelerator Using Decoupled Local Atmospheric Light Prior**
  Yanjie Tan, Yifu Zhu, Zhaoyang Huang, Feiteng Nie, Huailiang Tan, Hunan University, ChangSha, China

DO-MORE-WITH-LESS: OPTIMIZING AI MODELS FOR INFERENCE EFFICIENCIES

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): AI
Room: 3003, 3rd Floor

Session Chair: Amin Firoozshahian (Meta Platforms Inc.), Thierry Tambe (Stanford University)

Description: With AI models' continued growth, inference efficiencies have become more important than ever. This session presents six papers on model optimization techniques for improving inference efficiency. The first three papers aim at optimizing the model network topology with path selection, residual optimization, and graph substitution/parallelization. The next two papers present improvements in quantization with variable-length quantization and for point-cloud networks. The sixth paper presents a novel attention mechanism for transformer models.

- **PIVOT- Input-aware Path Selection for Energy-efficient ViT Inference**
  Abhishek Moitra, Abhiroop Bhattacharjee, Priyadarshini Panda, Yale University, New Haven, CT;
- **Deep Reorganization: Retaining Residuals in TinyML**
  Hashan Mendis, Chih-Kai Kang, Pi-Cheng Hsiu, Academia Sinica, Taipei, Taiwan; Chun-Han Lin, Ming-Syan Chen, National Taiwan University, Taipei, Taiwan;
- **GSPO: A Graph Substitution and Parallelization Joint Optimization Framework for DNN Inference**
  Zheng Xu, Shaojun Wei, Yang Hu, Shouyi Yin, Tsinghua University, Beijing, China;Xu Dai, Shanghai Artificial Intelligence Laboratory, Shanghai, China;
- **On the Design of Novel Attention Mechanism for Enhanced Efficiency of Transformers**
  Sumit Jha, Florida International University, Miami, FL; Susmit Jha, SRI International, Menlo Park, CA; Rickard Ewetz, Alvaro Velasquez, University of Central Florida, Rome, FL;
- **INSPIRE: Accelerating Deep Neural Networks via Hardware-friendly Index-Pair Encoding**
  Fangxin Liu, Ning Yang, Zongwu Wang, Haomin Li, Shiyuan Huang, Zhuoran Song, Li Jiang, Shanghai Jiao Tong University, Shanghai, China; Zhiyan Song, Songwen Pei, University of Shanghai for Science and Technology, Shanghai, China;
- **MoC: A Morton-Code-Based Fine-Grained Quantization for Accelerating Point Cloud Neural Networks**
  Xueyuan Liu, Zhuoran Song, Hao Chen, Xing Li, Xiaoyao Liang, Shanghai Jiao Tong University, Shanghai, China

FIX QUANTUM ERRORS TO WIN BQSKITS

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3002, 3rd Floor

Session Chair: Samah Saeed (CUNY City College), Fan Chen (Indiana University)

Description: Practical quantum computers suffer from varieties of noise regardless of qubit technologies. This session will cover approaches to resolve this issue namely, quantum error mitigation, quantum error correction, robust state preparation for multi-dimensional qudit states and accelerated simulation of stabilizer circuit.

- **SpREM: Exploiting Hamming Sparsity for Fast Quantum Readout Error Mitigation**
  Hanyu Zhang, Liqiang Lu, Siwei Tan, Jia Yu, Jianwei Yin, Zhejiang University, Hangzhou, China;Size Zheng, Peking University, Beijing, China;
- **HiLight: A Comprehensive Framework For High Performance And Light-Weight Scalability In Surface Code Communication**
  Sunghye Park, Dohun Kim, Seokhyeong Kang, Pohang University of Science and Technology (POSTECH), Pohang-si, South Korea;
- **SymPhase: Phase Symbolization for Fast Simulation of Stabilizer Circuits**
  Wang Fang, Mingsheng Ying, Institute of Software, Chinese Academy of Sciences, Beijing, China;
- **Mixed-Dimensional Qudit State Preparation Using Edge-Weighted Decision Diagrams**
  Kevin Mato, Robert Wille, Technical University Munich, Germany; Stefan Hillmich, Software Center Hagenberg (SCCH) GmbH, Hagenberg, Austria;
- **Effective Quantum Resource Optimization via Circuit Resizing in BQSKit**
  Siyuan Niu, Costin Iancu, Wibe de Jong, Ed Younis, Lawrence Berkeley National Lab, Berkeley, CA; Akel Hashim, University of California, Berkeley, CA;
- **FCM: Wire Cutting For Fusion Reduction in Measurement-based Quantum Computing**
  Zewei Mo, Yingheng Li, Aditya Pawar, Xulong Tang, Jun Yang, Youtao Zhang, University of Pittsburgh, PA

POWERING THE FUTURE: FROM MODELING, SIMULATION TO PREDICTION

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): EDA
Room: 3010, 3rd Floor

Session Chairs: Zhou Jin (China University of Petroleum); Umamaheswara Rao Tida (North Dakota State University)

Description: With semiconductor scaling continuing, the efficiency of power prediction, simulation, and modeling becomes crucial. This session brings to light the synergy between neural networks in power prediction and cutting-edge simulations for power grid analysis, alongside specialized modeling for glitch and flip-flop optimization. From PowPrediCT's circuit-aware predictions to MAUnet's IR drop insights, and from PowerRChol's simulation advancements to innovative glitch and flip-flop modeling, this session explores the integral technologies setting new benchmarks for power efficiency in the ever-evolving semiconductor landscape.

- **Advanced gate-level glitch modeling using ANNs**
  Anastasis Vagenas, Dimitrios Garyfallou, Nestor Evmorfopoulos, George Stamoulis, University of Thessaly, Volos, Greece;
- **Binding Multi-bit Flip-flop Cells through Design and Technology Co-optimization**
  Jooyeon Jeong, Taewhan Kim, Seoul National University, Seoul, South Korea;
- **MAUnet: Multiscale Attention U-Net for Effective IR Drop Prediction**
  Mingyue Wang, Yuanqing Cheng, Yage Lin, Kelin Peng, Shunchuan Yang, Beihang University, Beijing, China; Zhou Jin, China University of Petroleum-Beijing, Beijing, China; Wei Xing, Eastern Institute of Technology, Ningbo, China;
- **PowerRChol: Efficient Power Grid Analysis Based on Fast Randomized Cholesky Factorization**
  Zhiqiang Liu, Wenjian Yu, Tsinghua University, Beijing, China;
- **PowPrediCT: Cross-Stage Power Prediction with Circuit-Transformation-Aware Learning**
  Yufan Du, Zizheng Guo, Xun Jiang, Yuxiang Zhao, Yibo Lin, Runsheng Wang, Ru Huang, Peking University, Beijing, China; Zhuomin Chai, Wuhan University, Wuhan, China;
- **Nona: Accurate Power Prediction Model Using Neural Networks**
  HoSun Choi, Chanho Park, Euijun Kim, William Song, Yonsei University, Seoul, South Korea

* Denotes a Best Paper Candidate

PREDICT AND OPTIMIZE: FROM YIELD ESTIMATION TO NATURAL LANGUAGE LAYOUT CUSTOMIZATION

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3008, 3rd Floor

Session Chairs: Takashi Soto (Kyoto University); Ing-Chao Lin (National Cheng Kung University)

Description: This session highlights advancements in layout optimization, TCAD, accurate yield estimation, and soft error estimation techniques, together shaping the future of semiconductor design and reliability. The session explores topics like natural language assisted layout customization, TCAD simulation enhancement via advanced physics-informed neural networks, efficient Bayesian models for yield optimization, rare circuit failure analysis using normalizing flow, novel machine learning approaches to SEM defect segmentation, and how soft error impact estimation is handled in edge AI SoCs, with insights into measured vs., simulated data.

- **ChatPattern: Layout Pattern Customization via Natural Language**
  Zixiao Wang, Xufeng Yao, Wenqian Zhao, Farzan Farnia, Bei Yu, The Chinese University of Hong Kong, Hong Kong;Yunheng Shen, Tsinghua University, Beijing, China; Yang Bai, City University of Hong Kong, Hong Kong;
- **Multi-order Differential Neural Network for TCAD Simulation of the Semiconductor Devices**
  Zifei Cai, AnAoxue Huang, Yifeng Xiong, Dejiang Mu, Xiangshui Miao, Xingsheng Wang, Huazhong University of Science and Technology, Wuhan, China;
- **BNN-YEO: An Efficient Bayesian Neural Network for Yield Estimation and Optimization**
  Zhenxing Dou, ; Peng Wang, Beihang University, Beijing, China; Ming Cheng, University of Bologna, Italy; Ming Jia, XC Micro Technologies, Nanjing, China
- **NOFIS: Normalizing Flow for Rare Circuit Failure Analysis**
  Zhengqi Gao, Luca Daniel, Duane Boning, Massachusetts Institute of Technology, Cambridge, MA;Dinghuai Zhang, Mila - Quebec AI Institute, Universite de Montreal, Montreal, Canada
- **How Accurately Can Soft Error Impact Be Estimated in Black-box/White-box Cases? — A Case Study with an Edge AI SoC —**
  Quan Cheng, Masanori Hashimoto, Kyoto University, Kyoto, Japan; Qiufeng Li, Longyang Lin, Southern University of Science and Technology, Shenzehn, China; Wang Liao, Kochi University of Technology, Kochi, Japan; Liuyao Dai, University of California, Merced, CA; Hao Yu, Southern University of Science and Technology, Shenzhen, China;
- **Minimizing Labeling, Maximizing Performance: A Novel Approach to Nanoscale Scanning Electron Microscope (SEM) Defect Segmentation**
  Yibo Qiao, Weiping Xie, Shunyuan Lou, Qian Jin, Yining Chen, Qi Sun, Cheng Zhuo, Zhejiang University, Hangzhou, China; Lichao Zeng, University of Science and Technology of China, Hefei, China

UNVEILING PRECISION: MASTERING THE ART OF MASK MANUFACTURING AND HOTSPOT DETECTION

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3004, 3rd Floor

Session Chairs: Shao-Yun Fang (National Taiwan University of Science and Technology), Biying Xu (The Hong Kong University of Science and Technology)

Description: Join us at the forefront of semiconductor manufacturing. Delve into how language modeling techniques can be used for hotspot detection in chip layouts via semantic encoding. Discover strategies for co-optimizing source and masks in an efficient manner. Learn about the integration of correlation-aware strategies and reinforcement learning to enhance mask optimization. Explore advancements in inverse lithography technology (ILT) that account for mask writing realities, and appreciate elegant methods for accelerating ILT computations, promising reductions in turnaround time without sacrificing pattern fidelity. This session is a deep dive into the latest methodologies and technologies in photomask design, optimization, and manufacturing.

- **Efficient Bilevel Source Mask Optimization**
  Guojin Chen, Peng Xu, Bei Yu, The Chinese University of Hong Kong, Shatin, Hong Kong; Hongquan He, Hao Geng, Shanghai Tech University, Shanghai, China;
- **Efficient ILT via Multigrid-Schwartz Method**
  Shuyuan Sun, Fan Yang, Li Shang, Dian Zhou, Xuan Zeng, Fudan University,Shanghai, China; Bei Yu, The Chinese University of Hong Kong, Shatin, Hong Kong;
- **LLM-HD: Layout Language Model for Hotspot Detection with GDS Semantic Encoding**
  Yuyang Chen, Yiwen Wu, Jingya Wang, Tao Wu, Xumin He, Jingyi Yu, Hao Geng, Shanghai Tech University, Shanghai, China;
- **CAMO: Correlation-Aware Mask Optimization with Modulated Reinforcement Learning**
  Xiaoxiao Liang, Yuzhe Ma, The Hong Kong University of Science and Technology, Guangzhou, Hong Kong; Haoyu Yang, NVIDIA, Austin, TX; Kang Liu, Huazhong University of Science and Technology, Wuhan, China; Bei Yu, The Chinese University of Hong Kong, Shatin, Hong Kong;
- **EMOGen: Enhancing Mask Optimization via Pattern Generation**
  Su Zheng, Bei Yu, Martin Wong, The Chinese University of Hong Kong, Hong Kong; Yuzhe Ma, The Hong Kong University of Science and Technology, Guangzhou, Hong Kong;
- **Fracturing-aware Curvilinear ILT via Circular E-beam Mask Writer**
  Xinyun Zhang, Su Zheng, Guojin Chen, Binwu Zhu, Bei Yu, The Chinese University of Hong Kong, Shatin, Hong Kong; Hong Xu, City University of Hong Kong, Shatin, Hong Kong

WHAT'S YOUR BEST SIDE?

Time: 1:30 PM – 3:00 PM
Session Type: Research Manuscript
Topic Area(s): Security
Room: 3012, 3rd Floor

Session Chair: Avani Dave (Intel), Vincent Immler (Oregon State University)

Description: Side-channel leakage has been the scourge of cryptographers for decades and yet its impacts to confidentiality of real-world systems and microarchitectural design are still being unearthed. This session consists of presentations that capitalize on execution timing, power consumption, and even temperature leakages to infer secrets from machine learning architectures, trusted execution environments, and CPUs from top vendors! Several presentations also stress the importance of proper software, hardware, and software-hardware co-design to students and practitioners.

- **Conjuring: Leaking Control Flow via Speculative Fetch Attacks**
  Ali Hajiabadi, Trevor E. Carlson, National University of Singapore, Singapore;
- **Whisper: Timing the Transient Execution to Leak Secrets and Break KASLR**
  Yu Jin, Chunlu Wang, Yihao Yang, Xiaoyong Li, Beijing University of Posts and Telecommunications, Beijing, China; Pengfei Qiu, Chang Liu, Hongpei Zheng, Yongqiang Lyu, Dongsheng Wang, Tsinghua University, Beijing, China; Gang Qu, Univ. of Maryland, College Park, MD;
- **ThermalScope: A Practical Interrupt Side Channel Attack Based on Thermal Event Interrupts**
  Xin Zhang, Qingni Shen, Zhuoxi Yang, Zhonghai Wu, Peking University, Beijing, China; Zhi Zhang, University of Western Australia, Sydney, Australia; Wenhao Wang, Institute of Information Engineering, Chinese Academy of Sciences, Beijing, China; Yansong Gao, Data61, CSIRO, Sydney, Australia;
- **Architectural Whispers: Robust Machine Learning Models Fingerprinting via Frequency Throttling Side-Channels**
  Najmeh Nazari, Chongzhou Fang, Hosein Mohammadi Makrani, Setareh Rafatirad, Avesta Sasan, Houman Homayoun, University of California, Davis, CA; Behnam Omidi, Khaled N. Khasawneh, George Mason University, Fairfax, VA; Mahdi Eslamimehr, University of California, Los Angeles, CA; Hossein Sayadi, California State University, Long Beach, CA;
- **SecPaging: Secure Enclave Paging with Hardware-Enforced Protection against Controlled-Channel Attacks**
  Yunkai Bai, Peinan Li, Yubiao Huang, Shiwen Wang, Xingbin Wang, Dan Meng, Rui Hou, Institute of Information Engineering, Chinese Academy of Sciences, Beijing, China;
- **Levioso: Efficient Compiler-Informed Secure Speculation**
  Ali Hajiabadi, Andreas Diavastos, Trevor E. Carlson, National University of Singapore, Singapore; Archit Agarwal, University of California, San Diego, CA

POWER YOUR FUTURE: INVESTMENTS FOR THE CHIP DESIGN WORKFORCE AND RESEARCH

Time: 1:30 PM – 3:00 PM
Session Type: Research Panel
Topic Area(s): Design
Room: 3014, 3rd Floor

Organizers: Angela Hwang, Patrick Haspel, Synopsys, Sunnyvale, CA

Moderator: Marilyn Wolf, University of Nebraska, Lincoln, NE

Description: Deloitte predicts that the semiconductor industry will face a significant gap in workforce, with over 1 million additional jobs needed by 2030. Workforce development is critical, especially chip design talent (including logic and circuits, design verification, testing and CAD, and embedded software), an area that is typically overlooked but is a keystone in the semiconductor supply chain and is essential for technological advancement. The growing demand for design engineers is fueled by industry's emphasis on custom silicon and the realization that any advancement in software is enabled by hardware. This panel will address workforce development success, barriers, critical research areas, and government funding opportunities for cross sector collaborations to ensure a resilient chip design workforce with a focus on the following:

- Fundamental Research: Unprecedented demand and development of semiconductors demonstrates an opportunity to drive system-level performance improvements in computing. What are some strategies to cultivate research capabilities to address the next grand challenges in chip design and innovative ways to nurture PhD talent?
- Student Attraction & Retention: How do we enhance awareness about chip design to attract diverse talent? What strategies and resources can be implemented to build early excitement around a career in chip design and address the leaky talent pipeline through retention/retraining initiatives?
- Training & Education: What are the best ways to strategically incorporate IC design in early education? What programs or methods can be developed to enable our educators?
- Building Infrastructure: How can we overcome barriers like costly cloud services and fabrication resources to make educational infrastructure more accessible? What are some strategies to promote collaboration in education while centralizing, scaling and subsidizing infrastructure?

Presenters: Joe Cole, Synopsys, New York City, NY; Abi Ilumoka, National Science Foundation, Arlington, VA; Andrew Kahng, University of California, San Diego, CA; Matthew Kay, Naval Surface Warfare Center, Jasper, IN; Mark Willoughby, EuroPractice, Oxfordshire, United Kingdom; Jeff Parkhurst, Intel, Sacramento, CA; Antonio de la Serna, Siemens, Washington, DC

LARGE LANGUAGE MODEL - REVOLUTIONIZING THE ENTIRE COMPUTING PARADIGM

Time: 1:30 PM – 3:00 PM
Session Type: Special Session (Research)
Topic Area(s): AI
Room: 3006, 3rd Floor

Organizers: Sabya Das, Synopsys

Session Chair: Cong (Callie) Hao, Georgia Institute of Technology

Description: Large Language Models (LLMs) are fundamental machine learning models that use advanced algorithms to comprehend, process, and optimize natural language. These models are typically trained on vast amounts of data to learn patterns and use that in the processing and optimization phase. Due to the advent of LLMs, computing platforms are revolutionizing. This includes traditional Semiconductors as well as computing at both Cloud and Edge. In this session, we propose to have three complementary technologies that will cover this spectrum. In the first talk, the authors will discuss the LLM techniques that can be deployed for High-Level Synthesis Optimization and Verification. This approach enhances the efficiency and accessibility of AI accelerator development and serves as a bridge between AI algorithmic advancements and hardware innovation. The researchers in the second talk believe in and observe the importance of High-quality HDL in the design process. They will present that careful selection, filtering, and augmentation of data across HDLs can yield powerful LLM (and other) models that surpass current state-of-the-art models. This technique can be used to train various models for circuit design related activities. The final talk is about leveraging the extraordinary capabilities of Large Language Models to revolutionize AI accelerator design and enhance its accessibility.

- **New Solutions on LLM Acceleration, Optimization, and Application**
  Deming Chen, University of Illinois, Urbana-Champaign, IL
- **HDL-GPT: High Quality HDL Is All You Need**
  Ganapathy Parthasarathy, Synopsys, Mountain View, CA
- **LLM4AIGChip: Harnessing Large Language Models Towards Automation of AI Accelerator Design**
  Yingyan (Celine) Lin, Georgia Institute of Technology, Atlanta, GA

VISUALIZING THE FUTURE OF MULTI-DIE DESIGN WITH ANSYS & NVIDIA OMNIVERSE

Time: 1:45pm – 3:00pm
Session Type: Exhibitor Forum
Topic: Design
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Ansys and Nvidia collaborate closely to enable designers to bring a new paradigm to IC design: Visualizing and optimizing multi-die designs with NVIDIA's Omniverse technology. In combination with Ansys electromagnetic, thermal, and mechanical simulation it can provide capabilities never before seen in IC design. This session features representatives from Ansys and NVIDIA demonstrating Ansys solutions operating with NVIDIA's Omniverse for practical optimization solutions. The session will also cover key aspects of the companies' collaborations on AI and GPU design and enablement, as debuted in Jensen Huang's GTC 2024 keynote

Presenters: Rich Goldman, Ansys; Baskar Rajagopalan, NVIDIA

WITH GREAT POWER COMES GREAT RESPONSIBILITY – A GUIDE TO CUSTOMIZING YOUR PROCESSOR WITH VERIFICATION IN MIND

Time: 3:30 PM – 4:00 PM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Customization is now the way forward for increasing performance in electronic systems. By customizing the processor to the actual workload, you can gain massive improvements for power, performance, and area. Using the right tools, customization can be approached using a fast and easy iterative approach enabling rapid architecture exploration and automated RTL and SDK generation. But how can you keep control of the customizations made during the design process, and how can you ensure the design is easily verified once you have achieved the performance you need? The answer is in bounded customization. By adding custom instructions within set bounds, you can achieve a good balance of freedom and control. Because you will not need to re-verify the entire core, the verification process will be smooth. With bounded customization, there is no risk of dead silicon because the custom instructions cannot break the baseline core. By working with tools able to generate the customized RTL and SDK as well as a verification environment aiding the verification of the custom instructions, you gain the power to customize and the confidence to claim responsibility for the end result.

Speakers: Filip Benna, Brett Cline, Codasip

GLITZ, GLAM, AND BINARY JAM: A SYMPHONY OF NEW SECURITY TRENDS FOR DEEP NEURAL NETWORKS

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): AI
Room: 3002, 3rd Floor

Session Chairs: Benjamin Tan (University of Calgary)

Description: This session takes you through cutting-edge AI defenses: Explore novel strategies defending against adversarial examples, patches, and addressing privacy/IP concerns. Witness the fusion of technology and time, leveraging device aging to combat attacks. Dive into innovative watermarking frameworks and victim-focused defenses, strengthening DNNs' and LLMs' security. Join us in this AI Safeguard Showcase, revealing crucial insights into the dynamic universe of AI security and privacy. A condensed exploration of the future of AI defense awaits!

- **TBNet: A Neural Architectural Defense Framework Facilitating DNN Model Protection in Trusted Execution Environments**
  Ziyu Liu, Tong Zhou, Xiaolin Xu, Northeastern University, Boston, MA; Yukui Luo, University of Massachusetts, Dartmouth, Dartmouth, MA;
- **Older and Wise: The Marriage of Device Aging and Intellectual Property Protection of DNNs**
  Ning Lin, Shaocong Wang, Yue Zhang, Yangu He, Kwunhang Wong, Zhongrui Wang, The University of Hong Kong, Hong Kong; Arindam Basu, City University of Hong Kong, Hong Kong; Dashan Shang, Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China; Xiaoming Chen, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China;
- **QMark: Robust Watermarks for IP Protection of Quantized Large Language Models**
  Ruisi Zhang, Farinaz Koushanfar, University of California, San Diego, CA;
- **AdvHunter: Detecting Adversarial Perturbations in Black-Box Neural Networks through Hardware Performance Counters**
  Manaar Alam, Michail Maniatakos, New York University, Abu Dhabi, United Arab Emirates;
- **DNN-Defender: A Victim-Focused In-DRAM Defense Mechanism for Taming Adversarial Weight Attack on DNNs**
  Ranyang Zhou, Shaahin Angizi, New Jersey Institute of Technology, Newark, NJ; Sabbir Ahmed, State University of New York, Binghamton, NY; Adnan Siraj Rakin, Binghamton University, Binghamton, NY;
- **Defending against Adversarial Patches using Dimensionality Reduction**
  Nandish Chattopadhyay, Amira Guesmi, Muhammad Abdullah Hanif, Muhammad Shafique, New York University, Abu Dhabi, United Arab Emirates; Bassem Ouni, Technology Innovation Institute, Abu Dhabi, United Arab Emirates;
- **EOS: An Energy-Oriented Attack Framework for Spiking Neural Networks**
  Ning Yang, Fangxin Liu, Zongwu Wang, Haomin Li, Zhuoran Song, Shanghai Jiao Tong University, Shanghai, China; Songwen Pei, University of Shanghai for Science and Technology, Shanghai, China;
- **FastQuery: Communication-efficient Embedding Table Query for Private LLMs inference**
  Chenqi Lin, Tianshi Xu, Zebin Yang, Meng Li, Runsheng Wang, Ru Huang, Peking University, Beijing, China

HARDWARE SECURITY PRIMITIVES

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): Security
Room: 3012, 3rd Floor

Session Chair: Dean Sullivan (University of New Hampshire)

Description: This session includes eight papers on the latest development of hardware security primitives for security and privacy. The first paper describes a novel circuit architecture for true random number generation (TRNG). The second paper proposes an authenticated partial encryption protocol to enable secure testing of system in package (SiP). The third paper presents an architecture for the processing of multi-scalar multiplication, a fundamental cryptographic operation. Then we have a group of papers focusing on the acceleration of fully homomorphic encryption (FHE) based on the low-level operator Meta-OP (paper No. 4); a scalable memory mapping algorithm and a flexible no-stall hardware/software pipeline (paper No. 5); specialized units for the pipelined processing of FHE operations (paper No. 6); and 3D stacked memory (paper No. 7). The session concludes with the design and fabrication of a subthreshold SRAM PUF with zero bit error rate across all voltage/temperature corners.

- **DH-TRNG: A Dynamic Hybrid TRNG with Ultra-High Throughput and Area-Energy Efficiency**
  Yuan Zhang, Kuncai Zhong, Jiliang Zhang, Hunan University, Changsha, China;
- **GATE-SiP: Enabling Authenticated Encryption Testing in Systems-in-Package**
  Galib Ibne Haidar, Kimia Zamiri Azar, Hadi Mardani Kamali, Mark Tehranipoor, Farimah Farahmandi, University of Florida, Gainesville, FL;
- **Gypsophila: A Scalable and Bandwidth-Optimized Multi-Scalar Multiplication Architecture**
  Changxu Liu, Hao Zhou, Lan Yang, Jiamin Xu, Fan Yang, Fudan University, Shanghai, China; Patrick Dai, Semisand Chip Design Pte. Ltd, Singapore;
- **Alchemist: A Unified Accelerator Architecture for Cross-Scheme Fully Homomorphic Encryption**
  Jianan Mu, Husheng Han, Shangyi Shi, Jing Ye, Zizhen Liu, Shengwen Liang, Xing Hu, Huaiwei Li, Xiaowei Li, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Meng Li, Peking University, Beijing, China; Mingzhe Zhang, Institute of Information Engineering, Chinese Academy of Sciences, Beijing, China; Song Bian, Beihang University, Beijing, China;
- **An NTT/INTT Accelerator with Ultra-High Throughput and Area Efficiency for FHE**
  Zhaojun Lu, Weizong Yu, Peng Xu, Wei Wang, Huazhong University of Science and Technology, Wuhan, China; Jiliang Zhang, Hunan University, Changsha, China; Dengguo Feng, State Key Laboratory of Cryptology, Beijing, China;
- **PPGNN: Fast and Accurate Privacy-Preserving Graph Neural Network Inference via Parallel and Pipelined Arithmetic-and-Logic FHE Accelerator**
  Yuntao Wei, Xueyan Wang, Song Bian, Yicheng Huang, Weisheng Zhao, Beihang University, Beijing, China; Yier Jin, University of Science and Technology in China, Hefei, China;

- **A High-Throughput Private Inference Engine Based on 3D Stacked Memory**
  Zhaohui Chen, Qi Liu, Zhirui Li, Fahong Zhang, Yanheng Lu, Zhen Gu, Alibaba Group, Beijing, China; Ling Liang, Peking University, Beijing, China;
- **S2RAM PUF: An Ultra-low Power Subthreshold SRAM PUF with Zero Bit Error Rate**
  Li Ni, Jiliang Zhang, Hunan University, Changsha, China

HETEROGENEOUS AND RECONFIGURABLE ARCHITECTURE: APPLICATIONS AND TOOLS

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3003, 3rd Floor

Session Chairs: Jason Anderson (University of Toronto); Andrea Guerrieri (EPFL (Ecole polytechnique federale de Lausanne))

Description: Hardware accelerators are integral in modern computing systems to deliver the required performance-per-Watt efficiency by exploiting fine-grained spatial concurrency. Programmable and reconfigurable accelerators are important in extending hardware acceleration efficiency to a still larger and more diverse share of computing tasks. This session showcases novel applications of Field Programmable Gate Arrays, GPUs, and chiplets to accelerate new computing problems. This session also presents new advances in EDA algorithms to improve application mapping to Coarse-Grained Reconfigurable Architectures. The final paper explores reconfiguration within a von Neumann processor datapath to efficiently specialize to changing applications.

- **CLUMAP: Clustered Mapper for CGRAs with Predication**
  Omar Ismail, Jason H. Anderson, University of Toronto, Canada;
- **PT-Map: Efficient Program Transformation Optimization for CGRA Mapping**
  Bizhao Shi, Tuo Dai, Jiaxi Zhang, Xuechao Wei, Guojie Luo, Peking University, Beijing, China;
- **G-kway: Multilevel GPU-Accelerated k-way Graph Partitioner**
  Wan Luan Lee, Dian-Lun Lin, Tsung-Wei Huang, University of Wisconsin, Madison, WI; Shui Jiang, Tsung-Yi Ho, Bei Yu, The Chinese University of Hong Kong, Hong Kong; Yibo Lin, Peking University, Beijing, China;
- **SpectraFlux: Harnessing the Flow of Multi-FPGA in Mass Spectrometry Clustering**
  Tianqi Zhang, Sumukh Pinge, Tajana Rosing, University of California, San Diego, CA; Neha Prakriya, Jason Cong, University of California, Los Angeles, CA;
- **MSMAC: Accelerating Multi-Scalar Multiplication for Zero-Knowledge Proof**
  Pengcheng Qiu, Guiming Wu, Tingqiang Chu, Changzheng Wei, Runzhou Luo, Ying Yan, Wei Wang, Hui Zhang, Ant Group, Hangzhou, China;
- **PHD: Parallel Huffman Decoder on FPGA for Extreme Performance and Energy Efficiency**
  Yunkun Liao, Jingya Wu, Wenyan Lu, Xiaowei Li, Guihai Yan, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China;
- **Chiplever: Towards Effortless Extension of Chiplet-based System for FHE**
  Yibo Du, Huawei Li, Xiaowei Li, Yinhe Han, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China;Ying Wang, Fuping Li, Shengwen Liang, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Bing Li, Capital Normal University, Beijing, China;
- **Geneva: A Dynamic Confluence of Speculative Execution and In-Order Commitment Windows**
  Yanghee Lee, Jiwon Lee, Jaewon Kwon, Yongju Lee, Won Woo Ro, Yonsei University, Seoul, South Korea

MEMORIES ARE SMARTER THAN EVER BEFORE

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3004, 3rd Floor

Session Chairs: Peipei Zhou (University of Pittsburgh); Xueqing Li (Tsinghua University)

Description: Processing-in-memory (PIM) has been extensively studied in the last few years, but memories never stop evolving, providing more processing power and functions. The first paper proposes a ReRAM-based PIM architecture for accelerating sparse conjugate gradient solvers, followed by the second paper introducing an efficient MAC scheme for MRAM-based PIM. In the next two papers, emerging devices are employed as a key computing component in the system, demonstrating its effectiveness. Finally, the last three papers discuss the various design approaches to improve SRAM-based PIM hardware, ranging from circuits to modeling.

- **ReCG: ReRAM-Accelerated Sparse Conjugate Gradient**
  Mingjia Fan, Dechuang Yang, Weifeng Liu, China University of Petroleum-Beijing, Beijing, China;Xiaoming Chen, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China;
- **FRM-CIM: Full-Digital Recursive MAC Computing in Memory System Based on MRAM for Neural Network Applications**
  Jinkai Wang, Zekun Wang, Bojun Zhang, Zhengkun Gu, Youxiang Chen, Weisheng Zhao,Yue Zhang, Beihang University, Beijing, China;
- **Toward High-Accuracy, Programmable Extreme-Edge Intelligence for Neuromorphic Vision Sensors Utilizing Magnetic Domain Wall Motion-based MTJ**
  Md Abdullah-Al Kaiser, Gourav Datta, Peter Beerel, University of Southern California, Los Angeles, CA; Akhilesh Jaiswal, University of Wisconsin, Madison, WI;
- **Cross-Layer Exploration and Chip Demonstration of In-Sensor Computing for Large-Area Applications with Differential-Frame ROM-Based Compute-In-Memory**
  Jialong Liu, Wenjun Tang, Deyun Chen, Chen Jiang, Huazhong Yang, Xueqing Li, Tsinghua University, Beijing, China;
- **An In-Memory Computing Accelerator with Reconfigurable Dataflow for Multi-Scale Vision Transformer with Hybrid Topology**
  Zhiyuan Chen, Yufei Ma, Keyi Li, Yifan Jia, Guoxiang Li, Meng Wu, Tianyu Jia, Le Ye, Ru Huang, Peking University, Beijing, China;

- **Towards Efficient SRAM-PIM Architecture Design by Exploiting Unstructured Bit-Level Sparsity**
  Cenlin Duan, Jianlei Yang, Yiou Wang, Yikun Wang, Yingjie Qi, Xiaolin He, Xueyan Wang, Xiaotao Jia, Weisheng Zhao, Beihang University, Beijing, China; Bonan Yan, Peking University, Beijing, China
- **OPTIMA: Design-Space Exploration of Discharge-Based In-SRAM Computing: Quantifying Energy-Accuracy Trade-offs**
  Saeed Seyedfaraji, Severin Jager, Salar Shakibhamedan, Asad Aftab, Semeen Rehman, Technische Universitat Wien, Austria

MODELING, SOFTWARE, AND ARCHITECTURE JUST GOT SMARTER

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): Embedded Systems
Room: 3001, 3rd Floor

Session Chairs: Di Liu (Norwegian University of Science and Technology)

Description: This section presents new developments in embedded modeling, software and architecture. The first paper develops a deep-to-shallow transformable neural architecture search; the second one focuses on efficient code generation for data-intensive Simulink models; the third paper presents a framework of translating regular expressions. The fourth paper investigates a dynamic mechanism for reducing control flow divergence in GPUs. The next paper investigates methods to boost the efficiency of data deduplication; the sixth one develops code optimization schemes to accelerate stencil code kernels; the seventh paper investigates a novel approach to decompose tasks on intermittent computing systems; and the last one proposes a light-weighted idle time stealing strategy.

- **Double-Win NAS: Towards Deep-to-Shallow Transformable Neural Architecture Search for Intelligent Embedded Systems**
  Xiangzhong Luo, Hao Kong, Shuo Huai, Weichen Liu, Nanyang Technological University, Singapore; Di Liu, Norwegian University of Science and Technology, Trondheim, Norway;
- **Efficient Code Generation for Data-Intensive Simulink Models via Redundancy Elimination**
  Zehong Yu, Zhuo Su, Yu Jiang, Tsinghua University, Beijing, China; Aiguo Cui, Huawei, Shanghai, China; Rui Wang, Capital Normal University, Beijing, China;
- **ALVEARE: a Domain-Specific Framework for Regular Expressions**
  Filippo Carloni, Davide Conficconi, Marco D. Santambrogio, Politecnico di Milano, Italy;
- **Control Flow Divergence Optimization by Exploiting Tensor Cores**
  Weiguang Pang, Kexue Fu, longxiang Gao, Qilu University of Technology, Jinan, China; Xu Jiang, University of Electronic Science and Technology of China, Chengdu, China; Songran Liu, Northeastern University, Shenyang, China; Lei Qiao, Beijing Institute of Control Engineering, Beijing, China; Wang Yi, Uppsala University, Uppsala, Sweden;
- **FinerDedup: Sifting Fingerprints for Efficient Data Deduplication on Mobile Devices**
  Xianzhang Chen, Xingjie Zhou, Wei Li, Xi Yu, Duo Liu, Yujuan Tan, Ao Ren, Chongqing University, Chongqing, China;
- **SARIS: Accelerating Stencil Computations on Energy-Efficient RISC-V Compute Clusters with Indirect Stream Registers**
  Paul Scheffler, Luca Colagrande, ETH Zurich, Zurich, Switzerland; Luca Benini, Universita di Bologna, Bologna, Italy;
- **Cache-aware Task Decomposition for Efficient Intermittent Computing Systems**
  Shuo Xu, Wei Zhang, Mengying Zhao, Zimeng Zhou, Lei Ju, Shandong University, Qingdao, China;
- **How to Steal CPU Idle Time When Synchronous I/O Mode Becomes Promising**
  Chun-Feng Wu, National Yang Ming Chiao Tung University, Hsinchu, Taiwan; Yuan-Hao Chang, Academia Sinica, Taipei, Taiwan; Ming-Chang Yang, The Chinese University of Hong Kong, Hong Kong; Tei-Wei Kuo, National Taiwan University, Taipei, Taiwan

ON THE RIGHT PATH: NAVIGATING THE MAZE OF ROUTING AND CLOCK TREE SYNTHESIS!

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): EDA
Room: 3010, 3rd Floor

Session Chairs: Uday Mallappa (UC San Diego); Satish Sivaswamy (AMD)

Description: You have made it all the way here! So come hither and learn about the latest advanced algorithms to address the increasingly complex signal and data routing challenges! These include a novel reinforcement learning-based approach for obstacle-aware Steiner trees, an insightful pin-access co-optimization framework through on-the-fly standard cell pin layout regeneration, top-level design routing, minimal area length matching for PCB routing, a priori resource allocation-based router, a latency/load capacitance-centric approach for clock tree synthesis, and a GNN-assisted back-side clock routing algorithm.

- **Obstacle-Aware Length-Matching Routing for Any-Direction Traces in Printed Circuit Board**
  Weijie Fang, Longkun Guo, Jiawei Lin, Fuzhou University, Fuzhou, China; Xiong Silu, Huawei, Hangzhou, China; Huan He, Hangzhou Huawei Enterprises Telecommunication Technologies Co., LTD, Hangzhou, China; Jiacen Xu, Shanghai LEDA Technology Co., Ltd, Shanghai, China; Jianli Chen, Fudan University, Shanghai, China;
- **Toward Controllable Hierarchical Clock Tree Synthesis with Skew-Latency-Load Tree**
  Weiguo Li, Minnan Normal University, Zhangzhou, China; Zhipeng Huang, Xingquan Li, Peng Cheng Laboratory, Shenzhen, China; Bei Yu, The Chinese University of Hong Kong, Hong Kong; Wenxing Zhu, Fuzhou University, Fuzhou, China;
- **Net Resource Allocation: A Desirable Initial Routing Step**
  Zhisheng Zeng, Biwei Xie, Yungang Bao, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Zhipeng Huang, Xingquan Li, Peng Cheng Laboratory, Shenzhen, China; Jikang Liu, Ye Cai, Shenzhen University, Shenzhen, China;
- **Arbitrary-size Multi-layer OARSMT RL Router Trained with Combinatorial Monte-Carlo Tree Search**
  Liang-Ting Chen, Hung-Ru Kuo, Yih-Lang Li, Mango C.-T. Chao, National Yang Ming Chiao Tung University, Hsinchu, Taiwan;

- **GNN-assisted Back-side Clock Routing Methodology for Advance Technologies**
  Nesara Eranna Bethur, Advanced Micro Devices, Inc., Austin, TX; Pruek Vanna-iampikul, Lingjun Zhu, Sung Kyu Lim, Georgia Institute of Technology, Atlanta, GA; Odysseas Zografos, Giuliano Sisto, Dragomir Milojevic, Geert Hellings, Julien Ryckaert, Francky Catthoor, imec, Leuven, Belgium; Alberto Garcia-Ortiz, University of Bremen, Germany;
- **DGR: Differentiable Global Router**
  Wei Li, Carnegie Mellon University, Pittsburgh, PA; Anthony Agnesina, Haoyu Yang, Anand Rajaram, Haoxing Ren, NVIDIA, Austin, TX; Chia-Tung Ho, University of California, San Diego, CA;
- **Top-Level Routing for Multiply-Instantiated Blocks with Topology Hashing**
  Jiarui Wang, Xun Jiang, Yibo Lin, Peking University, Beijing, China;
- **Concurrent Detailed Routing with Pin Pattern Re-generation for Ultimate Pin Access Optimization**
  Ying-Jie Jiang, Shao-Yun Fang, National Taiwan University of Science and Technology, Taipei, Taiwan

SILICON STAIRWAYS: CLIMBING THE LAYERS OF 3D IC INNOVATION

Time: 3:30 PM – 5:30 PM
Session Type: Research Manuscript
Topic Area(s): EDA
Room: 3008, 3rd Floor

Session Chairs: Furkan Eris (AMD); Nader Sehatbakhsh (UCLA)

Description: This session converges on the forefront of semiconductor technology, highlighting revolutionary approaches in chip design that blend optical networking, artificial intelligence, and sustainability. It further unravels the intricate world of 3D integrated

- **Explainable Fuzzy Neural Network with Multi-Fidelity Reinforcement Learning for Micro-Architecture Design Space Exploration**
  Hanwei Fan, Ya Wang, Tingyuan Liang, Wei Zhang, Hong Kong University of Science and Technology, Hong Kong, Hong Kong; Sicheng Li, Alibaba Group, Sunnyvale, CA;
- **A High Level Approach to Co-Designing 3D ICs**
  Daniel Xing, Ankur Srivastava, University of Maryland, College Park, MD;
- **Multi-Resonance Mesh-Based Wavelength-Routed Optical Networks-on-Chip**
  Zhidan Zheng, Liaoyuan Cheng, Qingyu Li, Alexandre Truppel, Tsun-Ming Tseng, Ulf Schlichtmann, Technical University Munich, Muenchen, Germany; Kanta Arisawa, Shigeru Yamashita, Ritsumeikan University, Kusatsu, Japan;
- **Redistribution Layer Routing with Dynamic Via Insertion Under Irregular Via Structure**
  Je-Wei Chuang, Zong-Han Wu, Bo-Ying Huang, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan;
- **OTPlace-Vias: A Novel Optimal Transport Based Method for High Density Vias Placement in 3D Circuits**
  Lin Chen, Qi Xu, Hu Ding, University of Science and Technology of China, Hefei, China;
- **Voronoi Diagram-based Multiple Power Plane Generation on Redistribution Layers in 3D ICs**
  Chia-Wei Lin, Jing-Yao Weng, Mark Po-Hung Lin, National Yang Ming Chiao Tung University, Hsinchu, Taiwan; I-Te Lin, Ho-Chieh Hsu, Chia-Ming Liu, Synopsys, Hsinchu, Taiwan;
- **Thermal Resistance Network Derivative (TREND) Model for Efficient Thermal Simulation and Design of ICs and Packages**
  Shunxiang Lan, Min Tang, Junfa Mao, Shanghai Jiao Tong University, Shanghai, China; Liang Chen, Shanghai University, Shanghai, China;
- **3D-Carbon: An Analytical Carbon Modeling Tool for 3D and 2.5D Integrated Circuits**
  Yujie Zhao, Yang (Katie) Zhao, Cheng Wan, Yingyan (Celine) Lin, Georgia Institute of Technology, Atlanta, GA

3DIC DESIGN ECOSYSTEM - THE CATS THAT NEED HERDING!

Time: 1:30 PM – 3:00 PM
Session Type: Research Panel
Topic Area(s): Design
Room: 3014, 3rd Floor

Organizer: Sagar Kekare, Intel, Santa Clara, CA; Shimeng Yu, Georgia Institute of Technology, Atlanta, GA

Moderator: Daniel Nenni, SemiWiki, San Jose, CA

Description: At the end of 2D scaling of Moore's law, 3D integrated circuits that take advantages of advanced packaging and heterogeneous integration offers many prospects of extending the chip density scaling and the system performance improvements for the next decade. Much of 3DIC design activity in the industry today is done via different teams within the same chipmaker company. 3DICs hold the potential to not only make the chip architecture heterogeneous, and chiplet sourcing to be highly diversified. Moreover, 3DICs themselves have a few avenues to be realized towards commercial success, ranging from true disaggregated chiplets to sequential stacked processing. This presses us to answer a few key questions:

1. Technology:
   a. How will heat dissipation be managed, are new cooling techniques are being pursued to mitigate the thermal challenge?
   b. How to design the power delivery network from the board to the substrate to the multi-tier of 3D stack with minimal voltage drop and high-power conversion efficiency? How to design the backside power delivery in leading edge node CMOS with 3D stacking?
   c. How to ensure signal integrity, yield and reliability between multiple tiers of 3D stacking, and what testing and standardization efforts are needed to embrace the heterogeneous dies from different designers and foundries?
2. EDA flows and interoperability
   a. Will the ecosystem extend the same standards-based interoperability of design tools, flows and methodologies to 3DIC, as enjoyed by monolithic system designers today?
   b. How can EDA industry help system designers in planning, managing and tracking their complex 3DIC projects in implementation, analysis, and signoffs?

3. Roadmap:
   a. Is the roadmap to sequential monolithic stacked 3DIC an inevitability? What factors lead the industry to it?
   b. What are the boundaries between monolithic 3D integration (with sequential processing at BEOL) and heterogenous 3D integration (with die stacking or bonding)?

Are we as an industry able to apply lessons from the past struggles with monolithic chip design and interoperability to this emerging challenge? This panel will discuss the need, scope of solution and potential candidate efforts already in motion.

Panelists: Lalitha Immaneni, Intel, Tempe, AZ; Trupti Deshpande, Qualcomm, Santa Clara, CA; Deepak Kulkarni, AMD, Austin, TX; Puneet Gupta, University of California, Los Angeles, CA; Dragomir Milojevic, imec, Leuven, Belgium; Rob Aitken, Synopsys, San Jose, CA

EMERGING TECHNOLOGIES FOR ENERGY-EFFICIENT NEUROMORPHIC EDGE COMPUTING

Time: 3:30 PM – 5:30 PM
Session Type: Special Session (Research)
Topic Area(s): AI
Room: 3006, 3rd Floor

Organizer: Luis Guerra e Silva, INESC-ID

Session Chairs: Elena Ioana Vatajelu, TIMA Laboratory

Description: This special session aims to discuss various approaches to neuromorphic computing for edge AI applications focusing on emerging technologies, novel architectures and sensing modalities to enhance perception. We will have an introductory tutorial dedicated to current strategies to achieve low-power computing at the Edge based on CMOS and post-CMOS technologies. Then, we will focus on limitations of current solutions and introduce four different strategies to overcome such limitations in the remaining talks. These talks are related to four European projects funded under the same call entitled “Ultra-low-power, secure processors for edge computing”. These projects aiming at reducing by two orders of magnitude current energy consumptions and with budgets between 8 and 10 million Euros gather a large number of academic and industrial key European players on computing technologies. The second talk discusses design strategies in the CONVOLVE project for SoCs dedicated to edge AI applications by taking a holistic approach to design space exploration. Trade-offs tackling the whole tool chain will be presented to achieve substantial improvements in energy consumptions. The third talk discusses the neuromorphic approach taken in the NimbleAI project combining a vertebrate eye-inspired foveated DVS chip coupled with an insect eye-inspired microlens array to sense and process light fields at different resolutions with minimal latency and energy consumption. The final talk discusses the development of neuromorphic accelerators based on integrated photonics in the NEUROPULS project. Photonic architectures leveraging phase-change and III-V materials for neuromorphic computing will be presented. We expect this session to foster opportunities to link these initiatives at the EU level with similar initiatives worldwide.

- **Chip Technology and Computing for Edge-AI Devices: the Need of New Mind Set to Sustain the Future**
  Said Hamdioui, Delft University of Technology
- **Achieving PetaOps/W Edge-AI Processing**
  Henk Corporaal, Eindhoven University of Technology, Eindhoven, Netherlands
- **Enabling New Neuromorphic Visual Sensing Modalities**
  Xabier Iturbe, Ikerlan Technology Centre, Mondragon, Spain
- **Neuromorphic Architectures Based on Augmented Silicon Photonics Platforms**
  Fabio Pavanello, CROMA (CNRS), Grenoble, France

WORK-IN-PROGRESS POSTERS

Time: 6:00 PM – 7:00 PM
Session Type: Work-in-Progress Posters
Room: 2nd Floor Lobby

ACCELERATING DNN EXECUTION VIA WEIGHT AND DATA ADAPTIVE N:M PRUNING

Sai Qian Zhang, New York University, New York, NY; Thierry Tambe, Gu-Yeon Wei, David Brooks, Harvard University, Cambridge, MA

ACCELERATING HETEROGENEOUS WORKLOADS USING A RECONFIGURABLE IN-MEMORY COMPUTING ARCHITECTURE

Yanfeng Yang, Yi Zou, Yiyang Lin, Xianfeng Song, Yingbo Hao, South China University of Technology, Guangzhou, China

ACCELERATING LARGE-SCALE SPARSE LU FACTORIZATION FOR RF CIRCUIT SIMULATION

Guofeng Feng, Hongyu Wang, Zhuoqiang Guo, Mingzhen Li, Tong ZhaoWeile Jia, Guangming Tan, Ninghui Sun, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Zhou Jin, China University of Petroleum-Beijing, Beijing, China;

ACCELERATING RANGE-JOINS FOR BIG DATA GENOMIC VARIANT ANNOTATION ON HBM-ENABLED FPGAS

Aman Sinha, Shih-Chen Lo, Bo-Cheng Lai, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

ADAP-CIM: COMPUTE-IN-MEMORY BASED NEURAL NETWORK ACCELERATOR USING ADAPTIVE POSIT AND SPECULATIVE ALIGNMENT

Jingyu He, Fengbin Tu, Tim Cheng, Chi Ying Tsui, Hong Kong University of Science and Technology, Hong Kong, Hong Kong

ADAPTIVE GRAPH LEARNING FOR EFFICIENT THERMAL ANALYSIS OF THE CHIPLET SYSTEM UNDER INTERFACE VARIATIONS

Jingbo Sun, Zhenyu Wang, Vidya A. Chhabria, Arizona State University, Tempe, AZ; Frank Liu, Oak Ridge National Laboratory, Oak Ridge, TN; Yu Cao, University of Minnesota, Minneapolis, MN

WORK-IN-PROGRESS POSTERS (CONTINUED)

ADVANCED ANALOG DESIGN OPTIMIZATION: COMPARISON BETWEEN REINFORCEMENT LEARNING AND HEURISTIC ALGORITHMS

Michel Chevalier, Antoine Vialle, Jules Coulon, Severin Trochut, Roberto Guizzetti, S Pascal Urard, STMicroelectronics, Crolles, France; Lioua LabrakRémy Cellier Nacer Abouchi, Institut des Nanotechnologies de Lyon, Lyon, France; John Samuel, CPE Lyon, Lyon, France;

AFFINITY-BASED OPTIMIZATIONS OF HOMOMORPHIC ENCRYPTION OPERATIONS ON PROCESSING-IN-DRAM

Kevin Nam, Heon Hui Jung, Yunheung Paek, Seoul National University, Seoul, South Korea; Hyunyoung Oh, Gachon University, Seongnam, South Korea;

AGILE DISCOVERY OF EFFICIENT REAL-TIME SYSTEMS-ON-CHIPS IN THE HETEROGENEOUS ERA

Subhankar Pal, Aporva Amarnath, ; Augusto Vega, John-David Wellman, IBM Research, Yorktown Heights, NY; Behzad Boroujerdian, The University of Texas at Austin, Cambridge, MA; Alper Buyuktosunoglu, Pradip Bose, IBM Thomas J. Watson Research Center, Yorktown Heights, NY; Vijay Janapa Reddi, Harvard University, Cambridge, MA;

ANALYSIS OF 64-BIT PARALLEL PREFIX ADDERS AND 32-BIT MATRIX MULTIPLY UNITS DESIGNED WITH 7-NM CNFET

Chenlin Shi, Shinobu Miwa, Tongxin Yang, Hayato Yamaki, Hiroki Honda, University of Electro-Communications, Chofu, Japan Ryota Shioya, The University of Tokyo, Japan;

ATAFAN: DESIGN-FRIENDLY AGING-AWARE TIMING ANALYSIS FRAMEWORK BASED ON HYBRID GRAPH NETWORK

Jinfeng Ye, Pengpeng Ren, Haibao Chen, ; Zhigang Ji, Shanghai Jiao Tong University, Shanghai, China; Chao Yang, Zejian Cai, T-Head Semiconductor Co., Ltd, Shanghai, China; Ye Wei, Hui Fang, Loughborough University, Loughborough, United Kingdom

AUTOTILE: AUTONOMOUS TASK-TILING FOR DEEP INFERENCE ON BATTERY-LESS EMBEDDED SYSTEM

Jishnu Banerjee, Sahidul Islam, Wei Wei, Chen Pan, Mimi Xie, The University of Texas at San Antonio, TX

CIM FOR LLM: A COMPUTE-IN-MEMORY ARCHITECTURE FOR EFFICIENT LARGE LANGUAGE MODEL INFERENCE

Jung-Fang Ke, Zhi-Wei Liu, Yu-Guang Chen, National Central University, Taoyuan City, Taiwan; En-Ming Huang, Chun-Yi Lee, National Tsing Hua University, Hsinchu, Taiwan

CIMAP: A CIM CROSSBAR ARRAY DATA MAPPING METHODOLOGY FOR UNSTRUCTURED SPARSE CONVOLUTIONAL NEURAL NETWORKS

Yan-Lin Hung, Bing-Han Liu, Zun-Sheng Wu, Bo-Cheng Lai, Shyh-Jye Jou, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

CIRCUIT TRANSFORMER: END-TO-END LOGIC SYNTHESIS BY PREDICTING THE NEXT GATE

Xihan Li, Jun Wang, University College, London, United Kingdom; Xing Li, Lei Chen, Xing Zhang, Mingxuan Yuan, Huawei, Hong Kong, Hong Kong;

CIRSTAG: CIRCUIT STABILITY ANALYSIS VIA GRAPH NEURAL NETWORKS

Wuxinlin Cheng, Yihang Yuan, Ali Aghdaei, Zhuo Feng, Stevens Institute of Technology, Hoboken, NJ; Chenhui Deng, Zhiru Zhang, Cornell University, Ithaca, NY;

COMPRESSED LATENT REPLAYS FOR LIGHTWEIGHT CONTINUAL LEARNING ON SPIKING NEURAL NETWORKS

Alberto Dequino, Luca Benini, Francesco Conti, University of Bologna, Italy; Alessio Carpegna, Davide Nadalini, Alessandro Savino, Stefano Di Carlo, Politecnico di Torino, Italy;

COMPRESSION WITH ATTENTION: LEARNING IN LOWER DIMENSIONS

Gaurav Singh, Kia Bazargan, University of Minnesota, Minneapolis, MN

CONFIDENTIAL COMPUTING WITH HETEROGENEOUS DEVICES AT CLOUD-SCALE

Aritra Dhar, Renzo Andri, Huawei, Zurich, Switzerland; Supraja Sridhara, Shweta Shinde, Srdjan Capkun, ETH Zürich, Switzerland

A CROSSTALK-AWARE TIMING PREDICTION METHOD IN ROUTING

Leilei Jin, Jiajie Xu, Wenjie Fu, Hao Yan, Longxing Shi, Southeast University, Nanjing, China

DATIS: DRAM ARCHITECTURE AND TECHNOLOGY INTEGRATED SIMULATION

Zheng Qiao, Chen Zhang, Zhuoshan Zhou, Yong Liu, Zhigang Ji, Shanghai Jiao Tong University, Shanghai, China; Ru Huang, Peking University, Beijing, China

DB-HUNTER: INTERACTIVE-GUIDED DIFFERENTIAL TESTING FOR FPGA SIMULATION DEBUGGER

Shikai Guo, Xiaoyu Wang, Zhihao Xu, Xiaochen Li, He Jiang, Dalian University of Technology, Dalian, China

DEFENDING MEMBERSHIP INFERENCE ATTACK ON EDGE USING TRUSTED EXECUTION ENVIRONMENTS

Cheng-Yun Yang, Gowri Ramshankar, Sudarshan Nambiar, Evan Miller, Xun Zhang, Nicholas Eliopoulos, Purvish Jajal, Dave Tian, Yung-Hsiang Lu, Purdue University, West Lafayette, IN;Shuo-Han Chen, National Yang Ming Chiao Tung University, Hsinchu, Taiwan; Chiy-Ferng Perng, West Lafayette, IN

DISTRIBUTED INFERENCE OF DL WORKLOADS ON CIM-BASED HETEROGENEOUS ACCELERATORS

Mojtaba AlShams, Kamilya Smagulova, Ahmed Eltawil, King Abdullah University of Science and Technology, Thuwal, Saudi Arabia; Mohammed Fouda, Rain Neuromorphics Inc., San Francisco, CA

DISTRIBUTION-GUIDED FAIRNESS CALIBRATION IN LEARNING

Yi Sheng, Junhuan Yang, Zhepeng Wang, Weiwen Jiang, Lei Yang, George Mason University, Fairfax, VA; Qian Lou, University of Central Florida, Orlando, FL

WORK-IN-PROGRESS POSTERS (CONTINUED)

A DIVIDE-AND-CONQUER PEBBLING STRATEGY FOR ORACLE SYNTHESIS IN QUANTUM COMPUTING

Kezhen Zhang, Riling Li, Institute of Software, Chinese Academy of Sciences, Beijing, China; Mingsheng Ying, Tsinghua University, Beijing, China

DNNPHASER: ENHANCING DATA LOCALITY USING MULTIPHASE RING DATAFLOW FOR SPATIAL ACCELERATORS

Chia-Wei Chang, Jing-Jia Liou, National Tsing Hua University, HsinChu, Taiwan

DOCTOR: DYNAMIC ON-CHIP REMEDIATION AGAINST TEMPORALLY-DRIFTING THERMAL VARIATIONS TOWARD SELF-CORRECTED PHOTONIC TENSOR ACCELERATORS

Haotian Lu, Jiaqi Gu, Arizona State University, Tempe, AZ; Sanmitra Banerjee, NVIDIA, San Jose, CA

DON'T CACHE, SPECULATE!: SPECULATIVE ADDRESS TRANSLATION FOR FLASH-BASED STORAGE SYSTEMS

Hyungjin Kim, Seongwook Kim, Junhyeok Park, Gwangeun Byeon, Seokin Hong, Sungkyunkwan University, Suwon, South Korea

A DRAM-BASED PIM ARCHITECTURE FOR ACCELERATED AND ENERGY-EFFICIENT EXECUTION OF TRANSFORMERS

Gian Singh, Sarma Vrudhula, Arizona State University, Tempe, AZ

DRL-BASED VOLTAGE OPTIMIZATION FOR MULTIPLE DROPLET ROUTING IN DMFBS

Tomohisa Kawakami, Hiroyuki Tomiyama, Shigeru Yamashita, Ritsumeikan University, Kusatsu, Japan; Hiroki Nishikawa, Osaka University, Suita, Japan

DTRANS: A DATAFLOW-TRANSFORMATION FPGA ACCELERATOR WITH NONLINEAR-OPERATORS FUSION AIMING FOR THE GENERATIVE MODEL

Xuanzheng Wang, Peng Qu, Youhui Zhang, Tsinghua University, Beijing, China

DUAL-AXIS ECC: VERTICAL AND HORIZONTAL ERROR CORRECTION

Giyong Jung, Hee Ju Na, Sang-Hyo Kim, Jungrae Kim, Sungkyunkwan University, Suwon, South Korea

E-BFC: ULTRA ENERGY-EFFICIENT BUTTERFLY COUNTING IN BIPARTITE NETWORKS VIA ALGORITHM-ARCHITECTURE CO-OPTIMIZATION

Haiyang Liu, Xueyan Wang, Jianlei Yang, Xiaotao Jia, Weisheng Zhao, Beihang University, Beijing, China; Gang Qu, University of Maryland, College Park, MD

AN EFFICIENT AND SCALABLE CLOCKING ASSIGNMENT ALGORITHM FOR MULTI-THREADED MULTI-PHASE SINGLE FLUX QUANTUM CIRCUITS

Robert Aviles, Xi Li, Lei Lu, Zhaorui Ni, Peter Beerel, University of Southern California, Los Angeles, CA

AN EFFICIENT FRAMEWORK FOR HIGH-FIDELITY AUTOMOTIVE EXTERIOR DESIGN

Changdi Yang, Zichong Meng, Tim Ruppecht, Caiyue Lai, Enfu Nan, Jun Liu, Zhijun Hu, Pu Zhao, Yanzhi Wang, Northeastern University, Boston, MA

EFFICIENT MEMORY PLACEMENT IN CHIPLET-BASED SYSTEMS

Shant Rakshit, Himanshu Kumar Rai, International Institute of Information Technolgy, Bangalore, India

EFFICIENT PREDICTION OF SRAM READ ACCESS TIME AND YIELD VIA NEURAL NETWORK LEVERAGING TRANSFER LEARNING AND TRANSFORMER MODELS

Sungho Park, Jaehyeon Moon, Giseok Kim, Dohyung Kim, Seong-Ook Jung, Bumsub Ham, Hanwool Jeong, Kwangwoon University, Seoul, South Korea

EFFIPIPE: TOWARDS ENERGY-EFFICIENT LARGE-SCALE MODEL TRAINING ON COMMODITY GPUS

Zijie Tian, Shuo Wang, Yuhao Zhang, Youyou Lu, Jiwu Shu, Tsinghua University, Beijing, China

ELIMINATE CONTROL DIVERGENCE IN SPMV VIA IN-SRAM REDUCTION

Zhang Dunbo, Jia Chaoyang, Li Shen, Lu Kai, National University of Defense Technology, Changsha, China

EVERGREEN: COMPREHENSIVE CARBON MODELING FOR PERFORMANCE-EMISSION TRADEOFFS

Tersiteab Adem, Andrew McCrabb, Vidushi Goyal, Valeria Bertacco, University of Michigan, Ann Arbor, MI

A FAST IR-DROP MODELING FOR IN-RRAM COMPUTING CONSIDERING DATA ALLOCATION

Shih-Han Chang, Tung Lin, Chien-Nan Liu, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

FOTA-QUANT: FPGA-ORIENTED TOKEN ADAPTIVE QUANTIZATION FRAMEWORK FOR THE ACCELERATION OF LLMS

Xuan Shen, Zhaoyang Han, Peiyan Dong, Yanyue Xie, Zhenglun Kong, Zhengang Li, Yanzhi Wang, Miriam Leeser, Northeastern University, Boston, MA

FULLY AUTOMATED IMPLEMENTATION OF RESERVOIR COMPUTING MODELS ON FPGAS FOR NANOSECOND INFERENCE TIMES

Fabian Legl, Ingenieurbuero fuer Thermoakustik GmbH, Puchheim, Germany; Jonas Kantic, Technical University of Munich, Germany

GL0AM: GPU LOGIC SIMULATION USING 0-DELAY AND RE-SIMULATION ACCELERATION METHOD

Yanqing Zhang, NVIDIA, Santa Clara, CA; Haoxing Ren, Brucek Khailany, NVIDIA, Austin, TX

WORK-IN-PROGRESS POSTERS (CONTINUED)

GRAPH ATTENTION NETWORK-BASED SPARSE FORMAT SELECTION FOR ACCELERATING SPMM ON GPUS

Dezhan Tu, Tiandong Zhao, Zhuofu Tao, Tianjia Zhou, Lei He, University of California, Los Angeles, CA

H4H: HYBRID CONVOLUTION-TRANSFORMER ARCHITECTURE SEARCH FOR NPU-CIM HETEROGENEOUS SYSTEMS FOR AR/VR APPLICATIONS

Yiwei Zhao, Phillip Gibbons, Carnegie Mellon University, Pittsburgh, PA; Ziyun Li, Chiao Liu, Meta, Redmond, WA; Win-San Khwa, Yi-Lun Lu, TSMC, Hsinchu, Taiwan; Xiaoyu Sun, TSMC, San Jose, CA; Sai Qian Zhang, New York University, New York, NY; Syed Shakib Sarwar, Meta, Bellevue, WA; Kleber Stangherlin, Meta, Toronto, Canada; Jorge Gomez, Meta, Burlingame, WA; Jae-sun Seo, Cornell Tech, New York, NY; Barbara De Salvo, Meta, Belmont, CA;

HARDWARE PDE SOLVERS USING DYNAMIC STOCHASTIC COMPUTING

Hongqiao Zhang, Zhengkun Yu, Siting Liu, Shanghai Tech University, Shanghai, China; Jie Han, University of Alberta, Edmonton, Canada;

HDFUSION: HIERARCHICAL DATA FUSION FOR ROBUST DEEP TISSUE SENSING

Tailai Lihe, Begum Kasap, Kourosh Vali, Soheil Ghiasi, University of California, Davis, CA

HETEROGENEOUS VECTOR ACCELERATOR FOR MATRIX MULTIPLICATIONS ON FPGA

Jay Shah, International Institute of Information Technology, Bangalore, India

HIGH-PERFORMANCE REMOTE DATA PERSISTING FOR KEY-VALUE STORES VIA PERSISTENT MEMORY REGION

Yongping Luo, Peiquan Jin, Xiaoliang Wang, Zhaole Chu, University of Science and Technology of China; Hefei, China; Kuankuan Guo, Jinhui Guo, Peng Xu, Fei Liu, Bytedance Inc., Beijing, China

HRING: A HIERARCHICAL RING DESIGN METHOD FOR WAVELENGTH-ROUTED OPTICAL NETWORKS-ON-CHIP

Zhidan Zheng, Meng Lian, Mengchu Li, Tsun-Ming Tseng, Ulf Schlichtmann, Technical University of Munich, Germany

HYBRID STOCHASTIC COMPUTING OF LINEAR TIME O(N) AND ITS IN-MEMORY COMPUTING FOR HIGH PERFORMANCES

Yuhao Chen, Li Hongge, Xiaoyu Guo, Yinjie Song, Xinyu Zhu, Beihang University, Beijing, China

HYDROGEN: CONTENTION-AWARE HYBRID MEMORY MANAGEMENT FOR HETEROGENEOUS CPU-GPU ARCHITECTURES

Yiwei Li, Mingyu Gao, Tsinghua University, Beijing, China

IMPROVEMENTS TO DELAY-DRIVEN LUT MAPPING

Alessandro Tempia Calvino, Giovanni De Micheli, École Polytechnique Fédérale de Lausanne, Switzerland; Alan Mishchenko, Robert Brayton, University of California, Berkeley, CA

AN INSTANT LEAFCELL LAYOUT AUTO-GENERATOR FOR AREA COMPACT MEMORY DESIGN AUTOMATION

Wonjoon Jo, Giseok Kim, Sungho Park, Seong-Ook Jung, Yonsei University, Seoul, South Korea; Hanwool Jeong, Kwangwoon University, Seoul, South Korea

INSTRUCTION SEQUENCE GENERATION USING REINFORCEMENT LEARNING FOR SOFTWARE-BASED SELF-TEST OF PROCESSOR CORES

Jongseon Seo, Hyungmin Cho, Sungkyunkwan University, Suwon, South Korea

KNOWLEDGE IS POWER: A KNOWLEDGE-GUIDED ORACLE-LESS ATTACK ON LOGIC LOCKING

Abir Ahsan Akib, Yuntao Liu, Ankur Srivastava, University of Maryland, College Park, MD

LUTMUL: A PARADIGM SHIFT FROM DSPS TO LUTS FOR EFFICIENT MULTIPLICATION IN FPGA-BASED NEURAL NETWORK COMPUTATION

Yanyue Xie, Zhengang Li, Dana Diaconu, Suranga Handagala, Miriam Leeser, Xue Lin, Northeastern University, Boston, MA

MACO: MODEL-BASED ADAPTIVE CIRCUIT OPTIMIZATION BY TRANSFORMER-BASED BIDIRECTIONAL PREDICTIONS BETWEEN CIRCUIT PARAMETERS AND SPECIFICATIONS

Youngmin Oh, Doyun Kim, Yoon Hyeok Lee, Bosun Hwang, Samsung, Suwon, South Korea

MAM-CIM: DATA RESILIENCE SCHEDULING BASED MULTILEVEL ANALOG MEMORY FOR NEAR SENSOR COMPUTING-IN-MEMORY ARCHITECTURE

Yuhao Liu, Xiaotao Jia, Youguang Zhang, Weisheng Zhao, Beihang University, Beijing, China; Jianyi Yu, Cong Shi, Chongqing University, Chongqing, China; Ciyan Zheng, Guangdong Polytechnic Normal University, Guangzhou, China; Qi Wei, Tsinghua University, Beijing, China; Fei Qiao, Beijing National Research Center for Information Science and Technology, Beijing, China

MINING SIGNAL TEMPORAL LOGIC SPECIFICATIONS FOR HYBRID SYSTEMS

Daniele Nicoletti, Samuele Germiniani, Graziano Pravadelli, University of Verona, Italy

MROB: MULTI-LEVEL REORDER BUFFER DESIGN WITH REDUCED AREA AND POWER

Sai Praneeth Madduri, Mingxuan He, CA; Fangping Liu, Sang Wook Do, Futurewei Technologies, Santa Clara, CA

A MULTI-OBJECTIVE OPTIMIZATION FRAMEWORK OF SPIKING NEURAL NETWORK AND NEUROMORPHIC PROCESSOR

Yuan Li, Zhijie Yang, Xun Xiao, Yuhua Tang, Weixia Xu, National University of Defense Technology, Changsha, China Renzhi Chen, Jingyue Zhao, Lei Wang, Huadong Dai, Defense Innovation Institute, AMS, Beijing, China; Zhenhua Zhu, Tsinghua University, Beijing, China;

WORK-IN-PROGRESS POSTERS (CONTINUED)

MULTI-TERMINAL PATHFINDING WITH CONDITIONAL DENOISING DIFFUSION PROBABILISTIC MODEL
Leonid Popryho, Inna Partin-Vaisband, University of Illinois, Chicago, IL

A NEAR-DATA PROCESSING ARCHITECTURE FOR GNN TRAINING AND INFERENCE ACCELERATION
Haoyang Wang, Shengbing Zhang, Zhao Yang, Meng Zhang, Northwestern Polytechnical University, Xi'an, China

A NEW ITERATIVE METHOD WITH KRYLOV SUBSPACE RECYCLING FOR EFFICIENT PERIODIC AC AND NOISE ANALYSIS
Lingyun Ouyang, Harbin Institute of Technology, Harbin, China; Chao Jin, Shenzhen BTD Technology Co., Ltd., Shenzhen, China; Quan Chen, Southern University of Science and Technology, Shenzhen, China

A NOVEL APPROACH: APPLYING FRACTIONAL FACTORIAL DESIGN METHODOLOGY TO STRESS-MAP, EXPERIMENTAL STUDY FOR STRESS-INDUCED FAILURE (BUG), AND STRESS COVERAGE ASSESSMENT IN POST-SILICON VALIDATION PROCESS
lay wai kong, Glenn Benton Gibbs, Advanced Micro Devices (AMD), Austin, TX

AN OPEN-SOURCE FRAMEWORK FOR AMS MODELING AND VERIFICATION
William Salcedo, Sara Achour, Stanford University, Stanford, CA

PABTG: A PIPELINE ARCHITECTURE FOR BEAVER TRIPLE GENERATION IN SECURE MULTI-PARTY COMPUTATION
Xiaolin Li, Wei Yan, Hongwei Liu, Qinfen Hao, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

PCBENCH: A DATASET FOR PRINTED CIRCUIT BOARD ROUTING
Youbiao He, Jacob Frieden, Hebi Li, Roba Abbajabal, Ge Luo, Forrest Sheng Bao, Iowa State University, Ames, IA

PINN-BASED COMPACT MODEL FOR ON-CHIP SILICON PHOTONIC DEVICES
Yuxiang Fu, Yinyi Liu, Jiaxu Zhang, Jiang Xu, The Hong Kong University of Science and Technology, Guangzhou, China; Tianshu Hou, Shanghai Jiao Tong University, Shanghai, China; Ngai Wong, The University of Hong Kong, Hong Kong;

A PRACTICAL DRAM-BASED ANALOG PIM ARCHITECTURE
Hoon Shin, Rihae Park, Jae W. Lee, Seoul National University, Seoul, South Korea

P-RETI: PHOTONIC TENSOR CORE FOR REAL-TIME LEARNING
Dharanidar Dang, Priyabrata Dash, University of Texas, San Antonia, TX

PROBABILITY MODELING FOR VIA-METAL OPEN CIRCUIT DEFECTS UTILIZING SELF-ALIGNED VIAS PROCESS IN 5NM TECHNOLOGY NODE AND BEYOND
Xiaojing Su, Yajuan Su, Yayi Wei, Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China; Jingjing Li, Guangdong Greater Bay Area Institute of Integrated Circuit and System, Guangzhou, China;

QPULSE: ANSATZ DESIGN ANALYSIS AND ADVANTAGES OF PARAMETERIZED QUANTUM PULSES
Zhiding Liang, Peter Kogge, Yiyu Shi, University of Notre Dame, South Bend, CA; Jinglei Cheng, Purdue University, West Lafayette, IN; Zhixin Song, Georgia Institute of Technology, Atlanta, GA; Hang Ren, University of California, Berkeley, CA; Rui Yang, Kecheng Liu, Tongyang Li, Peking University, Beijing, China; Hanrui Wang, Massachusetts Institute of Technology, Cambridge, MA; Yongshan Ding, Yale University, New Haven, CT;

QUANTUM ERROR CORRECTION CODE DECODING WITH TRANSFERABLE TRANSFORMERS
Hanrui Wang, Kevin Shao, Song Han, Massachusetts Institute of Technology, Cambridge, MA; Pengyu Liu, Carnegie Mellon University, Pittsburgh, PA; Dantong Li, Yongshan Ding, Yale University, New Haven, CT; Jiaqi Gu, Arizona State University, Tempe, AZ;

RES-CIM: RERAM-CACHED SRAM COMPUTE-IN-MEMORY ARCHITECTURE WITH A DIFFERENTIAL SENSING SCHEME ENABLING INTRA-MACRO WEIGHT LOADING
Xiaomeng Wang, Jingyu He, Jiakun Zheng, Fengshi Tian, Fengbin Tu, Tim Kwang-Ting Cheng, Chi-Ying Tsui, Hong Kong University of Science and Technology, Hong Kong, Hong Kong

RETHINKING DRAM FAILURE PREDICTION IN MEMORY RELIABILITY: AN EFFICIENT DEEP IMAGE CLASSIFICATION PERSPECTIVE
Zhishuai Han, Pijia Hao, Inspur, Beijing, China

RETRACT: LOGARITHMIC-DEPTH RECONSTRUCTION OF CONTINUOUS CONTROLLED-NOT LOGIC BLOCK
Enhyeok Jang, Sungwoo Ahn, Won Woo Ro, Yonsei University, Seoul, South Korea

ROBUSTSTATE: BOOSTING FIDELITY OF QUANTUM STATE PREPARATION VIA NOISE-AWARE VARIATIONAL TRAINING
Hanrui Wang, Song Han, Massachusetts Institute of Technology, Cambridge, MA; Yilian Liu, Cornell University, Ithaca, NY; Pengyu Liu, Carnegie Mellon University, Pittsburgh, PA; Jiaqi Gu, Arizona State University, Tempe, AZ; Zirui Li, Shanghai Jiao Tong University, Shanghai, China; Zhiding Liang, Yiyu Shi, University of Notre Dame, South Bend, IN; Jinglei Cheng, Purdue University, West Lafayette, IN; Yongshan Ding, Yale University, New Haven, CT; Xuehai Qian, University of Southern California, Los Angeles, CA; Frederic Chong, University of Chicago, IL;

SEGEN: AUTOMATIC TOPOLOGY GENERATOR OF SEQUENCING ELEMENT
Kyounghun Kang, Wanyeong Jung, Korea Advanced Institute of Science and Technology (KAIST), Yuseong-Gu, South Korea

WORK-IN-PROGRESS POSTERS (CONTINUED)

SHARED-PIM: ENABLING CONCURRENT COMPUTATION AND DATA FLOW FOR FASTER PROCESSING-IN-MEMORY

Ahmed Mamdouh, Dayane Reis, University of South Florida, Tampa, FL; Haoran Geng, Michael Niemier, X. Sharon Hu, University of Notre Dame, South Bend, IN;

SOLVING MAXIMUM FLOWS OF UNDIRECTED GRAPHS BY MINIMIZING S-T EFFECTIVE RESISTANCES OF ELECTRICAL NETWORKS

Ali Aghdaei, Zhuo Feng, Stevens Institute of Technology, Hoboken, NJ; Kuilin Zhang, Michigan Technological University, Houghton, MI

SPULSEGEN: SUCCINCT PULSE GENERATOR ARCHITECTURE MAXIMIZING GATE FIDELITY FOR SUPERCONDUCTING QUANTUM COMPUTERS

Ryosuke Matsuo, Jun Shiomi, Osaka University, Suita, Japan; Kazuhisa Ogawa, Hidehisa Shiomi, Makoto Negoro, Takefumi Miyoshi, QIQB Osaka University, Hachioji-shi, Japan; Michihiro Shintani, Hiromitsu Awano, Takashi Sato, Kyoto University, Kyoto, Japan;

SVDE: SERVERLESS SYSTEM FOR LOW-LATENCY VIDEO ANALYTIC QUERIES USING TREE-BASED REGRESSION

Pingyi Huo, Yi Zheng, Prapti Panigrahi, Kiwan Maeng, Vijaykrishnan Narayanan, Pennsylvania State University, State College, PA; Theodoros Michailidis, Jishen Zhao, University of California, San Diego, CA;

TACPLACE: ULTRAFAST THERMAL-AWARE CHIPLET PLACEMENT UNDER MULTI-POWER MODE USING FEASIBILITY SEEKING

Shan Yu, Haiyang Liu, Xinming Wei, Guojie Luo, Peking University, Beijing, China

A VERIFICATION PLAN TO ASSESS THE QUALITY OF MOBILE TELEPHONY IN BRAZIL

Joel Oliveira, Marcio Kreutz, UFRN, Natal, Brazil

VITSEN: ENABLING VISION TRANSFORMERS AT THE EDGE THROUGH IN/NEAR -SENSOR PROCESSING SCHEMES

Sepehr Tabrizchi, Fatemeh Raei, Arman Roohi, University of Nebraska, Lincoln, NE; Brendan Reidy, Ramtin Zand, University of South Carolina, Columbia, SC; Deniz Najafi, Shaahin Angizi, New Jersey Institute of Technology, Newark, NJ;

WORST CASE RESPONSE TIME ANALYSIS FOR COMPLETELY FAIR SCHEDULING IN LINUX SYSTEMS

Kyonghwan Yoon, EunJin Jeong, Woosuk Kang, Jonghyun Choe, Soonhoi Ha, Seoul National University, Seoul, South Korea

XPMEM: A DESIGN OF BYTE-ADDRESSABLE PERSISTENT MEMORY WITH COMPUTE EXPRESS LINK FOR ADVANCED DATA CENTER APPLICATIONS

Fei Xue, Fred Au, Feng Zhu, Shu Li, Alibaba Group, Sunnyvale, CA; Xun Chen, Mengting Lu, Dengcai Xu, Hao Ding, Kun Wang, Kai Tao, Alibaba Group, Hangzhou, China; Fengguo Zuo, Yubing Wang,; Xiaofeng Zhou, Bin Hou, Xin Xu, Wei Li, Shijie Fan, Liang Zhong, Jing Lv, Xiping Jiang, UnilC, Xian, China;

ZERO-SPACE COST FAULT TOLERANCE FOR TRANSFORMER-BASED LANGUAGE MODELS ON RERAM

Bingbing Li, Zigeng Wang, Shaoyi Huang, Hongwu Peng, Caiwen Ding, University of Connecticut, Storrs, CT; Geng Yuan, University of Georgia, Athens, GA; Payman Behnam, Georgia Institute of Technology, Atlanta, GA; Wujie Wen, North Carolina State University, Raleigh, NC; Hang Liu, Rutgers University, New Brunswick, NJ

LATE BREAKING RESULTS POSTERS

Time: 6:00 PM – 7:00 PM
Session Type: Late Breaking Results Posters
Room: 2nd Floor Lobby

AQFP-AWARE BINARY NEURAL NETWORK ARCHITECTURE SEARCH

Zhengang Li, Xuan Shen, Maoud Zabihi, Yanzhi Wang, Northeastern University, Boston, MA; Geng Yuan, University of Georgia, Athens, GA; Tomoharu Yamauchi, Olivia Chen, Tokyo City University, Tokyo, Japan

A REAL-TIME DIFFUSION-BASED FILTER FOR HUMAN POSE ESTIMATION ON EDGE DEVICES

Chiara Bozzini, Michele Boldo, Enrico Martini, Nicola Bombieri, University of Verona, Italy

CIRCUIT-ALGORITHM CO-DESIGN FOR LEARNABLE AUDIO ANALOG FRONT-END

Jinhai Hu, Zhongyi Zhang, Wang Ling Goh, Nanyang Technological University, Singapore, Singapore; Cong Sheng Leow, University of Michigan, Ann Arbor, MI; Yuan Gao, Institute of Microelectronics, Beijing, China

COULOMB FORCE-BASED ROUTABILITY-DRIVEN PLACEMENT CONSIDERING GLOBAL AND LOCAL CONGESTION

Jihai Meng, Shaohong Weng, Yilu Chen, Zhifeng Lin, Fuzhou University, Fuzhou, China; Zhijie Cai, Jianli Chen, Fudan University, Shanghai, China

DIFFERENTIAL AND MASSIVELY PARALLEL SAMPLING OF SAT FORMULAS

Arash Ardakani, Minwoo Kang, Kevin He, Vighnesh Iyer, Suhong Moon, John Wawrzynek, University of California, Berkeley, CA

EFFICIENT BUILT-IN SELF-TEST FOR MICROFLUIDIC LARGE-SCALE INTEGRATION (MLSI)

Mengchu Li, Yushen Zhang, Tsun-Ming Tseng, Ulf Schlichtmann, Technical University Munich, Germany; Hanchen Gu, Swiss Federal Institute of Technology Zurich, Switzerland; Siyuan Liang, Tsung-Yi Ho, The Chinese University of Hong Kong, Hong Kong; Hudson Gasvoda, Rana Altay, Emre Araci, Santa Clara University, CA

EVALUATION OF HUMAN ACTION QUALITY WITH LINEAR RECURRENT UNITS AND GRAPH ATTENTION NETWORKS ON EMBEDDED SYSTEMS

Filippo Ziche, Nicola Bombieri, University of Verona, Italy

EXTRACTING QNNS FROM NISQ COMPUTERS VIA ENSEMBLE LEARNING

Zhenxiao Fu, Indiana University, Fan Chen, Indiana University, Bloomington, IN

LATE BREAKING RESULTS (CONTINUED)

FAST SYSTEM TECHNOLOGY CO-OPTIMIZATION FRAMEWORK FOR EMERGING TECHNOLOGY BASED ON GRAPH NEURAL NETWORKS

Tianliang Ma, Guangxi Fan, Xuguang Sun, Zhihui Deng, Kain Lu Low, Leilai Shao, Shanghai Jiao Tong University, Shanghai, China

LANGUAGE-LEVEL QOR MODELING FOR HIGH-LEVEL SYNTHESIS

Dimosthenis Masouros, Aggelos Ferikoglou, Sotirios Xydia, Dimitrios Soudris, National Technical University of Athens, Greece; Georgios Zervakis, University of Patras, Greece

LLM-ASSISTED AUTOMATED INCREMENTAL PROOF GENERATION FOR HARDWARE VERIFICATION

Khushboo Qayyum, Muhammad Hassan, Sallar Ahmadi-Pour, Chandan Kumar Jha, Rolf Drechsler, University of Bremen, Germany

MACHINE LEARNING BASED REFERENCE RIPPLE ERROR SUPPRESSION IN SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTERS

Debnath Maiti, Sumukh Bhanushali, Arindam Sanyal, Arizona State University, Tempe, AZ

MAJORITY-INVERTER GRAPH MINIMIZATION BY DESIGN SPACE EXPLORATION

Siang-Yun Lee, Alessandro Tempia Calvino, Giovanni De Micheli, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland; Heinz Riener, Cadence Design Systems, Inc., Bayern, Germany

MIXED-CELL-HEIGHT DETAILED PLACEMENT UNDER MULTI-CELL SPACING CONSTRAINTS

Benchao Zhu, Jianli Chen, Fudan University, Shanghai, China; Zheng Zeng, Fuzhou University, Fuzhou, China

MODERN AUTOMATIC PCB PLACEMENT WITH COMPLEX CONSTRAINTS

Chien-Hao Tsou, Sheng-Yah Lin, Wei-Chen Hung, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

ON THE ONE-KEY PREMISE OF LOGIC LOCKING

Yinghua Hu, Synopsys, Los Angeles, CA; Hari Cherupalli, Synopsys, Sunnyvale, CA; Mike Borza, Synopsys, Ontario, Canada; Deepak Sherlekar, Synopsys, Cupertino, CA

POWER RAIL ROUTING FOR ADVANCED MULTI-LAYERED PRINTED CIRCUIT BOARDS

Wei-Che Tseng, Zong-Ying Cai, Yu-Ping Huang, Yu-Hsiang Lo, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

ROUTABILITY-DRIVEN FPGA MACRO PLACEMENT CONSIDERING COMPLEX CASCADE SHAPE AND REGION CONSTRAINTS

Hao Gu, Jian Gu, Keyu Peng, Jun Yang, Ziran Zhu, Southeast University, Nanjing, China

TRISC: LOW-COST DESIGN OF TRIGONOMETRIC FUNCTIONS WITH QUASI STOCHASTIC COMPUTING

Sercan Aygun, Mehran Shoushtari Moghadam, M. Hassan Najafi, University of Louisiana at Lafayette, LA

WIRING REDUCTION FOR FIELD-COUPLED NANOTECHNOLOGIES

Simon Hofmann, Marcel Walter, Robert Wille, Technical University of Munich, Germany

ENABLING THE ERA OF IMMERSIVE COMPUTING

Time: 8:45 AM – 9:45 AM
Session Type: Keynote
Room: 3007, 3rd Floor

Description: Immersive computing (including virtual, augmented, mixed, and extended reality, metaverse, digital twins, and spatial computing) has the potential to transform most industries and human activities to create a better world for all. Delivering on this potential, however, requires bridging an orders of magnitude gap between the power, performance, and quality-of-experience attributes of current and desirable immersive systems. With a number of conflicting requirements - 100s of milliwatts of power, milliseconds of latency, unbounded compute to realize realistic sensory experiences – no silver bullet is available. Further, the true goodness metric of such systems must measure the subjective human experience within the immersive application. This talk calls for an integrative research agenda that drives codesigned end-to-end systems from hardware to system software stacks to foundation models spanning the end-user device/edge/cloud, with metrics that reflect the immersive human experience, in the context of real immersive applications. I will discuss work pursuing such an approach as part of the IMMERSE Center for Immersive Computing which brings together immersive technologies, applications, and human experience, and in the ILLIXR project based on an open-source end-to-end system to democratize immersive systems research.

Speaker: Sarita Adve, University of Illinois at Urbana-Champaign

AI FOR ANALOG SYNTHESIS

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): AI
Room: 3002, 3rd Floor

Session Chair: Markus Olbrich (Leibniz University Hannover)

Description: AI has become a major underlying method for solving the analog synthesis problem. This session tackles the multi-flavored challenges of analog synthesis using various modern AI techniques. They include hierarchical, multi-agent-based approaches, reinforcement learning, transfer learning, and advanced regression methods. The goals range from exploring Pareto fronts to considering PVT corners in the synthesis.

- **HiMOSS: A Novel High-dimensional Multi-objective Optimization Method via Adaptive Gradient-Based Subspace Sampling for Analog Circuit Sizing**
  Tianchen Gu, Ruiyu Lyu, Zhaori Bi, Changhao Yan, Fan Yang, Dian Zhou, Xuan Zeng, Fudan University, Shanghai, China; Tao Cui, Xin Liu, Chinese Academy of Sciences, Beijing, China; Zaikun Zhang, Hong Kong Polytechnic University, Hong Kong, China;
- **EVDMARL: Efficient Value Decomposition-based Multi-Agent Reinforcement Learning with Domain-Randomization for Complex Analog Circuit Design Migration**
  Handa Sun, Zhaori Bi, Wenning Jiang, Ye Lu, Changhao Yan, Fan Yang, Sheng-Guo Wang, Dian Zhou, Xuan Zeng, Fudan University, Shanghai, China; Wenchuang Hu, Sichuan University, Chengdu, China;
- **Using Probabilistic Model Rollouts to Boost the Sample Efficiency of Reinforcement Learning for Automated Analog Circuit Sizing**
  Mohsen Ahmadzadeh, Georges Gielen, KU Leuven, Belgium;
- **Learn-by-Compare: Analog Performance Prediction using Contrastive Regression with Design Knowledge**
  Zihu Wang, Karthik Somayaji N.S., Peng Li, University of California, Santa Barbara, CA;
- **PVTSizing: A TuRBO-RL-Based Batch-Sampling Optimization Framework for PVT-Robust Analog Circuit Synthesis**
  Zichen Kong, Xiyuan Tang, Yiheng Du, Yibo Lin, Yuan Wang, Peking University, Beijing, China;Wei Shi, University of Texas at Austin, TX;
- **KATO: Knowledge Alignment And Transfer for Transistor Sizing Of Different Design and Technology**
  Wei Xing, Eastern Institute of Technology, Ningbo, China; Weijian Fan, Shenzhen University, Shenzhen, China; Zhuohua Liu, Shenzhen University, Shenzhen, China; Yuan Yao, Yuanqi Hu, Beihang University, Beijing, China

ATTACKS AND DEFENSES AT MICROARCHITECTURE LEVEL AND BEYOND

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): Security
Room: 3008, 3rd Floor

Session Chair: Yinghua Hu (University of Southern California), Farimah Farahmandi (University of Florida)

Description: This session consists of papers on the new development of attacks and defenses at microarchitecture level and above. The first paper establishes a formal method to detect microarchitectural timing side-channel attacks. The second paper proposes hardware fuzzing with information flow tracking to address speculative execution leakages. The third paper presents a framework with deep learning (DL) and frame fusion (2F) for the detection and localization of denial of service (DoS) attack on network-on-chips. The last two papers are on the acceleration of the startup procedure of trusted execution environments (TEEs) and the execution of multi-precision integer arithmetic, respectively.

- **MCU-Wide Timing Side Channels and Their Detection**
  Johannes Muller, RPTU Kaiserslautern-Landau, Germany; Anna Lena Duque Anton, Lucas Deutschmann, Dino Mehmedagic, Mohammad Rahmani Fadiheh, Dominik Stoffel, Wolfgang Kunz, Technische Universitat Kaiserslautern, Germany; Cristiano Rodrigues, Daniel Oliveira Sandro Pinto, Universidade do Minho, Guimaraes, Portugal; Keerthikumara Devarajegowda, Siemens, Neubiberg, Germany;
- **Lost and Found in Speculation: Hybrid Speculative Vulnerability Detection**
  Mohamadreza Rostami, Shaza Zeitouni, Technische Universitat Darmstadt, Germany; Rahul Kande, Chen Chen, Jeyavijayan Rajendran, Texas A&M University, College Station, TX; Pouya Mahmoody, Ahmad-Reza Sadeghi, Technische Universitat Darmstadt, Germany;
- **DL2Fence: Integrating Deep Learning and Frame Fusion for Enhanced Detection and Localization of Refined Denial-of-Service in Large-Scale NoCs**
  Haoyu Wang, Basel Halak, Jianjie Ren, Ahmad Atamli, University of Southampton, United Kingdom;

- **EnTurbo: Accelerate Confidential Serverless Computing via Parallelizing Enclave Startup Procedure**
  Yifan Zhu, Peinan Li, Yunkai Bai, Yubiao Huang, Shiwen Wang, Xingbin Wang, Dan Meng, Rui Hou, Institute of Information Engineering, Chinese Academy of Sciences, Beijing, China;
- **RISC-V Instruction Set Extensions for Multi-Precision Integer Arithmetic**
  Hao Cheng, Georgios Fotiadis, Johann Groszschaedl, Peter Ryan, University of Luxembourg, Esch-sur-Alzette, Luxembourg; Daniel Page, Thinh Pham, University of Bristol, United Kingdom

COMPLEXITY MATTERS: SCHEDULING AND ACCELERATING DATA STRUCTURES IN DNNS

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): AI
Room: 3010, 3rd Floor

Session Chairs: Minah Lee (Georgia Institute of Technology); Amit Trivedi (University of Illinois at Chicago)

Description: In this session, many aspects of accelerating applications with complex data structures and online scheduling of multi-tenant deep learning inference will be discussed. GNNs and deep learning on point clouds require efficient handling data with high sparsity. Furthermore, 3D volume imaging suffers from the poor data locality which can be solved by redesigning the dataflow. For deep learning servers, effectively handling multi-tenancy with online scheduling is highly important that help satisfy the service-level-agreement. Last but not least, a novel Fibonacci quantization method will be presented that improves the energy efficiency with multiplier-free accelerator design.

- **E-DGCN: An Efficient Architecture Design for Accelerating Dynamic Graph Convolutional Network (DGCN) Inference**
  Yingnan Zhao, Jiaqi Yang, Ahmed Louri, George Washington University, Washington, DC; Ke Wang, University of North Carolina, Charlotte, Charlotte, NC;
- **EGMA: Enhancing Data Reuse and Workload Balancing in Message Passing GNN Acceleration via Gram Matrix Optimization**
  Fangzhou Ye, Lingxiang Yin, Amir Ghazizadeh Ahsaei, Hao Zheng, University of Central Florida, Orlando, FL;
- **Fused Sampling and Grouping with Search Space Reduction for Efficient Point Cloud Acceleration**
  Hyunsung Yoon, Pohang University of Science and Technology (POSTECH), Pohang-si, South Korea; Jae-Joon Kim, Seoul National University, Seoul, South Korea;
- **A Software-Hardware Co-design Solution for 3D Inner Structure Reconstruction**
  Xingchen Li, Zhe Zhou, Qilin Zheng, Guangyu Sun, QianKun Wang, Chenhao Xue, Peking University, Beijing, China;
- **A Deep Reinforcement Learning based Online Scheduling Policy for Deep Neural Network Multi-Tenant Multi-Accelerator Systems**
  Francesco Blanco, Enrico Russo, Maurizio Palesi, Davide Patti, Giuseppe Ascia, Vincenzo Catania, University of Catania, Italy;
- **FQP: A Fibonacci Quantization Processor with Multiplication-Free Computing and Topological-Order Routing**
  Xiaolong Yang, Yang Wang, Yubing Qin, Jiachen Wang, Shaojun Wei, Yang Hu, Shouyi YIN, Tsinghua University, Beijing, China

IT'S NOT 8B RETRO-GAMING, IT'S STATE-OF-THE-ART ARCHITECTURES USING QUANTIZATION, SPARSITY, AND COMPRESSION!

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): AI
Room: 3003, 3rd Floor

Session Chairs: Sercan Aygun (University of Louisiana); Charbel Sakr (NVIDIA)

Description: This session presents state-of-the-art work in architecture design focusing on optimization techniques such as quantization, sparsity, pruning, and compression for DNN accelerators. The session begins with a series of presentations on quantization, which is an increasingly popular and energy efficient technique used for deep neural networks (DNNs). The session presents other hot topic techniques such as utilization and optimizing sparsity and pruning, with a focus on the ever-popular transformer attention architecture.

- **Oltron: Algorithm-Hardware Co-design for Outlier-Aware Quantization of LLMs with Inter-/Intra-Layer Adaptation**
  Chenhao Xue, Xun Jiang, Yibo Lin, Guangyu Sun, Peking University, Beijing, China; Chen Zhang, Gao ZhuTianya, Shanghai Jiao Tong University, Shanghai, China;
- **Drift: Leveraging Distribution-based Dynamic Precision Quantization for Efficient Deep Neural Network Acceleration**
  Lian Liu, Yintao He, Ying Wang, State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Zhaohui Xu, Shanghai Tech University, Shanghai, China; Huawei Li, Xiaowei Li, Yinhe Han, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China;
- **MERSIT: A Hardware-Efficient 8-bit Data Format with Enhanced Post-Training Quantization DNN Accuracy**
  Nguyen-Dong Ho, Gyujun Jeong, Cheol-Min Kang, Seungkyu Choi, Ik Joon Chang, Kyung Hee University, Yongin-si, South Korea;
- **DySpMM: From Fix to Dynamic for Sparse Matrix-Matrix Multiplication Accelerators**
  Hongyi Wang, Kai Zhong, Haoyu Zhang, Shulin Zeng, Zhenhua Zhu, Xinhao Yang, Shuang Wang, ; Huazhong Yang, Yu Wang, Tsinghua University, Beijing, China; Guohao Dai, Shanghai Jiao Tong University, Shanghai, China
- **Partially-Structured Transformer Pruning with Patch-Limited XOR-Gate Compression for Stall-Free Sparse-Model Access**
  Younghoon Byun, Youngjoo Lee, Pohang University of Science and Technology (POSTECH), Pohang-si, South Korea;
- **SWAT: Scalable and Efficient Window Attention-based Transformers Acceleration on FPGAs**
  Zhenyu Bai, Huize Li, Pranav Dangi, Tulika Mitra, National University of Singapore, Singapore

VERIFIED VISIONS: NEW FRONTIERS IN FORMAL ASSURANCE

Time: 10:30 AM – 12:00 PM
Session Type: Research Manuscript
Topic Area(s): EDA
Room: 3004, 3rd Floor

Session Chair: Nan Wu (George Washington University)

Description: This section highlights significant progress in formal verification methodologies, ranging from SAT solvers to lemma prediction and safety model checking. The papers surpass traditional techniques by proposing unique binary decision diagrams, scalable solutions based on symbolic approaches and machine learning. If you are keen to discover the future of verification, make sure you don't miss it!

- **RexBDDs: Reduction-on-Edge Complement-and-Swap Binary Decision Diagrams**
  Gianfranco Ciardo, Andrew Miner, Lichuan Deng, Iowa State University, Ames, IA; Junaid Babar, Collins Aerospace, Cedar Rapids, IA;
- **NeuroSelect: Learning to Select Clauses in SAT Solvers**
  Hongduo Liu, Peng Xu, Yuan Pu, Tsung-Yi Ho, Bei Yu, The Chinese University of Hong Kong, Shatin, Hong Kong; Lihao Yin, Huawei, Hui-Ling Zhen, Mingxuan Yuan, Huawei, Hong Kong, Hong Kong;
- **Predicting Lemmas in Generalization of IC3**
  Yuheng Su, Qiusong Yang, Yiwei Ci, Institute of Software, Chinese Academy of Sciences, Beijing, China;
- **Engineering an Efficient Preprocessor for Model Counting**
  Mate Soos, Ethereum Foundation, Berlin, Germany; Kuldeep S Meel, University of Toronto, Toronto, ON, Canada;
- **Symbolic Quick Error Detection by Semantically Equivalent Program Execution**
  Yufeng Li, Qiusong Yang, Yiwei Ci, Enyuan Tian, Institute of Software, Chinese Academy of Sciences, Beijing, China;
- **Formally Verifying Arithmetic Chisel Designs for All Bit Widths at Once**
  Weizhi Feng, Yicheng Liu, David Jansen, Lijun Zhang, Zhilin Wu, Institute of Software, Chinese Academy of Sciences, Beijing, China; Jiaxiang Liu, Shenzhen University, Shenzhen, China

"MEMORY IS THE SCRIBE OF THE SOUL" BE IT VOLATILE OR NOT

Time: 1:30 PM – 3:30 PM
Session Type: Research Manuscript
Topic Area(s): Embedded Systems
Room: 3008, 3rd Floor

Session Chairs: Filippo Carloni (Politecnico di Milano)

Description: It is "still" the memory stupid! would say R. Sites, main or secondary memory, or even non-volatile one. This session presents 8 papers about unprecedented opportunities and challenges related to memory systems: 2 on DRAM/main memory optimization on technological or architectural aspects, 2 papers on prospective Non-Volatile Memory technologies (STT-RAM and RRAM) for enhancing energy consumption on embedded systems, 2 papers on high performance emerging SSDs, one paper on ZRAM optimization for mobile systems and one on In-Memory computing for graphs.

- **Reducing DRAM Latency via In-situ Temperature- and Process-Variation-Aware Timing Detection and Adaption**
  Yuxuan Qin, Chuxiong Lin, Weifeng He, Shanghai Jiao Tong University, Shanghai, China; Shi Xu, Mingche Lai, Zhang Luo, National University of Defense Technology, Changsha, China;
- **TAPMM:A Traffic-Aware Page Mapping Method for Multi-level NUMA Systems**
  Fengkun Dong, Guoqing Xiao, Haotian Wang, Yikun Hu, Kenli Li, Wangdong Yang, Hunan University, Changsha, China;
- **zeroTT: A Two-Step State Transition Avoidance Scheme for MLC STT-RAM**
  Dong Yin, Huizhang Luo, Mingxing Duan, Wangdong Yang, Zhuo Tang, Kenli Li, Hunan University, Changsha, China; Jeff Zhang, Arizona State University, Tempe, AZ;
- **A RRAM-based High Energy-efficient Accelerator Supporting Multimodal Tasks for Virtual Reality Wearable Devices**
  Xin ZHAO, Zhicheng Hu, Zilong Guo, Haodong Fan, Xi Yang, Jing Zhou, Liang Chang, University of Electronic Science and Technology of China, Chengdu, China
- **PipeSSD: A Lock-free Pipelined SSD Firmware Design for Multi-core Architecture**
  Zelin Du, Zixuan Huang, Jin Xue, Kecheng Huang, Zili Shao, The Chinese University of Hong Kong, HongKong, Hong Kong; Shaoqi Li, Tianyu Wang, Shenzhen University, Shenzhen, China;
- **Balloon-ZNS: Constructing High-Capacity and Low-Cost ZNS SSDs with Built-in Compression**
  Yu Wang, Zibin Sun, You Zhou, Changsheng Xie, Fei Wu, Huazhong University of Science and Technology, Wuhan, China; Tao Lu, DapuStor Corporation, Shenzhen, China;
- **ElasticZRAM: Revisiting ZRAM for Swapping on Mobile Devices**
  Wentong Li, Dingcui Yu, Yunpeng Song, Longfei Luo, Liang Shi, East China Normal University, Shanghai, China;
- **A Combined Content Addressable Memory and In-Memory Processing Approach for k-Clique Counting Acceleration**
  Xidi Ma,; Weichen Zhang, Xueyan Wang, Weisheng Zhao, Beihang University, Beijing, China; Tianyang Yu, Bi Wu, Nanjing University of Aeronautics and Astronautics, Nanjing, China; Gang Qu, University of Maryland, College Park, MD

FOUNDATION MODELS FOR EDA AND BEYOND

Time: 1:30 PM – 3:30 PM
Session Type: Research Manuscript
Topic Area(s): AI
Room: 3002, 3rd Floor

Session Chairs: Cong (Callie) Hao (Georgia Institute of Technology); Haoxing "Mark" Ren (NVIDIA)

Description: This session will dive into the intersection of machine learning with EDA and other cutting-edge applications. Attendees will witness how large language models (LLMs) revolutionize tasks from fixing RTL syntax errors, designing operational amplifiers and dramatically cutting down large training times of protein folding with AlphaFold. The session will subsequently explore sustainable benchmarking in accelerator-aware NAS, real-time network traffic analytics, anomaly detection at the edge and ML-driven optimization of physical design parameters for 3D ICs.

- **Automatically Fixing RTL Syntax Errors with Large Language Model**
  YunDa Tsai, NVIDIA, Taipei, Taiwan; Mingjie Liu, Haoxing Ren, NVIDIA, Austin, TX;
- **Artisan: Automated Operational Amplifier Design via Domain-specific Large Language Model**
  Zihao Chen, Jiangli Huang, Yiting Liu, Fan Yang, Li Shang, Xuan Zeng, Fudan University, Shanghai, China; Dian Zhou, The University of Texas at Dallas, TX;
- **ScaleFold: Reducing AlphaFold Initial Training Time to 10 Hours**
  Feiwen Zhu, Rundong Li, Jie Xin, Yifei Song, June Yang, NVIDIA, Beijing, China; Arkadiusz Nowaczynski, Michal Marcinkiewicz, NVIDIA, Warsaw, Poland; Sukru Eryilmaz, NVIDIA, Santa Clara, CA; Michael Andersch, NVIDIA, Berlin, Germany;
- **Data Is All You Need: Finetuning LLMs for Chip Design via an Automated Design-data Augmentation Framework**
  Kaiyan Chang, Ying Wang, Shengwen Liang, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, beijing, China; Kun Wang, Nan Yang, Wenlong Zhu, Cangyuan Li, Yudong Pan, Yiqi Liu, Mengdi Wang, Yinhe Han, Huawei Li, Xiaowei Li, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China;; Dantong Jin, Zhejiang Lab, Hangzhou, China; Zhirong Chen, Zhejiang University, Hangzhou, China; Hao Yan, Shanghai University, Shanghai, China; Yunhao Zhou, Shanghai Jiao Tong University, Shanghai, China; Zhuoliang Zhao, Fudan University, Shanghai, China; Yuan Cheng, Nanjing University, Shanghai, China;
- **Accel-NASBench: Sustainable Benchmarking for Accelerator-Aware NAS**
  Afzal Ahmad, Linfeng Du, Zhiyao Xie, Wei Zhang, Hong Kong University of Science and Technology, Hong Kong, Hong Kong;
- **TrafficHD: Efficient Hyperdimensional Computing for Real-Time Network Traffic Analytics**
  Haodong Lu, Zhiyuan Ma, Xinran Li, Shiyan Bi, Xiaoming He, Kun Wang, Fudan University, Shanghai, China;
- **VARADE: a Variational-based AutoRegressive model for Anomaly Detection on the Edge**
  Alessio Mascolini, Francesco Ponzio, Enrico Macii, Sara Vinco, Santa di Cataldo, Politecnico di Torino, Italy; Sebastiano Gaiardelli, Nicola Dall'Ora, Franco Fummi, University of Verona, , Italy;
- **ML-based Physical Design Parameter Optimization for 3D ICs: From Parameter Selection to Optimization**
  Hao-Hsiang Hsiao, Pruek Vanna-iampikul, Yi-Chen Lu, Sung Kyu Lim, Georgia Institute of Technology, Atlanta, GA

SOME THINGS ARE BEST LEFT IN/NEAR MEMORIES

Time: 1:30 PM – 3:30 PM
Session Type: Research Manuscript
Topic Area(s): Design
Room: 3003, 3rd Floor

Session Chair: Shubham Jain (IBM Thomas J. Watson Research)

Description: In/near-memory innovations for emerging workloads push the boundaries of performance and energy efficiency. The first two papers present accelerators for Open Modification Search and point cloud range search. The next three papers discuss graph mining, including an asynchronous callback interface for triangle counting, a data management system for regular path queries, and learned indexes for variable-length keys. The sixth paper presents hardware-managed DRAM caching using a Gaussian mixture model for CXL-enabled memory expansion. Finally, the last two papers introduce adaptive resource allocation for SmartNICs and a framework for optimizing PIM execution sequences using parallel data preparation.

- **Efficient Open Modification Spectral Library Searching in High-Dimensional Space with Multi-Level-Cell Memory**
  Keming Fan, Sumukh Pinge, ; Tajana Rosing, University of California, San Diego, CA; Wei-Chen Chen, H.-S. Philip Wong, Stanford University, Stanford, CA
- **CAMPER: Exploring the Potential of Content Addressable Memory for 3D Point Cloud Efficient Range Search**
  Jiapei Zheng, Lizhou Wu, Yutong Su, Jingyi Wang, Zhangcheng Huang, Chixiao Chen, Qi Liu, Fudan University, Shanghai, China;
- **Sting: Near-storage accelerator framework for scalable triangle counting and beyond**
  Seongyoung Kang, University of California, Irvine, Irvine, CA; Sang-Woo Jun, University of California, Irvine, Irvine, CA;
- **Accelerating Regular Path Queries over Graph Database with Processing-in-Memory**
  Ruoyan Ma, Shengan Zheng, Guifeng Wang, Jin Pu, Yifan Hua, ; Linpeng Huang, Shanghai Jiao Tong University, Shanghai, China; Wentao Wang, Peking University, Beijing, China
- **LIVAK: A High-Performance In-Memory Learned Index for Variable-Length Keys**
  Zhaole Chu, Zhou Zhang, Peiquan Jin, Xiaoliang Wang, Yongping Luo, University of Science and Technology of China, Hefei, China; Xujian Zhao, Southwest University of Science and Technology of China, Mianyang, China;
- **ICGMM: CXL-enabled Memory Expansion with Intelligent Caching Using Gaussian Mixture Model**
  Hanqiu Chen, Cong Hao, Georgia Institute of Technology, Atlanta, GA; Yitu Wang, Yiran Chen, Duke University, Durham, NC; Vitorio Cargnini, Mohammadreza Soltaniyeh, Dongyang Li, Gongjin Sun, Pradeep Subedi, Andrew Chang, Samsung Semiconductor, San Jose, CA;
- **TIGA: Towards Efficient Near Data Processing in SmartNICs-based Disaggregated Memory Systems**
  Zhuohui Duan, Wuhan, China; Zelin Yu, Haikun Liu, Xiaofei Liao, Hai Jin, Shijie Zheng, Sihan Wu, Huazhong University of Science and Technology, Wuhan, China;
- **Execution Sequence Optimization for Processing In-Memory using Parallel Data Preparation**
  Muhammad Rashedul Haq Rashed, Sven Thijssen, Dominic Simon, Rickard Ewetz, University of Central Florida, Orlando, FL; Sumit Jha, Florida International University, Miami, FL

SPEEDY: INNOVATIVE STRATEGIES FOR SYNTHESIS, PLACEMENT, DRC, AND YIELD

Time: 1:30 PM – 3:30 PM
Session Type: Research Manuscript
Topic Area(s): EDA
Room: 3004, 3rd Floor

Session Chairs: Yu-Guang Chen (National Central University), Vidya Chhabria (Arizona State University)

Description: Take this journey with us through the amazing world of physical design and learn about novel algorithms to tame the challenges arising from the growing complexities in technology scaling and advanced packaging! Topics include faster and more accurate yield prediction, standard cell design co-optimization, package-level GPU-accelerated design rule checker, performance-improving placement-aware logic resynthesis and datapath-aware mixed-size placement approaches, advanced techniques for synthesizing cutting-edge CFET-based standard cells with much lower area and routing resources, and a highly efficient placement algorithm for significantly boosting performance of ultra-low power adiabatic quantum-flux parametron-based logic designs for high-performance computing applications.

- **Every Failure Is A Lesson: Utilizing All Failure Samples To Deliver Tuning-Free Efficient Yield Evaluation**
  Wei Xing, Lei He, Eastern Institute of Technology, Ningbo, China; Yanfang Liu, Beihang University, Beijing, China; Weijian Fan, Shenzhen University, Shenzhen, China;
- **Unleashing the Potential of AQFP Logic Placement via Entanglement Entropy and Projection**
  Yinuo Bai, Enxin Yi, Zhou Jin, China University of Petroleum-Beijing, Beijing, China; Wei Xing, Eastern Institute of Technology, Ningbo, China; Bei Yu, The Chinese University of Hong Kong, Shatin, Hong Kong;
- **SkyPlace: A New Mixed-size Placement Framework using Modularity-based Clustering and SDP Relaxation**
  Jaekyung Im, Seokhyeong Kang, Pohang University of Science and Technology (POSTECH), Pohang-si, South Korea;
- **Optimal Transistor Folding and Placement for Synthesizing Standard Cells of Complementary FET Technology**
  Suwan Kim, Taewhan Kim, Seoul National University, Seoul, South Korea;
- **PPA-Relevant Clustering-Driven Placement for Large-Scale VLSI Designs**
  Andrew Kahng, Sayak Kundu, Bodhisatta Pramanik, University of California, San Diego, CA Seokhyeong Kang, Kyungjun Min, Seonghyeon Park, Pohang University of Science and Technology (POSTECH), Pohang, South Korea;
- **Lesyn: Placement-aware Logic Resynthesis for Non-Integer Multiple-Cell-Height Designs**
  Yuan Pu, Fangzhou Liu, Yu Zhang, Zhuolun He Bei Yu, The Chinese University of Hong Kong, Hong Kong; Kai-Yuan Chao, Huawei, Hong Kong, Hong Kong; Yibo Lin, Peking University, Beijing, China;
- **PDRC: Package Design Rule Checking via GPU-Accelerated Geometric Intersection Algorithms for Non-Manhattan Geometry**
  Jiaxi Jiang, Lancheng Zou, Wenqian Zhao, Zhuolun He, Tinghuan Chen, Bei Yu, The Chinese University of Hong Kong, Shatin, Hong Kong;
- **Mixed-Size 3D Analytical Placement with Heterogeneous Technology Nodes**
  Yan-Jen Chen, Cheng-Hsiu Hsieh, Po-Han Su, Shao-Hsiang Chen, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

ADDITIONAL MEETINGS

HACK at DAC

Sunday, June 23 & Monday, June 24
8:00 am – 6:00 pm
Level 2 Lobby

Young Fellows Kick-Off and All-Day Activities

Sunday, June 23
9:00 am – 6:00 pm
Room 3018

DAC Early Career Workshop

Sunday, June 23
9:00 am – 5:00 pm
Room 3016

Needham Presentation

Sunday, June 23
5:00 pm – 6:00 pm
Room 3002

TODAES Editorial Board Meeting

Monday, June 24
10:00 am – 1:00 pm
Room 3000

ACM SIGDA Annual Volunteer & Sponsored Conference Meeting

Monday, June 24
2:00 pm – 6:00 pm
Room 3000

IEEE CEDA Distinguished Lecture Luncheon

Tuesday, June 25
12:00 pm - 1:30 pm
Room 3018

HACK at DAC Awards

Tuesday, June 25
3:30 pm – 5:00 pm
Room 3000

Birds of a Feather

Tuesday, June 25
6:30 pm – 9:30 pm
Room 3001

Young Fellows Posters

Tuesday, June 25
7:00 pm - 9:00 pm
Level 2 Lobby

PhD Forum & University Demo

Tuesday, June 25
7:00 pm – 9:00 pm
Level 2 Lobby

System Design Contest Awards

Wednesday, June 26
3:30 pm – 5:00 pm
Room 3000

Young Fellows Closing Ceremony

Thursday, June 27
3:30 pm - 5:30 pm
Room 3018

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