SECURITY/PRIVACY • INTELLECTUAL PROPERTY (IP) • EMBEDDED SYSTEMS AND SOFTWARE (ESS) • ARTIFICIAL INTELLIGENCE/MACHINE LEARNING (AI/ML) • DESIGN SERVICES

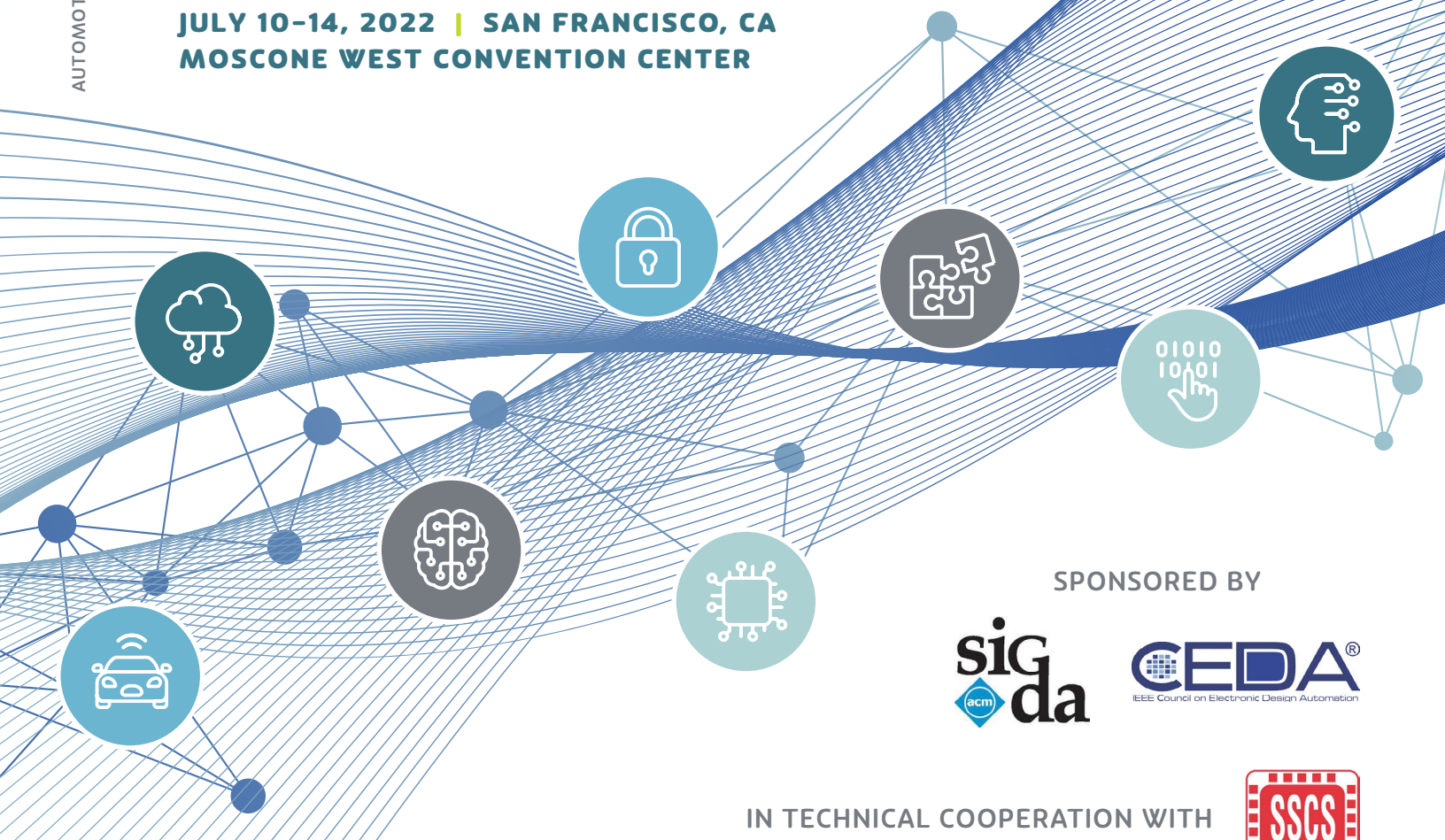
AUTOMOTIVE • ELECTRONIC DESIGN AUTOMATION (EDA) • DESIGN ON CLOUD •

CONFERENCE PROGRAM & EXHIBITS GUIDE

59 DESIGN AUTOMATION CONFERENCE

FROM CHIPS TO SYSTEMS — LEARN TODAY, CREATE TOMORROW

JULY 10–14, 2022 | SAN FRANCISCO, CA
MOSCONE WEST CONVENTION CENTER



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IN TECHNICAL COOPERATION WITH SSCS

#59DAC

DATE 23

DESIGN, AUTOMATION AND TEST IN EUROPE

THE EUROPEAN EVENT FOR ELECTRONIC SYSTEM DESIGN & TEST

17 – 19 APRIL 2023
ANTWERP, BE

FLANDERS MEETING & CONVENTIONS CENTER ANTWERP (FMCCA)

FOR ITS 2023 EDITION, DATE PRESENTS ITSELF IN A RENEWED FORMAT:

After three years of online editions due to COVID-19, DATE 2023 focusses on interaction, reinforcing and rebuilding links in the community. Rather than spreading the attendance throughout an entire week, we condense DATE to three days – and make them count! DATE 2023 will focus on what conferences are for: meeting, discussing and exchanging.

HIGHLIGHTS:

- The 26th edition of the main European event bringing together designers and design automation users, researchers and vendors as well as specialists in the design, test and manufacturing of electronic circuits and systems hardware and software
- Keynote speakers from academia and industry
- Research paper presentations
- Late breaking results paper presentations
- Special days on emerging topics:
  - Human AI-Interaction
  - Personalised Medicine
- Special initiative on Autonomous Systems Design
- Focus sessions on a broad range of hot academic and industrial topics
- Unplugged sessions
- Embedded tutorials
- Half-day workshops on specialised and novel topics
- **Young People Programme** (PhD Forum / Careers Fair - Industry / Careers Fair - Academia / Student Teams Fair / University Fair)
- Multi-Partner Project sessions

WWW.DATE-CONFERENCE.COM

FOLLOW US ON

edaa european design and automation association

sigda

CEDA IEEE Council on Electronic Design Automation

semi

ESDA Electronic System Design Alliance

TECHNICAL CO-SPONSORS

IEEE Computer Society Test Technology Technical Council [TTTC]
IEEE Solid-State Circuits Society [SSCS]
IEEE Computer Society [IEEE CS]

WELCOME!

Dear Colleagues,

Welcome to the 59th Design Automation Conference!

Thanks for joining us in San Francisco, home to the oldest Chinatown in North America, and whose famous fog has a name (Karl) with its own Twitter handle, and where denim jeans were invented. Of course, San Francisco can also be described using terms like technology innovation, R&D, and disruption. Plenty of that will be on display this week at Moscone West Convention Center. We will be hosting #59DAC face-to-face, without the mediating technology that has kept us separated over the last couple of years!

After 59 years, #59DAC continues to be the leading conference in design and design automation from IC chips to systems and continues to evolve with new energy and innovation. With the help of literally hundreds of volunteers, the DAC executive committee has assembled a top-tier research program, highly regarded practitioners' forums, and a widely represented exhibition. We have four very interesting and informative #59DAC keynotes as well as excellent technical SkyTalk and TechTalk presentations. Besides the robust technical program, social breaks are scheduled to give you ample time to relax, have a drink and some snacks, meet new acquaintances, and collaborate.

Besides the more than 100 total sessions related to core EDA and IP topic areas, #59DAC features topics in areas such as:

- 40 sessions in Design (from heterogeneous SoCs, architectures, circuits, to emerging technologies)
- 15 sessions in Embedded Software and Systems (from IoT, CPS, embedded memory, and edge computing)
- 35 sessions in AI/Machine learning (software and system designs of neural network accelerators as well as the application of AI/machine learning techniques to advancing electronic design automation)
- 10 sessions in Cloud (design in cloud, ML, orchestration, device life cycle management)

As always, you will find much action and excitement on the exhibition floor. With our twice-daily coffee breaks on the exhibition floor, you will be able to visit more than 130 exhibitors and our popular DAC Pavilion. Please try to check out these other cool areas and activities:

- Design Infrastructure Alley
- Design-on-Cloud Pavilion
- Open Source Central
- Poster Gladiator Battles

One new addition for this DAC is our hands-on design-on-cloud training sessions being hosted Tuesday and Wednesday in the Design-on-Cloud Theater.

Don't forget to download DAC's mobile app! It not only makes it easier for you to manage your schedule and activities at the show but also navigate the three floors of Moscone West.

I hope I will get to talk to many of you in person during #59DAC. Our tag line is "Learn today and create tomorrow." We believe there is plenty to learn at #59DAC and we look forward to seeing what you create tomorrow!

The great writer Mark Twain once said, "I have always been rather better treated in San Francisco than I actually deserved." We hope to treat you equally well at #59DAC.

Enjoy #59DAC!

Rob Oshana

ROB OSHANA

59th DAC General Chair

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CONFERENCE INFORMATION

Exhibit Hours

Exhibit Halls on Level 1 and Level 2

Monday
Exhibits Open: 10:00 am – 6:00 pm

Tuesday
Exhibits Open: 10:00 am – 6:00 pm

Wednesday
Exhibits Open: 10:00 am – 6:00 pm

Registration Hours

Location: Level 1 Lobby

Saturday	12:00 pm – 6:00 pm
Sunday	7:00 am – 7:00 pm
Monday	7:00 am – 7:00 pm
Tuesday	8:00 am – 6:00 pm
Wednesday	8:00 am – 6:00 pm
Thursday	8:00 am – 3:00 pm

Online Proceedings

To view the proceedings, download the zip file using the following link –
https://reports.smithbucklin.com/dac/59Dac.zip

Stay Connected

Enjoy complimentary WiFi at DAC:

Network Name: **DAC2022**
Password: **59DAC2022**

'Birds of a Feather' Meetings

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal, non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather" (BOF).

All BOF Meetings are held at Moscone Center West, Tuesday July 12, from 7:00 pm – 8:30 pm in rooms 3000, 3001, 3002, 3003, 3004, 3005. To arrange a BOF meeting, please email DAC Show Management at **info@dac.com**.

First Aid Room

Moscone West First Aid Office is located on the 1st floor near the Howard Street entrance (behind registration).
Phone: 415-974-4159

REPORT ALL MEDICAL EMERGENCIES IMMEDIATELY

To report a medical emergency, call 511 on any white House Phone, or on a call phone dial 415-974-4159

DAC Mobile App

Download the official DAC59 Mobile App for the most up to date schedule, speaker changes, and general announcements!

To download the mobile app, visit https://app.dac.com

Or scan the QR code below:

DAC NETWORKING OPPORTUNITIES

Networking Receptions

Sunday, July 10th

Welcome Reception
6:00 pm – 7:30 pm | Level 3 Lobby

Monday, July 11th

Engineering Track Poster Session and Networking Reception
5:00 pm – 6:00 pm | Exhibit Hall Level 2

SYNOPSYS® Silicon to Software™

Women in Tech Reception
6:00 pm – 7:30 pm | Level 2 Lobby

Tuesday, July 12th

Engineering Track Poster Session and Networking Reception
5:00 pm – 6:00 pm | Exhibit Hall Level 2

Networking Reception & Work-in-Progress Poster Session
6:00 pm – 7:00 pm | Level 2 Lobby

TPC Reception (Invitation Only)
5:30 pm – 6:00 pm | Level 2 Lobby

Wednesday, July 13th

Engineering Track Poster Session and Networking Reception
5:00 pm – 6:00 pm | Exhibit Hall Level 2

Networking Reception & Work-in-Progress and Late Breaking Results Poster Session
6:00 pm – 7:00 pm | Level 2 Lobby

KEYNOTE PRESENTATIONS Room 3008

MARK PAPERMASTER

CTO and EVP Technology and Engineering, AMD

Advancing EDA Through the Power of AI and High-performance Computing

Monday, July 11, 2022 | 8:45 am – 9:45 am

Technologies to enable truly intelligent systems are now accelerating the EDA evolution. We are at an inflection point where AI algorithms have a huge impact, in both EDA and in CAD with the realization of digital twins and generative design. Moreover, many more high performance and acerated compute solutions are available, both on-prem and cloud-based, to speed design and analysis. AMD CTO & EVP of Technology and Engineering Mark Papermaster will explore new compute approaches to help the industry overcome challenges and address time, cost and complexity barriers that impede innovation and future success.

Mark Papermaster is Chief Technology Officer and Executive Vice President of Technology and Engineering responsible for Advanced Micro Devices' (AMD) technical direction and product development including microprocessor design, I/O and memory, system-on-chip (SOC) methodology, and advanced research. He led the re-design of engineering processes at AMD and the development of the award-winning "Zen" high-performance x86 CPU family, high-performance GPUs and the company's modular design approach, Infinity Architecture. He also oversees Information Technology (IT) that delivers AMD's compute infrastructure and services.

His more than 35 years of engineering experience includes significant leadership roles managing the development of a wide range of products, from microprocessors to mobile devices and high-performance servers. Before joining AMD in October 2011 as Chief Technology Officer and Senior Vice President, Papermaster was the leader of Cisco's Silicon Engineering Group, Apple Senior Vice President of Devices Hardware Engineering for iPod and iPhone and held multiple IBM roles in technology and server development.

Papermaster received his bachelor's degree from the University of Texas at Austin and master's degree from the University of Vermont, both in Electrical Engineering. He is a long-term member of the University of Texas Cockrell School of Engineering Advisory Board, Olin College Presidents Council, the Juvenile Diabetes Research Foundation, CTO Forum Advisory Board, IEEE Industry Advisory Board, and most recently the Global Semiconductor Alliance Board of Directors.

ANIRUDH DEVGAN, PHD

President and Chief Executive Officer, Cadence Design System, Inc.

Computational Software and the Future of Intelligent Electronic System Design

Tuesday, July 12, 2022 | 8:40 am – 9:45 am

The EDA industry has driven orders of magnitude productivity, scalability, and quality improvements. We are now in the era of AI, where it impacts our daily lives, the products we depend on, and how we design those electronics systems. But adding AI technology to existing tools and flows is only the first step in this journey. We can now deliver optimization across multiple dimensions, intersecting domains, and historically loosely coupled components of systems. These new dimensions are transforming the industry, resulting in multiple orders of magnitude improvements in system design productivity with optimization results never before possible or even conceived.

Biography: Dr. Anirudh Devgan has served as President and CEO of Cadence Design Systems, Inc. since December 2021, and has been a member of the Board of Directors since August 2021. He served as President of the company from 2017 to 2021, overseeing all business groups, research and development, sales, field engineering and customer support, strategy, marketing, mergers and acquisitions, business development, and IT. Prior to becoming President, he was Executive Vice President and General Manager of the Digital & Signoff and System Verification groups at Cadence. Prior to joining Cadence in 2012, Dr. Devgan was General Manager and Corporate Vice President of the Custom Design Business Unit at Magma Design Automation. Previous roles include management and technical positions at IBM, where he received numerous awards including the IBM Outstanding Innovation Award. Dr. Devgan is an IEEE Fellow, has written numerous research papers, and holds several patents. Dr. Devgan received a Bachelor of Technology degree in electrical engineering from the Indian Institute of Technology, Delhi, and MS and PhD degrees in electrical and computer engineering from Carnegie Mellon University.

KEYNOTE PRESENTATIONS *continued*

STEVE TEIG

CEO, PERCEIVE

Machine Learning for Real: Why Principles, Efficiency, and Ubiquity Matter

Wednesday, July 13, 2022 | 8:40 am – 9:45 am

Marc Andreessen famously opined that “software is eating the world.” Recently, various people have suggested that AI is eating software. Deep learning seems to touch every discipline these days, but behind its startling magic tricks, it is surprisingly primitive. Most deep learning today requires vast data centers whose power consumption burdens an already overstressed planet. Add in the latency and loss of privacy, and it is clear that society would benefit from gadgets that do not require connection to the cloud to be “smart”. Even more concerning, however, is the strong dependence of today’s deep learning on folklore: on recipes and anecdotes, rather than scientific principles and explanatory mathematics. Instead, we can develop rigorous, scalable machine learning guided by information theory to create models that are predictive, power-efficient, and cost-effective.

Biography: Steve Teig is a visionary technologist and serial entrepreneur whose work has impacted industries ranging from software and semiconductors to biotechnology and machine learning. He has served as founder and/or CTO for multiple companies, and his contributions have been recognized with numerous awards, including an Edison Award and a World Technology Award. He is an inventor on 365 U.S. patents across multiple disciplines, and a well-regarded speaker who has delivered keynotes and invited lectures at conferences and universities around the world. He currently serves as CEO of Perceive, which provides the Ergo® edge AI processor, a purpose-built chip to enable large neural networks to run within power-constrained devices for a wide range of applications.

GIOVANNI DE MICHELI

Director of the Institute of Electrical Engineering and of the Integrated Systems Centre, EPFL

Strange Loops in Design Technology

Thursday, July 14, 2022 | 8:40 am – 9:45 am

Strong ties link the evolution of computing, semiconductor technology and design automation. The unprecedented growth of system solutions, services and markets are due to the cross-fertilization of various areas of science and technology, where often new problems motivate new solutions in a circular way. Design automation has led engineers in sailing through uncharted territories, in shaping our digital society on robust grounds and in providing us with a launchpad for the future.

Biography: Giovanni De Micheli is a research scientist in electronics and computer science. He is credited for the invention of the Network on Chip design automation paradigm and for the creation of algorithms and design tools for Electronic Design Automation. He is Professor and Director of the Integrated Systems Laboratory at EPFL Lausanne, Switzerland. Previously, he was Professor of Electrical Engineering at Stanford University. Prof. De Micheli is a Fellow of ACM , AAAS and IEEE, a member of the Academia Europaea and an International Honorary member of the American Academy of Arts and Sciences. He is the recipient of several awards from IEEE, ACM and EDAA. His current research interests include several aspects of EDA, such as synthesis for emerging technologies. He is also interested in heterogeneous platform design including electrical components and biosensors, as well as in data processing of biomedical information. He was the DAC chair in 2000.

SKYTALK PRESENTATIONS DAC Pavilion (Booth #2260)

TERESA MCLAURIN

Fellow and Senior Director of Design for Test (DFT) Architechure at Arm

Building Resiliency – The Next Imperative in Design

Tuesday, July 12, 2022 | 1:00 pm – 1:45 pm

Innovations in the world of design work toward ensuring that technology continues to deliver smaller and faster. This has included new methods that are beyond shrinking the transistors as Moore's Law is slowing down. Testing and Design for Test must keep up to ensure that the designs created are fully testable to prevent costly test escapes. In addition to technology, areas that require intermittent testing such as automotive and large data centers to support the cloud must also be addressed. Teresa will illustrate how some of the trends of test may be examples of how resiliency on silicon will evolve in the industry.

Teresa McLaurin is a Fellow and Senior Director of DFT Architecture at Arm in Austin Texas. Before working at Arm she worked at Motorola and Western Digital in test engineering, product engineering management and DFT. She is a senior member of the IEEE and has contributed to the IEEE 1500 and 1838 standards. She was the recipient of the 2020 TTTC Bob Madge Innovation Award and the 2021 GSA Rising Women of influence Award.

SANDEEP MEHNDIRATTA

Vice President, Enterprise Go-To-Market, Synopsys

It's Getting Cloudy Out There

Wednesday, July 13, 2022 | 1:00 pm – 1:45 pm

Cloud is everywhere – for chip design, companies large, medium, and small are evaluating their options in using high-performance computing (HPC) infrastructure to accelerate and differentiate their designs. In this session, we will discuss the drivers and challenges of moving EDA workloads to the cloud and how leading design teams are maximizing the benefits of moving to the cloud.

Sandeep Mehndiratta is Vice President, Enterprise Go-To-Market, at Synopsys, where he is responsible for optimizing GTM motion for Synopsys products and solutions, including driving the cloud strategy for the company's EDA solutions. Sandeep has over 20 years of experience in technology across multiple disciplines. He has a passion for translating vision into execution, leveraging his hands-on experience in sales engineering, business operations and product management, helping companies build-up and scale go-to-market operations, business processes and high-performing teams.

TECHTALK PRESENTATIONS

AKI FUJIMURA

Chairman and CEO of D2S, Inc.

Is Curvy Design an Opportunity or a Dream?

Monday, July 11, 2022 | 11:30 am – 12:30 pm

The semiconductor manufacturing community is ready for the first time in 40 years to enable a wholesale change in what future chips could look like by manufacturing curvilinear features. But most of the chip design community doesn't know that and this talk is about bridging that awareness from manufacturing to the design community. The entire chip design infrastructure is based on the Manhattan assumption. In my previous life in EDA, I had something to do with that, so I know this very well. I also know this is not going to change any time soon. At the same time, though, is there any doubt that a curvilinear "curvy" chip, if magically made possible, would be smaller, faster, and use less power? Of course not. The shortest distance between two points is a straight line. And the least resistive path is a smoothly curved path, not a series of 90 degree turns. Another thing we know from my current life in software for semiconductor manufacturing: a target shape that is easier to manufacture is more reliably manufacturable. And 90-degree turns are not manufacturable, but smooth curvilinear turns are. Curvy designs would yield better, decrease chip size and perform more consistently. There's an opportunity to take advantage of what semiconductor manufacturing has enabled for the first time in 40 years. In this talk, I'll provide a baseline education of how photomasks and wafers are manufactured then summarize the changes in semiconductor manufacturing that enable curvy designs. My goal is to explain why manufacturing is no longer a barrier to curvy design and spark the imagination of the EDA and design community.

Aki is the chairman and CEO of D2S, Inc. D2S is the managing company sponsor of the eBeam Initiative and a member of the Center for Deep Learning in Electronics Manufacturing. Previously, Aki served as CTO at Cadence Design Systems. Aki returned to Cadence for the second time through the acquisition of Simplex Solutions where he was President/COO and inside board member. He was also an inside board member and VP at Pure Software. Simplex and Pure both IPO'd during his tenure. He was a founding member of Tangent Systems in 1984, which was subsequently acquired by Cadence Design Systems in 1989.

Aki serves on the governing council of the Electronic System Design Alliance, a SEMI technical community. Aki was on the board of HLDS, RTime, Bristol S7, and Coverity, Inc., all of which were successfully acquired.

Aki received his BS/MS in Electrical Engineering from MIT.

BOB BRENNAN

Vice President of Customer Solutions Engineering for Intel Foundry Services

Open Architectures to Accelerate Industry Growth

Tuesday, July 12, 2022 | 11:30 am – 12:30 pm

There is an exponential growth in demand for workload specific compute in artificial intelligence (both training and inference), network and storage acceleration, 5G/6G edge servers, media acceleration, high performance compute (ex. Vector processing), graphics, and gaming. The industry is facing many architectural challenges to improve cost, performance, power, security, etc. to meet this demand. The solution will require a broad alignment around standardized open architectures from the ISA to the SoC level, alignment of the IP supplier ecosystem, cooperation in standards, new EDA tools, and support from foundries and packaging suppliers.

This talk will highlight some of the recent progress in the industry, and a call to collaborate on enabling and supporting these new architectures.

Biography: Bob Brennan is Vice President of Customer Solutions Engineering for Intel Foundry Services at Intel Corporation. He is responsible for leading the delivery of end-to-end design solutions to help IFS customers use Intel's portfolio of unique IPs and design technology in their product designs. This responsibility covers the entire design life cycle for customers, from customer design architecture to the strategic selection of Intel IP to platform enablement, as well as design services support for SoC integration including validation and debug support. Bob also has the honor of serving as a board member for RISC-V International. In his previous role, Bob served as Vice President of Emerging Memory & System at Micron, where he managed product, design, and engineering teams to accelerate the delivery of new designs on new technologies. Before that, Bob served as Senior Vice President of Memory Solutions Lab at Samsung, where he established an Enterprise SSD product line, delivered Samsung's first revenue software product while continuing an active role in architecture development. Prior to these roles, Bob spent 22 years at Intel serving in various senior technical positions, including Server Architecture, Laptop Architecture, Mobile SoC Architecture, and CPU Core Design, Verification and Architecture.

TECHTALK PRESENTATIONS *continued*

MARILYN WOLF

Professor of Engineering and Director of the School of Computing at the University of Nebraska Lincoln

Co-Design for Edge Intelligence: Perception, Control, Computing

Wednesday, July 13, 2022 | 11:30 am – 12:30 pm

Autonomous vehicles combine machine learning-based perception with planning and control. Co-design introduces the opportunity for new types of optimizations for perception that range across accuracy, execution time, and power consumption. The requirements on embedded computer vision for autonomy include accuracy, latency, and power consumption. These requirements interact---for example, long latencies can interfere with control performance. This talk will explore the use of co-design to create highly capable and efficient autonomous systems.

Marilyn C. Wolf has enabled a new generation of researchers to conceptualize, build, and validate modern embedded computing systems through influential textbooks, high-impact conferences, and mentoring graduate students. These computers embedded within physical objects power our world in transportation, healthcare, and many other disciplines. Wolf wrote one of the first textbooks in the field, Computers as Components: Principles of Embedded Computing System Design, as well as High-Performance Embedded Computing: Applications in Cyber-Physical Systems and Mobile Computing, which is geared specifically to graduate courses. She has helped to create many of the technical meetings and technical publications in the field, including Embedded Systems Week and the journal Design Automation for Embedded Systems, providing essential forums for graduate students.

An IEEE Fellow, Wolf is the Elmer E. Koch Professor of Engineering and Director of the School of Computing at the University of Nebraska–Lincoln, Lincoln, NE, USA.

IN MEMORIAM

Dr. Thomas W. Williams (1943-2022)

Tom was born in Rochester, New York on August 3, 1943. His father was Walter A. Williams and his mother was Mary Borysewski, both of Rochester and have predeceased him. He is survived by Jonathan Phillip Davis, son, and 2 granddaughters, London Reese Davis and Holland Faith Davis of Park City, Utah, and his wife Candace Merrill-Williams of Canmore, AB, Canada.

Tom was a leader in the test community, with a long and distinguished career at IBM and Synopsys. Tom was known for his fundamental contributions to scan technology, and participated in many different ways in the engineering community and IEEE. Of the many industry events he was part of, Tom would definitely want to mention his DFT Workshop in Vail, Colorado. Tom has an extensive list of publications, keynotes and awards and is remembered for his unique presentation style. His slides were sometimes flipped and ended with beautiful pictures, taken by him, of wildlife and nature. He received the Kaufman Award in 2018

Every interaction with Tom was a joyful experience for all. Tom has livened up many of our lives. Even a brief interaction with Tom has been memorable to many. Tom's love for life showed in his photography and his love for wine and Italian food. His emails were memorable for the mis-spelled words, as he had a disability that would show until the end of life.

Tom Williams will be missed. He was a unique personality and a great soul. His mustache brought out his personality in all the pictures we have of him.

Wojtek Maly (1946 - 2022)

Prof. Wojtek Maly spent 35 years at Carnegie Mellon University conducting a truly pioneering research in several areas ranging from statistical design of integrated circuits (now called Design for Manufacturability) to built-in self test and test based diagnosis. He also proposed a breakthrough approach to the 3-dimensional IC system design and, in the last 10 years, 3-dimensional transistor architectures (VeSFET) and circuits (VeSTIC). His groundbreaking research has had a tremendous and lasting impact on the EDA field and semiconductor industry in general.

Dhiraj Pradhan

Dhiraj Pradhan, Fellow of ACM, IEEE and the Japan Society of Promotion of Science, also recipient of many other awards including the German Humboldt Prize, was a renowned professor and researcher who served on the faculty at the University of Bristol, Texas A&M University, and the University of Massachusetts, Amherst, and as visiting professor at many major universities around the world. He is widely recognized for his many original contributions to reliable and fault-tolerant systems, VLSI testing, and EDA.

Suzanne Graham (1951-2022)

Suzanne Graham (Sue) was a mother, grandmother, and part of a caring community of friends-that-are-family. She passed away in her sleep at her Portland, Oregon home on March 5, 2022 after a brave battle with breast cancer which originally began back in 2000. She is survived by her children, Caitlin and Gavin Bristol, and her two grandchildren, Isla and Owen Naar.

DAC AWARDS AND SCHOLARSHIPS

2022 DAC Under-40 Innovators Award

Luca Amaru

Yanjing Li

Hesham Omran

Guangyu Sun

2022 Marie R. Pistilli Women in Engineering Achievement Award

Michelle Clancy, Cayenne Global

P.O. Pistilli Undergraduate Scholarship for Advancement in Computer Science and Electrical Engineering

Janiya Richardson

IEEE/CEDA

2022 IEEE Leon K. Kirchmayer Graduate Teaching Award

Marilyn C. Wolf, School of Computing, University of Nebraska-Lincoln

IEEE Robert N. Noyce Medal

Jason Jingsheng Cong, UCLA

IEEE Computer Society Edward J. McCluskey Technical Achievement Award

Yiran Chen, Duke University

IEEE Computer Society Harry H. Goode Memorial Award

Subhasish Mitra, Stanford University

IEEE CEDA Outstanding Service Award

Harry Foster, Siemens EDA

IEEE Fellow

Iris Bahar, Colorado School of Mines

Samarjit Chakraborty, UNC Chapel Hill

Luca Daniel, Massachusetts Institute of Technology

Puneet Gupta, UCLA

Mahesh Iyer, Intel Corporation

Yu Wang, Tsinghua University

IEEE/ACM A Richard Newton Technical Impact Award in Electronic Design Automation

Jacob K. White, MIT

Kenneth S. Kundert, Cadence

Ricardo Telichevesky, Cadence

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems Donald O. Pederson Best Paper Award

Kyungwook Chang, School of Electrical and Computer Engineering, Georgia Institute of Technology

Bon Woong Ku, Synopsys

Sung Kyu Lim, School of Electrical and Computer Engineering, Georgia Institute of Technology

2022 Phil Kaufman Award for Distinguished Contributions to ESD

Dr. Anirudh Devgan, Cadence Design Systems

DAC AWARDS AND SCHOLARSHIPS *continued*

ACM/SIGDA

2022 ACM Transactions on Design Automation of Electronic Systems Best Paper and Rookie Author of the Year Award:

Yukui Luo, **Shijin Duan**, and **Xiaolin Xu**, FPGAPRO: A Defense Framework Against Crosstalk-Induced Secret Leakage in FPGA, vol. 27, no. 3, May 2022, Article No. 24, pp. 1-31

Best Paper Award for ACM Transactions on Reconfigurable Technology and Systems for the Year 2022:

Alexandra Kourfali and **Dirk Stroobandt**, In-Circuit Debugging with Dynamic Reconfiguration of FPGA Interconnects, vol. 13, no. 1, Mar. 2020, Article No. 5, pp. 1-29

ACM SIGDA Distinguished Service Award

Harry Foster, Siemens EDA

Vijaykrishnan Narayanan, The Pennsylvania State University

ACM SIGDA Outstanding New Faculty Award

Yingyan (Celine) Lin, Rice University

ACM FELLOW

Sharon Hu, University of Notre Dame

Hai (Helen) Li, Duke University

David Z. Pan, University of Texas at Austin

Tajana Simunic Rosing, University of California, San Diego

Mark M. Tehranipoor, University of Florida

ACM SIGDA Outstanding PH.D. Dissertation Award

Ganapati Bhat, Arizona State University

SIGDA Pioneering Achievement Award

Rob A. Rutenbar, University of Pittsburgh

SIGDA Service Award

Jeff Goeders, Brigham Young University

Yiyu Shi, University of Notre Dame

Tsung-Wei Huang, University of Utah

Cheng Zhuo, Zhejiang University

System Design Contest

1st Place: TBD

2nd Place: TBD

3rd Place: TBD

DAC PAVILION SCHEDULE

Booth #2260

Monday, July 11

10:15 am – 11:15 am

ANALYST REVIEW: SEMICONDUCTOR MARKET TRENDS: TYING IT ALL TOGETHER FOR THE BIG PICTURE

Speakers: Richard Wawrzyniak, Principal Market Analyst: ASIC & SoC, Semico Research Corp.

11:30 am – 12:30 pm

TECHTALK: IS CURVY DESIGN AN OPPORTUNITY OR A DREAM?

Speaker: Aki Fujimura, Chairman and CEO of D2S, Inc.

2:00 pm – 2:45 pm

PANEL: IS DEMOCRATIZATION OF CHIP DESIGN ALREADY HAPPENING?

Moderator: Nitin Dahad, Editor, embedded.com

Panelists: Alain Dargelas, VP Engineering, RapidSilicon; Rob Mains, Chips Alliance; Rick O'Connor, CEO, Open Hardware Group; Mohamed Kassem, CTO eFabless; Vic Kilkarni, Chief Strategy Officer, Silicon Integrative Initiative, Inc.

3:00 pm – 3:45 pm

PANEL: THOSE DARN BUGS! WHEN WILL THEY BE EXTERMINATED FOR GOOD?

Moderator: Brian Bailey, Semiconductor Engineering

Panelists: Ashish Darbari, Axiomise; Mark Glasser, Cerebras; Ty Garibay, Mythic; Larry Lapides, Imperas

4:30 pm – 5:30 pm

GLADIATOR ARENA POSTER BATTLE

Tuesday, July 12

10:15 am – 11:15 am

ANALYST REVIEW: THE STATE OF EDA: A VIEW FROM WALL STREET

Speakers: Jay Vleeschhouwer Griffin Securities

11:30 am – 12:30 pm

TECHTALK: OPEN ARCHITECTURES TO ACCELERATE INDUSTRY GROWTH

Speaker: Bob Brennan, Vice President of Customer Solutions Engineering, Intel Foundry Systems

1:00 pm – 1:45 pm

SKYTALK: BUILDING RESILIENCY – THE NEXT IMPERATIVE IN DESIGN

Speaker: Teresa McLaurin, Fellow and Senior Director of Design for Test (DFT) Architecture, Arm

2:00 pm – 2:45 pm

WOMEN IN ENGINEERING: TRANSFORMING THE INNOVATION PARADIGM

Moderator: Ann Steffora Mutschler, Executive Editor/EDA, Semiconductor Engineering

Panelists: Radhika Shankar, Group Director, Synopsys; Geeta Pyne, Chief Enterprise Architect, Intuit; Sherry Hess, Cadence; Raji Arasu, CTO, Autodesk

3:00 pm – 3:45 pm

PANEL: WHAT CAN EDA AND THE ELECTRONICS ECOSYSTEM DO FOR GREENER ELECTRONICS TO SAVE THE PLANET?

Moderator: Frank Schirrmesiter, Cadence Design Systems, Inc.

Panelists: Dipti Vachani, Arm; Jennifer Huffstetler, Intel; David Pellerin, Amazon Web Services; Dharmesh Jani, Meta; Vojin Zivojnovic, Aggios

4:30 pm – 5:30 pm

GLADIATOR ARENA POSTER BATTLE

Wednesday, July 13

11:15 am

2022 IEEE LEON K. KIRCHMAYER GRADUATE TEACHING AWARD PRESENTATION

11:30 am – 12:30 pm

TECHTALK: CO-DESIGN FOR EDGE INTELLIGENCE: PERCEPTION, CONTROL, COMPUTING

Speaker: Marilyn Wolf, Professor of Engineering and Director of the School of Computing at the University of Nebraska Lincoln

1:00 pm – 1:45 pm

SKYTALK: IT'S GETTING CLOUDY OUT THERE

Speaker: Sandeep Mehndiratta, Vice President, Enterprise Go-To-Marketer, Synopsys

2:00 pm – 2:45 pm

PANEL: BESPOKE SILICON – TAILOR-MADE FOR MAXIMUM PERFORMANCE

Moderator: John Lee, Ansys

Panelists: Prashant Varshney, Microsoft; Mathew Kaipanatu, Google; Kam Kittrell, Cadence Design Systems, Inc.

3:00 pm – 3:45 pm

PANEL: HOW ROBUST IS YOUR HARDWARE SECURITY PROGRAM?

Moderator: Andreas Kuehlmann, Tortuga Logic

Panelists: Debra Delise, Analog Devices; Jason Fung, Intel; Joe Tostenrude, Microsoft; Vivek Vedula, Arm Ltd.

4:30 pm – 5:30 pm

GLADIATOR ARENA POSTER BATTLE

WORKSHOP: SOFTWARE STACK DESIGN FOR QUANTUM COMPUTING

Time: 8:00 AM – 12:00 PM
Room: 3004, Level 3
Topics Area(s): Quantum Computing, Design

Organizer(s): Xin-Chuan Wu, Intel; Greg Byrd, North Carolina State University; Yongshan Ding, Yale University; Shavindra Premarante, Intel; Albert Schmitz, Intel

Quantum computing promises to solve certain computational problems that are intractable even using the most powerful classical high-performance computers. Quantum algorithms have the potential to revolutionize areas such as quantum chemistry, cryptography, and optimization. However, current quantum machines in the Noisy Intermediate-Scale Quantum (NISQ) era are too small for large applications. There is a shortage of researchers and engineers to close the resource gap between quantum algorithms and real devices available today. This workshop aims to grow the community of quantum computing researchers and quantum software engineers to develop practical quantum systems and applications.

In this workshop, we will introduce the basic concept of quantum computation to enable researchers to explore the area and discuss the design challenges and research directions in the current NISQ era. Next, we will cover the near-term research in quantum error mitigation techniques, as well as introduce hybrid quantum-classical variational algorithms that are the most promising applications to demonstrate quantum speedup for NISQ devices. Finally, we will introduce the architecture design and the implementation of the quantum compiler.

This workshop will be highly interactive. Participants will install the Intel Quantum framework and have hands-on experience in running the example applications. We will also demonstrate how a hybrid quantum-classical program is written, compiled, and executed on the platform.

WORKSHOP: 3RD ROAD4NN WORKSHOP: RESEARCH OPEN AUTOMATIC DESIGN FOR NEURAL NETWORKS

Time: 8:00 AM – 5:00 PM
Room: 3000, Level 3
Topics Area(s): AI, EDA

Organizer(s): Zhenman Fang, Simon Fraser University, Burnaby, Canada; Yanzhi Wang, Northeastern University, Boston, MA; Zhe Chen, University of California, Los Angeles, CA

In the past decade, machine learning, especially neural network based deep learning, has achieved an amazing success. Various neural networks, such as CNNs, RNNs, LSTMs, Transformers, BERT, GNNs, and SNNs, have been deployed for various industrial applications like image classification, speech recognition, and automated control. On one hand, there is a very fast algorithm evolvement of neural network models, almost every week there is a new model from a major academic and/or industry institute. On the other hand, all major industry giants have been developing and/or deploying specialized hardware platforms to accelerate the performance and energy-efficiency of neural networks across the cloud and edge devices. This include Nvidia GPU, Intel Nervana/Habana/Loihi ASICs, Xilinx FPGA, Google TPU, Microsoft Brainwave, Amazon Inferentia, to name just a few. However, there is a significant gap between the fast algorithm evolvement and staggering hardware development, hence calling for broader participation in software-hardware co-design from both academia and industry.

In this workshop, we focus on the research open automatic design for neural networks, a holistic open source approach to general-purpose computer systems broadly inspired by neural networks. More specifically, we discuss full stack open source infrastructure support to develop and deploy novel neural networks, including novel algorithms and applications, hardware architectures and emerging devices, as well as programming, system, and tool support. We plan to bring together academic and industry experts to share their experience, discuss challenges they face as well as potential focus areas for the community.

WORKSHOP: 7TH WORKSHOP ON APPROXIMATE COMPUTING

Time: 8:00 AM – 5:00 PM
Room: 3007, Level 3
Topics Area(s): Design

Organizer(s): Alexandra Kourfali, University of Stuttgart, Stuttgart, Germany; Alessandro Savino, Politecnico di Torino, Torino, Italy; Benjamin Carrion Schaefer, The University of Texas at Dallas, Richardson, TX

Nowadays, Approximate Computing (AxC) represents a novel design paradigm for building modern systems, which offer trade-offs between efficiency in terms of performance, power consumption, hardware area, execution timing, and the quality/exactness of the outcomes. AxC is based on the intuitive observation that, while performing exact computation requires a high amount of computational resources, allowing a selective approximation or an occasional relaxation of the specification may provide significant gains in energy efficiency while still providing acceptable results. Suitable solutions will not be fully realized in a single layer only. Therefore, applying AxC in different layers of hardware, architecture, software, and algorithms should be investigated. Moreover, while the hidden cost of AxC is a reduction of an application's inherent resiliency to errors, AxC has also recently been demonstrated to be effective in safety-critical applications. This workshop (seventh edition after successful ones at Paderborn'15, ESWEEK'16, ETS'18, DATE'19, DAC'20, ICCAD21) aims at exploring the AxC continuum, making room for the exploration of methodologies able to exploit effective and real systems that can inspire application in many recent application domains such as machine learning, safety, and security. Moreover, this year's edition will also be organized in conjunction with a Marie Curie-funded research program (APROPOS).

WORKSHOP: CAD FOR HARDWARE SECURITY WORKSHOP (CAD4SEC)

Time: 8:00 AM – 5:00 PM
Room: 3006, Level 3
Topics Area(s): Security

Organizer(s): Farimah Farahmandi, Mark Tehranipoor, University of Florida, Gainesville, FL

Security vulnerabilities in hardware designs are catastrophic since it is almost impossible to patch them once they are fabricated. Recent studies have shown many vulnerabilities in SoC hardware implementations, including side-channel leakage, information leakage, access control violations, malicious functionality, etc. These attacks can effectively bypass the built-in security mechanisms and put chips or systems at risk. Ensuring the security of hardware designs is challenging due to their huge complexity, aggressive time to markets, and the variety of attacks. Since designers may not have sufficient knowledge about the security requirements due to the huge complexity of SoC designs and their attack surfaces, it is difficult to manually analyze the design implementation in different levels of abstractions. Therefore, the semiconductor industry and system integrators are looking for a set of metrics, reusable security solutions, and automatic computer-aided design (CAD) tools to aid analysis, identifying, root-causing, and mitigating SoC security problems.

Vulnerabilities in SoCs are due to design mistakes, lack of security understandings, design transformations, various attack surfaces, and malicious intents. Further, exiting CAD tools are used in SoC design flow can introduce additional vulnerabilities in the SoCs unintentionally. For example, some design practices/choices may make the design vulnerable to timing and power side-channel leakage. Not only will these vulnerabilities move from one level of abstraction to another, but unique vulnerabilities can also be introduced during design transformations. For example, an RTL design with power side-channel issues can suffer from access control issues when it is synthesized to gate-level, and design-for-debug infrastructure will be inserted. Therefore, it is essential to have automatic CAD solutions to be able to analyze the security of SoCs in a comprehensive manner, in all levels of abstractions, and against all existing threats (e.g., fault-injection, side-channel, and hardware Trojan attacks). CAD tools should be able to access the security of the design in the pre-silicon stage and suggest possible countermeasures while still, it is possible to modify the design and address the potential vulnerabilities.

CAD4Sec will invite experts from industry (like Synopsys, Cadence, Google, Analog Devices, Siemens EDA), academia, and government (like DARPA, NAVY, AFRL) to shed light on the need for and the recent progress on the development of automatic security CAD solutions in all levels of abstractions (i.e., C/C++, RTL, gate-level, and layout). The workshop will include demos on the recent CAD for security tools to detect various vulnerabilities. There will be technical talks and a panel consisting of experts in the field to talk about the road map for CAD for security development.

The CAD4Sec workshop will cover the following:

- CAD for power/timing side-channel vulnerability assessment
- CAD for electromagnetic radiation vulnerability assessment
- CAD for fault-injection vulnerability evaluation
- CAD for automatic security property generation
- CAD for security equivalence checking between different design abstractions
- CAD for security equivalence checking between different SoCs
- CAD for Optical/microprobing/nanoprobing probing for assurance
- CAD for (Anti-)Reverse engineering and physical attacks
- CAD for FPGA Bitstream protection and vulnerabilities
- CAD for Trojans detection and prevention

WORKSHOP: IN-MEMORY ARCHITECTURES AND COMPUTING APPLICATIONS WORKSHOP (IMACAW)

Time: 8:00 AM – 5:00 PM
Room: 3005, Level 3
Topics Area(s): AI, Design

Organizer(s): Nima TaheriNejad, Technische Universität Wien, Vienna, Austria; Alberto Bosio, Lyon Institute of Nanotechnology, Lyon, France; Deliang Fan, Arizona State University, Tempe, AZ

Today's computer architectures and device technologies used to manufacture them are facing major challenges, rendering them incapable of delivering the performances required by complex applications such as Big-Data processing and Artificial Intelligence (AI). The iMACAW workshop aims at providing a forum to discuss In-Memory-Computing (as an alternative architecture) and its potential applications. To this end, we take a cross-technology approach covering State-of-the-Art (SoA) works that use SRAM, DRAM, FLASH, RRAM, PCM, MRAM, and FeFET as their memory technology. The workshop also aims at reinforcing the In-Memory-Computing (IMC) community and at offering a holistic vision of this emerging computing paradigm to the design automation communities. This workshop will provide an opportunity for the audience to listen to invited speakers who are pioneers of the field, learn from them, ask questions, and interact with them. Open submission contributors also get the opportunity to share their knowledge, most-recent work, and their work in progress with the community, interact with them, and receive feedback.

WORKSHOP: RAGE – THE 1ST INTERNATIONAL WORKSHOP ON REAL-TIME AND INTELLIGENT EDGE COMPUTING

Time: 8:00 AM – 5:00 PM
Room: 3002, Level 3
Topics Area(s): AI/Embedded Systems

Organizer(s): Daniel Casini, Scuola Superiore Sant'Anna, Pisa, Italy; Dakshina Dasari, Robert Bosch GmbH, Renningen, Germany; Matthias Becker, KTH Royal Institute of Technology, Stockholm, Sweden

The edge computing paradigm is becoming increasingly popular as it facilitates real-time computation, reduces energy consumption and carbon footprint, and fosters security and privacy preservation by processing the data closer to its origins, thereby drastically reducing the amount of data sent to the cloud. On the application side, there is a growing interest in using edge computing as a key pillar to support decentralized artificial intelligence by implementing federated learning and adaptive deep learning inference at the edge. However, many edge applications tightly interact with the surrounding environment and are required to deliver a result (e.g., perform actuation or send a message through a 5G network) within a predefined deadline. Therefore, a key requirement in edge computing is the need to be predictable across the edge-to-cloud continuum while also efficiently utilizing the system resources.

However, meeting the above requirements is non-trivial. Modern edge devices can be very diverse (from hand-held devices to large in-premise servers) and can include complex embedded platforms with multiple heterogeneous cores and hardware accelerators such as GPUs, TPUs, and FPGAs. This complexity introduces considerable challenges when trying to guarantee timing requirements of real-time applications: for example, due to scheduling policies implemented by the hardware accelerators (often hidden by vendors), or due to the memory contention experienced by the cores when accessing concurrently main memory. Secondly, the network transmission time (TSN over Ethernet to 5G links) can lead to variability in the end-to-end latencies incurred by edge applications.

Furthermore, the operating system (OS) also plays a crucial role in enabling the edge computing paradigm, but quite often at the price of increasing the difficulty in deriving timing guarantees: for example, think of a complex deep neural network that needs to leverage a Linux-based OS (which is far more complicated than a real-time operating system), since it makes available all the software stacks (e.g., TensorRT) and device drivers to interact with NVIDIA GPUs.

The complexity of the problem is further increased by the usage of middleware frameworks, which simplify the development of applications, but at the cost of introducing additional scheduling policies that add to those implemented by the underlying operating system, hindering predictability. Some relevant examples are ROS, in the context of robotics, TensorFlow for artificial intelligence, TensorRT for efficient deep neural network inference on GPUs, and others. Virtualization technologies are also becoming crucial in implementing the edge paradigm, but again, at the expense of creating a more complex operating environment, where guaranteeing temporal properties is really challenging. These problems are common to many application domains, including cyber-physical systems, future-generation autonomous-driving applications, robotics, Industry 4.0, smart-buildings, and more.

In this workshop, we solicit the submission of work-in-progress papers. Workshop topics include, but are not limited to:

- Real-time edge computing
- QoS mechanisms for temporal isolation
- Mechanisms for end-to-end latency guarantees in the edge-to-cloud continuum
- Predictability in middleware frameworks (ROS, TensorFlow, TensorRT, and more)
- Real-time edge computing use cases
- Real-time network protocols for edge computing
- Real-time distributed artificial intelligence
- Predictable and efficient parallel applications
- Timing predictability for artificial intelligence

WORKSHOP: WORKSHOP ON DESIGN AUTOMATION FOR THE CERTIFICATION OF AUTONOMOUS SYSTEMS (DAC-AS)

Time: 8:00 AM – 5:00 PM
Room: 3003, Level 3
Topics Area(s): AI, Autonomous Systems

Organizer(s): Zamira Daw, Timothy Wang, Raytheon Technologies, Berkeley, CA; Pierluigi Nuzzo, University of Southern California, Los Angeles, CA; Isaac Amundson, Collins Aerospace, Minneapolis, MN

The integration of increasingly richer software functions into complex, autonomous systems raises concerns about their trustworthiness with respect to safety, security, and other dependability measures. While its definition can vary by industry, trust is often achieved through a process of certification, in which the residual risks associated with the deployment of a system in a specified environment are evaluated and deemed acceptable. However, current certification processes heavily depend on human judgment. A certification or regulatory authority is expected to determine whether a system is trustworthy by analyzing large amounts of evidence about a product and its development.

Such a lengthy process can result in superficial, incomplete, biased, and costly evaluations. The situation is exacerbated by the emergence of artificial intelligence (AI) and machine learning (ML) solutions in consumer applications, which has revolutionized the industry, enabling features that were not possible with traditional methods. Safety-critical and mission-critical domains such as the aerospace, automotive, medical, and nuclear domains are eager to leverage AI-enabled software in their products as well, but there is a lack of consensus on how to ensure that such software is trustworthy. Certification standards such as DO-178C and IEC 62304 do not provide explicit guidance for certifying software containing AI components. Without a clear pathway to certification, the risks in developing AI-enabled high-integrity systems remains a barrier to adoption.

This workshop investigates the potential of design automation to mitigate these risks. Design automation concepts can help streamline the certification process by aiding the construction of comprehensive and defensible arguments for system correctness, for example, in the form of assurance cases. On the other hand, new design methods and tools can facilitate the analysis of AI enhanced components and the generation of evidence to support the correctness claims. The workshop aims to bring together the certification, design automation, and artificial intelligence communities in both academia and industry to discuss promising methods for increasing trust in autonomous systems. The one-day workshop will consist of the following three sessions:

1. A set of invited talks covering: (i) argument-based certification, an emerging approach in the medical and aerospace domains that allow developers to provide their own means of regulatory compliance, as defined by structured arguments; (ii) design and verification methods that can increase assurance of AI-enabled systems. Invited talks will be given by established researchers both from academia and industry.

2. An academic and industrial panel on “Certification of AI-Enabled Systems” to foster closer interactions with the audience.

3. A set of working sessions, including parallel breakout sessions, where the participants will discuss, in groups, structured arguments for the assurance of AI-enabled components. A plenary session will follow, to summarize and share with all the participants the outcomes of the breakout sessions.

Meant as a highly interactive workshop, DAC-AS will help the certification, design automation, and artificial intelligence communities to share their experience, identify potential focus areas, and foster collaborations that could lead to breakthroughs in the certification of autonomous systems.

WORKSHOP: THE FIFTH INTERNATIONAL WORKSHOP ON DESIGN AUTOMATION FOR CYBER-PHYSICAL SYSTEMS (DACPS)

Time: 1:30 PM – 5:00 PM
Room: 3004, Level 3
Topics Area(s): Embedded Systems

Organizer(s): Chung-Wei Lin, National Taiwan University, Taipei, Taiwan; Xun Jiao, Villanova University, Villanova, PA; Mohammad Al Faruque, University of California, Irvine, CA; Shiyan Hu, University of Southampton, Southampton, United Kingdom; Xin Li, Duke University, Durham, NC; Qi Zhu, Northwestern University, Evanston, IL

Cyber-Physical Systems (CPS) are characterized by the strong interactions between cyber and physical components. CPS system examples include automotive and transportation systems, avionics systems, smart home, building and community, smart battery and energy systems, robotic systems, cyber-physical biochip, wearable devices, and so on. Due to the deeply complex intertwining among different components, CPS designs pose fundamental challenges in multiple aspects such as safety, performance, security, reliability, fault tolerance, extensibility, and energy consumption. Developing innovative design automation techniques, algorithms and tools is imperative to address the unique challenges in CPS design and operation, such as the fast increase of system scale and complexity, the close interactions with dynamic physical environment and human activities, the significant uncertainties in sensor readings, the employment of distributed architectural platforms, and the tight resource and timing constraints. This workshop will present the state-of-the-art research results on the topic of design automation for CPS/IoT systems, introduce practical challenges and promising solutions in various industry sectors, and stimulate CAD researchers to participate in the interdisciplinary CPS/IoT research.

VISIONARY TALK: EDA TO POWER THROUGH SEMICONDUCTOR CYCLES

Time: 5:00 PM – 6:00 PM
Room: 3001, Level 3

Historically the semiconductor industry goes through a boom-bust cycle every 3-4 years. Despite the chip shortage headlines, Wall Street is increasingly skeptical about the longevity of the current semiconductor boom cycle. The outlook is still bright, but there are dark clouds on the horizon. If the chip shortage turns into a glut, will a downturn affect the EDA industry? Our answer is no. In this presentation, I will walk you through reasons why EDA industry will power through semiconductor cycles and emerge on the other side stronger.

Speaker: Charles Shi, Principal, Research Analyst, Needham & Company LLC

OPENING SESSION, AWARDS PRESENTATION & MONDAY KEYNOTE

Time: 8:45 AM – 9:45 AM
Room: 3008-3012, Level 3

ADVANCING EDA THROUGH THE POWER OF AI AND HIGH-PERFORMANCE COMPUTING

Mark Papermaster, AMD, Austin, TX

Technologies to enable truly intelligent systems are now accelerating the EDA evolution. We are at an inflection point where AI algorithms have a huge impact, in both EDA and in CAD with the realization of digital twins and generative design. Moreover, many more high performance and acerated compute solutions are available, both on-prem and cloud-based, to speed design and analysis. AMD CTO & EVP of Technology and Engineering Mark Papermaster will explore new compute approaches to help the industry overcome challenges and address time, cost and complexity barriers that impede innovation and future success.

Monday Sessions

SEMICONDUCTOR MARKET TRENDS: TYING IT ALL TOGETHER FOR THE BIG PICTURE

Time: 10:15 AM – 11:15 AM
Room: DAC Pavilion, Level 2 Exhibit Hall
Event Type: Analyst Presentation
Topics Area(s): AI, EDA, IP

In this discussion we will review the Semiconductor industry and ecosystem in terms of market size, trends, forecasts, R&D investment, and fab capacity. In addition, we will look at the trends and forecasts for the SoC, IP, and AI markets along with ASIC and SoC design starts.

Speaker: Richard Wawrzyniak, Semico Research Corp., Oconto, WA

DON'T TIKTOK

Time: 10:30 AM – 12:00 PM
Room: 2008, Level 2
Event Type: Engineering Tracks
Topics Area(s): Back-End Design

Chair/Co-Chair: Patricia Fong, Marvell Semiconductor

SPEEDING-UP DESIGN CLOSURE WITH ACCURATE STATISTICAL TIMING MACRO-MODELS

Chaitanya Peddawad, IBM, Bengaluru, India; Steven Meyers, IBM, Overland Park, KS

ADVANCED COMPREHENSIVE DEBUG METHODOLOGY TO ACCELERATE SOC TIMING CONVERGENCE

Anmol Khatri, Intel Technology India Pvt. Ltd, Bayana, India

TIMING ANALYTICS AND REPORTING: FROM DESIGN START TO FINISH

Charles Schmitter, Charles Gates, Chris Cavitt, IBM, Poughkeepsie, NY; Kerim Kalafala, IBM, Hopewell Junction, NY; SheshaShayee Raghunathan, IBM, Bengaluru, India; Deb Dean, IBM, Cary, NC

QUICK & EFFICIENT EXTRACTION OF LIBRARY PESSIMISM: ENABLER FOR FASTER HOLD TIMING CLOSURE

Sriraj Chellappan, Texas Instruments, Nasik, India; Shuchita Kaila, Texas Instruments, Bengaluru, India; Gokul Sabada, Texas Instruments, Karnataka, India; Tapsir Shaikh, Texas Instruments, Pune, India; Malav Shah, Texas Instruments, Bengaluru, India

PERFORMANCE-DRIVEN MULTI-BIT OPTIMIZATION FLOW

Chaeyoung Jang, Samsung Electronics, Yongin-si, South Korea; Insub Shin, Bonghyun Lee, Samsung Electronics, Hwaseong, South Korea

I/O CONSTRAINTS OPTIMIZATION

Lekshmi C, Shivangi Gupta, Sourav Saha, Rakshit Bazaz, Intel Technology India Pvt. Ltd, Bengaluru, India; Anmol Khatri, Intel Technology India Pvt. Ltd, Bayana, India; Raj Yadav, Intel Technology India Pvt. Ltd, Ahmedabad, India

EMBEDDED SYSTEMS AND SOFTWARE

Time: 10:30 AM – 12:00 PM
Room: 2012, Level 2
Event Type: Engineering Tracks
Topics Area(s): Embedded Systems, RISC-V

Chair/Co-Chair: Chirag Dhruv, AMD

AUTOMATIC CHECKPOINT SUPPORT IN THE DEVICE MODELING LANGUAGE (DML)

Jakob Engblom, Intel Corporation, Stockholm, Sweden; Erik Carstensen, Intel Corporation, Göteborg, Sweden

OPTIMIZATION OF HOT/COLD SEPARATION ALGORITHM COMPUTATION FOR SSD

GyeongMin Nam, Chanha Kim, Samsung Electronics, Hwasung, South Korea; SeungRyong Jang, Samsung Electronics, Hwaseong-si, South Korea

RAPID EMBEDDED SOFTWARE VERIFICATION THROUGH HARDWARE-ACCELERATED, PARALLEL SYSTEMC TLM SIMULATION – A RISC-V EXAMPLE

Lukas Jünger, Rainer Leupers, RWTH Aachen University, Aachen, Germany

DESIGN VERIFICATION FOR VIRTUAL PROTOTYPE EXPLOITING UVM

Myeongjin Kim, Samsung Electronics, Hwaseong-si, South Korea; Byunghoon Lee, Jaeyeong Jeon, Seungik Ha, Jinbeom Kim, ; Jongseong Park, Kyungsu Kang, JaeWoo Im, Samsung Electronics, Hwaseong, South Korea

SPECIFICATION DRIVEN AUTOMATION OF SOC RTL INTEGRATION USING IP-XACT

Shimoli Shinde, Texas Instruments, Bengaluru, India; Gaurav Varshney, Texas Instruments, Bengaluru, India

BRINGING INTERNET OF THINGS AND ARTIFICIAL INTELLIGENCE TOGETHER - BUT IS IT TRUSTWORTHY?

Michael Karner, VIRTUAL VEHICLE Research GmbH, Graz, Austria; Peter Moertl, VIRTUAL VEHICLE Research GmbH, Klagenfurt-Villach, Austria; Ramiro Samano-Robles, CISTER Research Center, Aveiro, Portugal

TAMING THE VALIDATION DRAGON WITH FORMAL AND STATIC VERIFICATION

Time: 10:30 AM – 12:00 PM
Room: 2010, Level 2
Event Type: Engineering Tracks
Topics Area(s): Front-End Design

Chair/Co-Chair: Vikas Sachdeva, RealIntent

With validation's seemingly infinite appetite to consume engineering resources, formal and static methods have become a crucial tool to enable closure of complex designs. This session covers the still-growing role of formal and static methods in various areas of front-end design: microarchitecture and functional correctness; clocks, resets, and metastability; and analog/mixed-signal verification.

NOVEL APPROACH TO EARLY DETECTION OF METASTABILITY RELATED ISSUES

Alessandro Locardi, Andrea Lopinto, STMicroelectronics, Milan, Italy

VERIFYING REGISTER MAPS WITH JASPERGOLD: HOW FORMAL COMPARES TO UVM

Davide Sanalitro, STMicroelectronics, Cornaredo, Italy; Edoardo Bollea, STMicroelectronics, Castelletto, Italy; Maurizio Martina, Guido Masera, Polytechnic University of Turin, Turin, Italy

EFFICIENT FUNCTIONAL SIGN OFF BY AUTOMATIC ASSERTION GENERATION FOR RTL BUILDING BLOCKS

Toshiya Uenishi, Renesas Electronics Corporation, Kodaira-shi, Japan; Yasushi Ozaki, Renesas Electronics Corporation, Tokyo, Japan; Andrew Guyler, Real Intent Inc, Portland, OR; Roger Hughes, Real Intent Inc, Sunnyvale, CA; Kazutaka Kanda, Real Intent Inc, Yokohama, Japan

RDC(RESET DOMAIN CROSSING) SIGN-OFF METHODOLOGY ON DESIGNS WITH COMPLEX RESET STRUCTURES

Ma-Eum Lee, Hoo-Nam Kim, Ho-Jin Lee, Hyung-Seob Bae, Won-Sun Park, Seung-Pil Lee, SK hynix, Icheon-si, South Korea; Chang-Ho Do, SK hynix, Ansan, South Korea; Beomkeun Shin, Vikas Sachdeva, Real Intent Inc, Bengaluru, India

FORMAL VERIFICATION CONTRACT BASED MICRO ARCHITECTURAL ANALYSIS OF SERVER SOC'S

Harshal Mumbaikar, Intel Technology India Pvt. Ltd, Raigarh, India; Surinder Sood, Manoj Munigala, Madhusudhan n, Intel Technology India Pvt. Ltd, Bengaluru, India

A NOVEL ANALOG CENTRIC AUTOMATED VERIFICATION METHODOLOGY DRIVEN BY STATE DIAGRAM APPROACH

Gopika Kumar, Texas Instruments, Bengaluru, India; Guha Lakshmanan, Texas Instruments (India) Pvt. Ltd., Bengaluru, India; Otis Gorley, Texas Instruments, McKinney, TX

IS CURVY DESIGN AN OPPORTUNITY OR A DREAM?

Time: 11:30 AM – 12:30 PM
Room: DAC Pavilion, Level 2 Exhibit Hall
Event Type: Tech Talk
Topics Area(s): Design

The semiconductor manufacturing community is ready for the first time in 40 years to enable a wholesale change in what future chips could look like by manufacturing curvilinear features. But most of the chip design community doesn't know that and this talk is about bridging that awareness from manufacturing to the design community. The entire chip design infrastructure is based on the Manhattan assumption. In my previous life in EDA, I had something to do with that, so I know this very well. I also know this is not going to change any time soon. At the same time, though, is there any doubt that a curvilinear "curvy" chip, if magically made possible, would be smaller, faster, and use less power? Of course not. The shortest distance between two points is a straight line. And the least resistive path is a smoothly curved path, not a series of 90 degree turns. Another thing we know from my current life in software for semiconductor manufacturing: a target shape that is easier to manufacture is more reliably manufacturable. And 90-degree turns are not manufacturable, but smooth curvilinear turns are. Curvy designs would yield better, decrease chip size and perform more consistently. There's an opportunity to take advantage of what semiconductor manufacturing has enabled for the first time in 40 years. In this talk, I'll provide a baseline education of how photomasks and wafers are manufactured then summarize the changes in semiconductor manufacturing that enable curvy designs. My goal is to explain why manufacturing is no longer a barrier to curvy design and spark the imagination of the EDA and design community.

Speaker: Aki Fujimura, D2S, Saratoga, CA

PATHWAYS TO REALIZATIONS

Time: 1:30 PM – 3:00 PM
Room: 2008, Level 2
Event Type: Engineering Tracks
Topics Area(s): AI, Back-End Design

Chair/Co-Chair: Dhanapathy Krishnamoorthy, Intel Corporation

ROUTING CONGESTION PREDICTION WITH MACHINE LEARNING IN PHYSICAL SYNTHESIS

Kaylee Trevino, Nancy Zhou, IBM, Austin, TX; Mike Kazda, IBM, Poughkeepsie, NY; Lakshmi Reddy, IBM Research, Yorktown Heights, NY; Alex Suess, IBM Systems, Hopewell Junction, NY; William Dougherty, IBM, Pittsburgh, PA; Hua Xiang, IBM Research, San Jose, CA

REFINING TAPEOUT: AUTOMATION FOR SIMPLICITY AND ACCURACY

Greg Ford, Marvell, Santa Clara, CA; Mark Lasher, Marvell, Colchester, VT

IMPLEMENTING QDI DESIGN WITH CONVENTIONAL SYNCHRONOUS DESIGN FLOW: A CASE OF LONG DISTANCE INTERCONNECT ACROSS VOLTAGE DOMAIN

Kyungmin Lee, Sungmoon Kang, Yongsang Yu, Manhwee Jo, Wooil Kim, Samsung Electronics, Hwaseong, South Korea

INTELLIGENT FLOORPLANNING (IFP)

Mithil Shah, Krunal Agrawal, Intel Technology India Pvt. Ltd, Bengaluru, India

POWER AWARE SCAN STRUCTURE PLANNER

Chen Yuan Kao, Sin Huei Li, Chien Chen Wu, Min Hsiu Tsai, Global UniChip Corp., Hsinchu City, Taiwan

DESIGN RULE DECISION METHODOLOGY FOR BALANCING PROCESS LIMIT AND ROUTABILITY IMPROVEMENT

Seunghwan Song, Jooyeon Kwon, Sangdo Park, Hyung-Ock Kim, Sangyun Kim, Samsung Electronics, Hwaseong, South Korea

DESIGN CONSIDERATIONS FOR EMBEDDED AT THE EDGE

Time: 1:30 PM – 3:00 PM
Room: 2012, Level 2
Event Type: Engineering Tracks
Topics Area(s): Embedded Systems

Chair/Co-Chair: Mark Kraeling, Wabtec

Embedded products have always had a very unique set of requirements. Initial embedded systems were more firmware-based, meaning the software was written and never touched or updated throughout the life of the product. This deployment type has transformed into systems that must be updated, whether it is for new features, security enhancements, or advanced protocol improvements. These type of changes for embedded systems normally occur at the "edge", or where an embedded system is not connecting itself to other systems or a machine interface. In this session we will explore various design considerations for embedded systems that are deployed at the edge.

Presenters: Reed Hinkle, Arm Ltd., Round Rock, TX; Nico Penisoara, NXP Semiconductors, Nice, France; Leila Sabeti, Intel Corporation, San Francisco, CA

AUTOMATING THE FRONT END AND FACING THE BIG PICTURE

Time: 1:30 PM – 3:00 PM
Room: 2010, Level 2
Event Type: Engineering Tracks
Topics Area(s): AI, Cloud, Front-End Design

Chair/Co-Chair: Anil Deshpande, Samsung Electronics

Effective front-end design and validation in the 21st century often requires us to take a step back from our local silos in order to understand the global validation process, and leverage information from multiple domains to achieve success. In this session we will discuss new insights for running general EDA tools more efficiently, enabling effective interactions between design stages, running global regressions more effectively, and leveraging new machine learning technologies.

MACHINE LEARNING BASED ABNORMAL SIMULATION DETECTOR IN SOC VERIFICATION

Jinwoo Park, Yeonho Jeong, Jicheon Kim, Daewoo Kim, Youngsik Kim, Seonil Choi, Samsung Electronics, Hwaseong, South Korea

AUTOMATIC DEBUG KNOWLEDGE SHARING PLATFORM IN SOC VERIFICATION

Yeonho Jeong, Jinwoo Park, Jicheon Kim, Daewoo Kim, Youngsik Kim, Seonil Choi, Samsung Electronics, Hwaseong, South Korea

SYSTEM AND METHOD TO IMPROVE RTL QUALITY BY USING BACKEND TOOLS FLOWS AND METHODOLOGY FOR RTL HANDOFF

Amol Joshi, Anil Kawediya, Intel Corporation, Folsom, CA; Greg Bradford, Intel Corporation, Colorado Springs, CO

SMART ADAPTIVE REGRESSION USING NEAREST NEIGHBOURS ALGORITHM

RajaNataraj Sivaraj, Xiaohan Yang, Rajendra Prasad, Infineon Technologies, Bristol, United Kingdom

SMART COMPREHENSIVE AUTOMATION FRAMEWORKS TO RESOLVE THE MAINSTREAM MICROCONTROLLER SOC DESIGN CHALLENGES

Swathy Lal, Shivani Jayakumar, Ashwini Padoor, Shashank Madineni, Saravanan G, Arif Mohammed, Rajeev Suvarna, Texas Instruments, Bengaluru, India; Sangram Thopte, Texas Instruments, Pune, India; Khyati Kiyawat, Texas Instruments, Madhya Pradesh, India

A NEXT-GENERATION, CLOUD-BASED EDA ENVIRONMENT, BUILT EASILY IN THE AWS CLOUD

Nupur Bhonge, Cliosoft, San Jose, CA; Jessica Tandel, Amazon Web Services, San Francisco, CA; Dnyanesh Digraskar, Amazon Web Services, Austin, TX

IS DEMOCRATIZATION OF CHIP DESIGN ALREADY HAPPENING?

Time: 2:00 PM – 2:45 PM
Room: DAC Pavilion, Level 2 Exhibit Hall
Event Type: DAC Pavilion Panel
Topics Area(s): Design

Moderator: Nitin Dahad, embedded.com, London, United Kingdom

Silicon has become ubiquitous in a way none of us could have imagined. No longer restricted to powerful servers, silicon content has found its way into many systems. Bespoke silicon is no longer rare - and in many cases a necessary step towards differentiation. Be it automotive, mobile or edge, silicon content continues to increase. However, silicon design and manufacturing continues to be accessible to just a few - with a substantial barrier to entry. The panel will discuss how far we have come (or how far behind we are) when it comes to democratizing silicon.

Panelists: Alain Dargelas, RapidSilicon, Los Gatos, CA; Rob Mains, Chips Alliance, Morgan Hill, CA; Rick O'Connor, Open Hardware Group, Ottawa, Canada; Mohamed Kassem, eFabless, Palo Alto, CA; Vic Kulkarni, Silicon Integrative Initiative, Inc., San Jose, CA

PANEL: THOSE DARN BUGS! WHEN WILL THEY BE EXTERMINATED FOR GOOD?

Time: 3:00 PM – 3:45 PM
Room: DAC Pavilion, Level 2 Exhibit Hall
Event Type: DAC Pavilion Panel

Moderator: Brian Bailey, Semiconductor Engineering

Verification is not scaling with design.

While the size of a computer shrank from a mainframe to a watch, an unquestionably remarkable feat, the time to verify these complex designs hasn't. Neither have bug escapes, even though the ratio of verification engineer to designer is 5:1 for most processor design projects, and the cost of verification is 70% of a design verification budget. Even so, the 2020 Wilson Research Group report from Siemens EDA's Harry Foster points out that 68% of ASICS go through a respin and 83% of FPGAs do not work the first time. The elusive zero bug escape is a long-held goal for silicon design houses.

The question many DAC attendees ask is whether bug eradication will ever become a reality. The panel will explore this topic in detail to find out what's causing the industry to not scale verification to the point that we can sign off our chips on time, the first time with zero bugs.

Moderator Brian Bailey will lead panelists through a discussion to the changing verification landscape from functional verification to functional safety and security verification. They will address many of the perceived challenges, including:

- The quality of tools and costs
- Lack of methodology and training
- How management decisions affect the interplay of technology, methodology and verification quality

At the conclusion of the panel, they will attempt to establish what needs to change to make bug eradication a reality. Audience participation will be encouraged.

Panelists: Ashish Darbari, Axiomise; Mark Glasser, Cerebras; Ty Garibay, Mythic AI; Larry Lapides, Imperas

THE HARDWARE/SOFTWARE NEXUS IN CHIP DESIGN

Time: 3:30 PM – 5:00 PM
Room: 2008, Level 2
Event Type: Engineering Tracks
Topics Area(s): Back-End Design

Chair/Co-Chair: Sabya Das, Synopsys

Organizer(s): Sabya Das, Synopsys, San Francisco, CA

Software plays a key role in both the design and enablement of hardware. This session focuses on the interaction between hardware and software to implement efficient chip design flows and application-optimized hardware solutions. The first talk describes a design methodology that employs High-Level Synthesis and a hardware-software co-design framework for designing custom deep learning accelerators. The second talk advocates a software-first approach to build correct-by-construction and optimized hardware using work-load specific simulation feedback at various stages of the design flow. The third talk highlights the challenges in chip emulation and prototyping.

Presenters: Rangharajan Venkatesan, NVIDIA, Santa Clara, CA; Jakob Engblom, Intel Corporation, Stockholm, Sweden; Olivier Coudert, Synopsys, San Francisco, CA

OPEN SOURCE HARDWARE TO ENABLE FASTER TTR

Time: 3:30 PM – 5:00 PM
Room: 2010, Level 2
Event Type: Engineering Tracks
Topics Area(s): IP

Organizer(s): Sashi Oblisetty, Synopsys, Mountain View, CA

Though not as pervasive as open source software, open source hardware is picking up. A quick check on github shows thousands of Verilog projects. What does this mean for the renaissance we are seeing in chip design? How can both established and upcoming companies leverage open source hardware and accelerate business objectives?

Presenters: Jonathan Balkind, University of California, Santa Barbara, CA; Dominic Rizzo, Google, Mountain View, CA; Mike Thompson, Open Hardware Group, Ottawa, Canada

WHEN RTL DOESN'T CUT IT: TOPICS IN ANALOG, MIXED SIGNAL AND CUSTOM IP DESIGN

Time: 3:30 PM – 5:00 PM
Room: 2012, Level 2
Event Type: Engineering Tracks
Topics Area(s): AI, IP

Chair/Co-Chair: Henning Spruth (NXP Semiconductors)

Transistor level design is more important than ever with the complex physics of advanced nodes and market demand for differentiation driving designers to use the full capability of a process. This session showcases novel developments in the areas of analog, mixed signal and custom IP design. It covers a variety of topics such as high sigma Monte Carlo simulations, symbolic verification techniques, DFM, PLL architectures, using machine learning for mixed signal modeling, and verification of analog ML IP.

MEMORY READ YIELD ESTIMATION USING HIGH SIGMA MONTE CARLO

Ashish Kumar, STMicroelectronics, Noida, India; Shubham Varshney, Zia Semiconductor, Noida, India; Rakesh Shenoy, Synopsys, Noida, India

MACHINE LEARNING-BASED BER ESTIMATION IN RECEIVER IBIS-AMI MODELING

Inhwan Song, Soonwon Kwon, Wook Kim, Donghyuk Lim, Soomin Jeon, Woojin Jung, Mintae Lee, Yeon-Ho Im, Hyung-Ock Kim, Samsung Electronics, Hwaseong, South Korea

VERIFYING I/O DESIGNS USING SYMBOLIC SIMULATION TO INCREASE DESIGN AND MODEL ROBUSTNESS

Natish Singla, STMicroelectronics, Noida, India; Anil Kumar Dwivedi, STMicroelectronics, Delhi, India; Geeta Madan, STMicroelectronics, West Delhi, India; Rakesh Shenoy, Synopsys, Noida, India; Moninder Singh, Synopsys, Mountain View, CA

DESIGN FOR MANUFACTURABILITY (DFM) FOR ANALOG IP

Lynn Wang, GlobalFoundries, Santa Clara, CA; Joe LeBritton, Siemens EDA, Austin, TX; Zhao Lee, GlobalFoundries, Singapore, Singapore; Karen Henderson, Siemens EDA, Cambridge, MA; Hossam Sarhan, Siemens EDA, Grenoble, France; Uwe Schroeder, GlobalFoundries, Santa Cruz, CA

FREQUENCY SYNTHESIZERS WITH A PURPOSE IN ADVANCED PROCESS TECHNOLOGIES

Pradeep Thiagarajan, Siemens EDA, Raleigh, NC; Rounak Lokare, Analog Bits, Mountain View, CA

A HIERARCHICAL AND TRACTABLE MIXED SIGNAL VERIFICATION METHODOLOGY FOR FIRST-GENERATION ANALOG AI PROCESSORS

Jay Wang, Mythic, Atlanta, GA; Skylar Skrzyniarz, Weihua Chen, Mythic, Austin, TX; Scott Johnson, Mythic, Round Rock, TX; Sumit Vishwakarma, Siemens EDA, San Jose, CA

MONDAY GLADIATOR POSTER BATTLE

Time: 4:30 PM – 5:30 PM

Room: DAC Pavilion, Level 2

See the 2022 Engineering Track Poster Gladiator finalist present their posters in a speed round. Poster Gladiators are chosen from all Engineering Track sessions including front-end, back-end, IP, embedded and cloud. Attendees and judges vote for the best Poster Gladiator! Come to the Pavilion and cast your vote. The 2022 Poster Gladiator will be selected at the Wednesday Poster Gladiator session.

SUCCESSIVE REFINEMENT- AN APPROACH TO DECOUPLE FRONT-END AND BACK-END POWER INTENT

Rohit Sinha, Kavya Kotha, Intel Technology India Pvt. Ltd, Hyderabad, India

MINIMIZE POWER CONSUMPTION WITH A NOVEL POWER ECO FLOW

Jianfeng Liu, Eunju Hwang, YeongYeong Shin, Seokhoon Kim, Jun Seomun, Sangyun Kim, Samsung Electronics, Hwaseong, South Korea

DESIGN TIMING EFFECTS OF LAYER-TO-LAYER INTERCONNECT SKEW

Ayhan Mutlu, Synopsys, Los Gatos, CA; Duc Huynh, Li-Chung Hsu, Li Ding, Synopsys, San Jose, CA; Jian-Feng Chen, Synopsys, Mountain View, CA

A UNIFIED IP QA METHODOLOGY TO IMPROVE VALIDATION COVERAGE AND THROUGHPUT

Lippika Parwani, STMicroelectronics, Greater Noida, India; Jean-Arnaud Francois, STMicroelectronics, Crolles, France; Geetanjali Sharma, STMicroelectronics, Mumbai, India; Wei-Lii Tan, Siemens EDA, Fremont, CA; Lionel Couder, Siemens EDA, Grenoble, France

MONDAY ENGINEERING TRACKS POSTER RECEPTION

Time: 5:00 PM – 6:00 PM

Room: Level 2 Exhibit Hall

4G/5G ENCODER-DECODER IP USE CASES AND PERFORMANCE VALIDATION IN EMULATION AND POST SILICON USING PORTABLE STIMULUS STANDARD'S HSI

Suresh Vasu, Vinit Shenoy, Nithin Venkatesh, Suhas Reddy, Joydeep Maitra, Intel Technology India Pvt. Ltd, Bengaluru, India; Luis Campos, Intel Corporation, Santa Clara, CA

AUTOMATED TIMING-AWARE DYNAMIC VOLTAGE DROP ECO

Seonghun Jeong, Dongyoun Yi, Byunghyun Lee, Sun Ik Heo, Len Hsu, KH Kim, Synopsys, Hsinchu City, Taiwan; Anusha Gummana, Sankar Ramachandran, Ansys, Bengaluru, India

BACK END OF LINE PROCESS-AWARE STATIC TIMING ANALYSIS

Mijeong Lim, Samsung, Suwon, South Korea

BILLION INSTANCE TIMING SIGN-OFF

Tim Helvey, Marvell, Rochester, MN; David Lawson, Marvell, Orange County, CA

CDC SIGNOFF FLOW WITH DFT LOGIC

Herbert Blesse, Dreamchip Technologies GmbH, Hannover, Germany; Vardan Vardanyan, Real Intent Inc, Yerevan, Armenia

CELL EM AWARE DESIGN OPTIMIZATION

Minseok Kang, Samsung Electronics, Suwon, South Korea; Kwangseok Choi, Samsung Electronics, Hwaseong, South Korea; Jinmo Jung, Synopsys, Mountain View, CA; Vivek Panure, Synopsys, Hyderabad, India

CLOCK SPINE AUTOMATION FOR CLOCK LATENCY AND TURN-AROUND-TIME REDUCTION

Ingeol Lee, Samsung Electronics, Hwaseung-si, South Korea; Jaehoon Kim, Samsung Electronics, Hwaseong, South Korea; Jun Seomun, Samsung Electronics, Hwaseong, South Korea; Sangyun Kim, Samsung Electronics, Hwaseong, South Korea

CLUSTERING CHARACTERIZATION CONDITION FOR MULTI-BIT CELL

Woojin Jung, Mintae Lee, Soyeong Lee, Jaieun Baek, Wook Kim, Keunho Lee, Inhwan Song, Yeon-Ho Im, Samsung Electronics, Hwaseong, South Korea

COMPILER APPROACH FOR AUTOMATING DIE2DIE TRANS-RECEIVER HIP PLACEMENT FOR 3D-IC DESIGN

Madan Lal, Sanjana Kale, Shubham Lunawat, Hemant Jain, Nijesh C, Intel Technology India Pvt. Ltd, Bengaluru, India

DVD DIAGNOSTICS - DEBUGGING DYNAMIC IR PROBLEMS USING ADVANCED ANALYTICS

Ilhan Hatirnaz, NXP Semiconductors, Munich, Germany; Manmeet Singh, Ansys, Noida, India

A DYNAMIC APPROACH TOWARDS NOC PERFORMANCE VERIFICATION IN PRE-SILICON AND OVERCOME THE TRADITIONAL OVERHEADS

Suresh Vasu, Zafar Mohammad, Thirumala Chakravarthy, Intel Technology India Pvt. Ltd, Karnataka, India

ENABLING A 20B-TRANSISTOR CHIP WITH UNIT LEVEL TIMING ABSTRACTION

Adil Bhanji, IBM, Wappingers Falls, NY; Chaitanya Peddawad, IBM, Bengaluru, India; Jack DiLullo, IBM, Austin, TX; Jason Morsey, IBM, Hopewell Junction, NY; Michael Wood, IBM, Lancaster, OH; Ravichander Ledalla, IBM, Fishkill, NY

EFFICIENT CUSTOM LOGIC P&R FLOW USING VIRTUAL HIERARCHY

Doh-young Kim, Youngjai Ryu, Dongmin Lee, Hun Lim, Youngjin Cho, Samsung Electronics, Hwaseong, South Korea; Keunbong Lee, Cadence Design Systems, Inc., Santa Clara, CA; Jungmin Choi, Cadence Design Systems, Inc., Icheon-si, South Korea

FORMAL VERIFICATION OF DEEP NEURAL NETWORKS IN HARDWARE

Kenneth Roe, Shreyansh Agrawal, Intel Technology India Pvt. Ltd, Jabalpur, India; Surinder Sood, Intel Technology India Pvt. Ltd, Bengaluru, India

IMPROVING FPGA QUALITY & PROTOTYPING TURN AROUND TIME USING STATIC VERIFICATION

Amit Goldie, Himanshu Kathuria, Synopsys, Noida, India; Ankush Bagotra, Synopsys, Mountain View, CA; Sampath Amarasinghe, Synopsys, Etobicoke, Canada

LEARNINGS FROM RDC SIGN-OFF ON LOW POWER SOC

Jieun Ahn, Samsung Electronics, Seoul, South Korea; Seongdeuk Jo, Woohyun Son, Kiseok Bae, Mijung Noh, Samsung Electronics, Hwaseong, South Korea; Hyobeen Park, Real Intent Inc, Sunnyvale, CA; Vikas Sachdeva, Real Intent Inc, Bengaluru, India

LIBRARY ANALYTICS AND LIBRARY PARTITIONING [LALP] FOR PPA EFFICIENCY

Sourav Saha, Rushabh Shah, Raghunandana R, Shrikrishna Gawade, Divya M, Praveen Ghagare, Intel Corporation, Bengaluru, India

LOGFILE ERROR ANALYSIS: HOW TO MAKE SENSE OF MILLIONS OF LINES OF LOGFILES USING CHEW_LOGS (CHECK ERRORS AND WARNING IN LOGFILES)

Thomas Arneberg, Marvell, Chippewa Falls, WI

MACHINE LEARNING TECHNIQUES FOR PDK DEVELOPMENT EFFICIENCY

Nolan Pavek, GlobalFoundries, Miami, FL; Romain Feuillette, GlobalFoundries, Burlington, CA; Vivienne Miller, GlobalFoundries, Ellicott City, MD

NEW METHODOLOGY FOR EXTRACTING TEST COVERAGE ON PURE DRAM & FLASH DESIGN

SeaEun Park, SeongWook Lee, Samsung Electronics, Hwaseong, South Korea; Jungyun Choi, Samsung Electronics, Hwasung-si, South Korea

ON-CHIP PDN-AWARE SIMULATION METHODOLOGY WITH RC NETWORK REDUCTION

Juho Jeon, Donghyun Kang, Seonghyeon Park, Mingu Kang, Hwapyong Kim, Haeun Jeon, Youngho Seo, Yujin Lee, Seungjae Lee, Soeun Sin, Sojin Kim, Kwangok Jeong, Hyuckjoon Kwon, Jungyun Choi, Seunghyeok Kwon, Samsung Electronics, Cheonggye-dong, South Korea; Botak Lim, Daehee Lee, Samsung Electronics, Yongin, South Korea

OVERCOMING IR CHALLENGES FOR RETICLE SIZED ASIC IN NEW ARCHITECTURE AND ADVANCED NODE

Swati Jindal, Microsoft, Fremont, CA; Anand Iyer, Microsoft, Mountain View, CA; Pranav Ranganathan, Microsoft, Raleigh, NC

POWER SOLUTION TO MAXIMIZE PERFORMANCE-PER-WATT FOR GPGPU

Shixuan Que, Yuanyuan Ling, Iluvatar, Shanghai, China; Ling Sun, Lili Dai, Iluvatar, Nanjing, China; Zhenbang Wang, Ansys, Pittsburgh, PA

POWER-THERMAL CO-SIMULATION FOR MORE ACCURATELY DC IRDROP AND TEMPERATURE DISTRIBUTION OF GPGPU'S PCB AND PACKAGE

Shuyuan Guan, Birentech, Shanghai, China; Zhenghao Chu, Ansys, Beijing, China

PRE AND POST SILICON ANALYSIS IN THE DESIGN AND VALIDATION OF AI ENABLED HIGH PERFORMANCE MICROPROCESSORS

Nagu Dhanwada, IBM, Poughkeepsie, NY; Karthik Swaminathan, IBM Research, Yorktown Heights, NY; Kartik Acharya, IBM, Atlanta, GA; Khajista Fattu, Anurag Umbarkar,IBM, Austin, TX; Ramon Bertran, IBM Research, New York City, NY

ROBUST FSM VERIFICATION APPROACH HANDLING CRITICAL CDC CONVERGENCE SCENARIOS

Abhinav Parashar, Texas Instruments, Karnataka, India; Harish Maruthiyodan, Texas Instruments (India) Pvt. Ltd., Bengaluru, India

ROHD: THE RAPID OPEN HARDWARE DEVELOPMENT FRAMEWORK

Max Korbel, Intel Corporation, Santa Clara, CA

A SCALABLE FRAMEWORK TO VALIDATE INTERCONNECT-BASED FIREWALLS TO ENHANCE SOC SECURITY COVERAGE

Ashutosh Mishra, Intel Technology India Pvt. Ltd, Bengaluru, India

SMART STRATEGY TO ANALYZE CDC VIOLATION RELATED TO IPS INTERACTION AT SOC

Amanjit Panda, Western Digital, Bengaluru, India; Nanda Pallari, Western Digital, Hyderabad, India; Varun Sharma, Real Intent Inc, Bengaluru, India

STATIC TIMING AND POWER ANALYSIS WITH PROCESS SPACE EXPLORATION

Changho Han, Chul Rim, Sun Ik Heo, Samsung Electronics, Hwaseong, South Korea; Mijeong Lim, Samsung Electronics, Seoul, South Korea; Asheesh Baghel, Synopsys, Hyderabad, India; Ruijing Shen, Synopsys, New York City, NY; Mayur Bubna, Synopsys, Sunnyvale, CA; Li Ding, Synopsys, San Jose, CA

SYSTEM-LEVEL DEADLOCK SIGN-OFF USING ARCHITECTURAL FORMAL VERIFICATION

Bhushan Parikh, Shaman Narayana, Intel Corporation, Chandler, AZ

TIME INTERLEAVING OF ANALOG TO DIGITAL CONVERTERS CALIBRATION TECHNIQUES

Adeel Ahmad, Vervesemi Microelectronics PVT LTD, Greater Noida, India

USING FORMAL VERIFICATION SIGNOFF FOR DIGITAL IP

David Vincenzoni, STMicroelectronics, Agrate Brianza, Italy

A JOURNEY TO SW/HW CO-DESIGN IN MACHINE LEARNING: FUNDAMENTAL, ADVANCEMENT, AND APPLICATION

Time: 10:30 AM – 12:00 PM
Room: 3004, Level 3
Event Type: Tutorial
Topics Area(s): AI, EDA

Organizer(s): Cong Hao, Georgia Institute of Technology, Atlanta, GA; Lei Yang, University of New Mexico, Albuquerque, NM; Meng Li, Facebook, San Francisco, CA;

The rapid evolution of machine learning (ML) has been enabling the integration of intelligence into various applications.

In today's ML-empowered applications, maximizing accuracy is no longer the only design objective; instead, the demands on hardware efficiency (e.g., latency, power) is sharply increasing. Driven by different objectives, two individual research threads, i.e., ML algorithm design and hardware acceleration, are being intensively investigated. However, to achieve the best accuracy-efficiency trade-off, two threads must be jointly studied and eventually merge into one journey.

In this tutorial, we aim to guide the interested audiences to the walk through the exhilarating journey towards efficient software/hardware co-design in ML-empowered systems, as well as its vast interests in a wide range of applications. Given the complexity of the topic and rich background knowledge required, we divide the tutorial into three talks, progressively leading to the goal from the fundamentals to advanced techniques, and to applications. The three talks will also cover different aspects of applications: autonomous systems, medical and drug discovery, and on-device augmented reality (AR).

Talk I aims to introduce the fundamentals of efficient ML acceleration design, as well as automated ML algorithm design, i.e., neural architecture search (NAS), which establishes the foundation for more advanced co-design techniques and applications. Talk I will also briefly introduce the co-design application in power-efficient autonomous systems. Talk II aims to discuss co-design technique advancements such as systematic co-design frameworks on top of Talk I, as well as real-world applications of co-design techniques with unique challenges and opportunities, especially fairness and privacy. Talk III specifically targets an emerging application from industry, augmented reality (AR), which has a sharply rising demand for sw/hw co-design for both vision and speech tasks.

Presenters: Cong Hao, Georgia Institute of Technology, Atlanta, GA; Lei Yang, University of New Mexico, Albuquerque, NM; Meng Li, Facebook, San Francisco, CA;

APPROXIMATE COMPUTING: FROM EMERGING COMPUTATIONAL PARADIGM TO SYSTEM DESIGN AND APPLICATIONS

Time: 10:30 AM – 12:00 PM
Room: 3005, Level 3
Event Type: Tutorial
Topics Area(s): Design, EDA

Organizer(s): Weiqiang Liu, Nanjing University of Aeronautics and Astronautics, Nanjing, China; Chongyan Gu, Queen's University Belfast, Belfast, United Kingdom

Computing systems are conventionally designed to operate as accurately as possible. However, this trend faces severe technology challenges, such as power dissipation, circuit reliability, and performance. There are several pervasive computing applications (such as machine learning, pattern recognition, digital signal processing, communication, robotics, and multimedia), that are inherently error-tolerant or error-resilient. Approximate computing has been proposed for highly energy-efficient systems targeting the above-mentioned emerging error-tolerant applications; approximate computing consists of approximately (inexactly) processing data to save power and achieve high performance, while results remain at an acceptable level for subsequent use. This tutorial starts with the motivation of approximate computing and then it reviews current techniques for approximate hardware designs.

This tutorial will cover the following topics:

1. Exploiting Approximate Computing for Efficient and Reliable Convolutional Neural Networks: The technology evolution addresses the demand for faster computers. Despite the achieved speed-up in terms of memory and computation performances, the workload involved in DNN application is still hard to fit the embedded device. The Approximate Computing (AxC) paradigm aims at solving this problem by reducing the precision of the hardware/software components leading to an efficient implementation of the DNN. The literature mainly exploited AxC for achieving energy efficiency or improving performance, however AxC has also an impact of the robustness and the reliability of DNNs. In this context, we will provide a brief introduction on existing and latest AxC solutions for achieving efficiency and reliable DNN.

2. Adaptive Approximation for Energy-Efficient Machine Learning: Energy consumption of Information and Computing Technologies (ICT) has been expanding its footprint in the global energy footprint. With the ever-pervasive presence of machine learning and especially deep learning algorithms, they play a notable role in this overall energy consumption. Consequently, managing the energy consumption of these systems has become a top priority. In this talk, first, we briefly present self-awareness concepts as one of the efficient bases of adaptivity in modern systems. Next, after a glance into various fundamental approximate computing methods, we present adaptive approximation as a key to energy-aware machine learning. We present several solutions to demonstrate various adaptive approximation methods used as well as their benefits. We use these examples to draw our conclusions and project a path forward.

Presenters: Alberto Bosio, Lyon Institute of Nanotechnology, Lyon, France; Nima Taherinejad, Technische Universität Wien, Vienna, Austria

CLOUD COMPUTING AND EDGE COMPUTING FOR CONNECTED AND AUTOMATED VEHICLES

Time: 10:30 AM – 12:00 PM
Room: 3001, Level 3
Event Type: Tutorial
Topics Area(s): Autonomous Systems, Cloud

Organizer(s): Ziran Wang, Toyota Motor North America, Mountain View, CA;

The recent development of cloud computing and edge computing bring forward numerous novel technologies whose application scenarios are not only applied to the user level (e.g., individual consumer or private company), but also the system level (e.g., commercial or industrial sector). For example, cloud computing and edge computing play a significant role in the current Connected and Automated Vehicle (CAV) technology, which enable CAVs to offload their massive on-board data and heavy computing tasks. By leveraging the Internet of Things (IoT) technology, different entities in the intelligent transportation system (e.g., vehicles, infrastructure, traffic management centers, etc.) get connected with each other, thus making the entire system smarter, safer, and more efficient.

However, these advances also bring significant challenges to public authorities, industry, as well as scientific communities. In terms of system design and control, current cloud and edge architecture of CAVs need to be refined or even redesigned to better function under uncertainties in demand, and to better cooperate with existing conventional vehicles and infrastructure. From the performance assessment perspective, models and simulation tools based on artificial intelligence and big data have been widely developed for validation and evaluation of cloud computing and edge computing, in particular taking into account the increasing trends in vehicle connectivity and automation. However, the validity of these models needs to be re-examined with field implementations.

This tutorial is composed of three talks. The first talk will be given by Dr. Wang, regarding the utilization of cloud computing in a digital twin framework designed for CAVs. The second talk will be given by Prof. Shi regarding edge computing and its applications in CAVs. The third talk will be given by Prof. Zhu regarding the assured design of CAVs to build a trust framework with edge servers.

Presenters: Qi Zhu, Northwestern University, Evanston, IL; Ziran Wang, Toyota Motor North America, Mountain View, CA; Weisong Shi, Wayne State University, Detroit, MI

EFFICIENT COMPUTER VISION FOR EMBEDDED SYSTEMS

Time: 10:30 AM – 12:00 PM
Room: 3002, Level 3
Event Type: Tutorial
Topics Area(s): Embedded Systems

Organizer(s): Yung-Hsiang Lu, Purdue University, West Lafayette, IN

Many embedded systems are equipped with cameras and can capture vast amounts of visual data continuously. Due to limited energy and wireless data rates, the raw data (i.e., pixels) cannot be transmitted and must be analyzed at the embedded systems. The tutorial provides hands-on experience improving energy efficiency of computer vision. The first speaker will provide step-by-step instruction using PyTorch for quantization, pruning, and knowledge distillation. The second speaker will present the solutions that won the 2020 and 2021 IEEE Low-Power Computer Vision Challenge. The third speaker will explain engineering principles and processes to create reproducible software for machine learning.

Presenters: Abhinav Goel, NVIDIA; Zhenyu Wu, Wormplex AI Research; George Thiruvathukal, Loyola University Chicago

TOWARDS FULLY-HOMOMORPHIC-ENCRYPTION-BASED PRIVACY-PRESERVING COMPUTING: A CROSS-LAYER DESIGN PERSPECTIVE

Time: 10:30 AM – 12:00 PM
Room: 3003, Level 3
Topics Area(s): Design, Security

Organizer(s): Song Bian, Kyoto University, Kyoto, Japan; Yue Zhang, Nanyang Technological University, Beijing, China

In a typical anything-as-a-service scheme, average clients are reluctant to send their personal data to untrusted servers. Moreover, recent law regulations limit the irresponsible use of private data as more and more financial values are discovered and harvested from the growing amount of data. Privacy-preserving computing becomes critical to enabling average clients to use untrusted servers. In particular, homomorphic encryption (HE) is one of the most promising cryptographic technologies to building privacy-preserving computing systems. Unfortunately, in most real-world applications, HE, especially fully homomorphic encryption (FHE), is notorious for its prohibitive amount of computational overheads. For instance, even on the latest fully-customized FHE hardware accelerator (i.e., F1 from MICRO'21), a FHE-based neural network inference on a small image still requires 0.24 seconds.

To better systematize the opportunities and challenges of FHE-based privacy-preserving computing, in this tutorial, we focus on providing with the audience a thorough introduction to FHE, as well as novel insights over the timely topic of cryptography, hardware, software, and machine learning co-design for the FHE-specific hardware acceleration. We make the observation that the main obstacle behind the design of such privacy-preserving computing systems is the multi-disciplinary nature of real-world applications. Consequently, only a cross-layer design and optimization approach can make such FHE-based privacy-preserving computing systems practical. Therefore, we will organize the tutorial with the following components.

1. Cryptography and Applications

Dr. Lei Jiang will introduce the preliminary knowledge on the algebraic and algorithmic foundations of ring learning with errors (RLWE)-based FHE. They will also present their recent progresses over applying privacy-preserving neural network inference (ICRL'21, ICML'21) to visual recognition, text analysis, and other industrial real-world applications.

2. FHE Circuit Construction and Synthesis

Dr. Takashi Sato will present his recent work on a FHE standard cell library (WAHC'21), optimizations on FHE-based Boolean circuitry, and a FHE-based RISC-V CPU (Security'21). He will present how to build composite logic gates over FHE, e.g., 3-input gates and multi-output gates using FHE including Half Adder, Full Adder and AOI21. At last, he will introduce how to build a FHE-based five-stage pipelined RISC-V processor using customized FHE gates.

3. Hardware and Algorithm Co-design

Dr. Jiansong Zhang will introduce their latest results on hardware-accelerated privacy-preserving machine learning. More specifically, they will introduce their recent work on privacy-preserving neural-network inference, where a new convolution protocol is proposed to aid the efficient design of accelerator architecture (TIFS'21, CVPR'20). Then, they will introduce the latest hardware architecture from industry to accelera te real-world deployment of FHE-based secure protocols.

Presenters: Lei Jiang, Indiana University, Bloomington, Bloomington, IN; Takashi Sato, Kyoto University, Kyoto, Japan; Jiansong Zhang, Alibaba Group, Beijing, China

EFFICIENT COMPUTER VISION FOR EMBEDDED SYSTEMS

Time: 1:30 PM – 3:00 PM
Room: 3001, Level 3
Event Type: Tutorial
Topics Area(s): Embedded Systems

Organizer(s): Yung-Hsiang Lu, Purdue University, West Lafayette, IN

Many embedded systems are equipped with cameras and can capture vast amounts of visual data continuously. Due to limited energy and wireless data rates, the raw data (i.e., pixels) cannot be transmitted and must be analyzed at the embedded systems. The tutorial provides hands-on experience improving energy efficiency of computer vision. The first speaker will provide step-by-step instruction using PyTorch for quantization, pruning, and knowledge distillation. The second speaker will present the solutions that won the 2020 and 2021 IEEE Low-Power Computer Vision Challenge. The third speaker will explain engineering principles and processes to create reproducible software for machine learning.

Presenters: Abhinav Goel, NVIDIA; Zhenyu Wu, Wormplex AI Research; George Thiruvathukal, Loyola University Chicago

HARDWARE/SOFTWARE CO-DESIGN WITH HIGH-LEVEL SYNTHESIS

Time: 1:30 PM – 5:00 PM
Room: 3005, Level 3
Topics Area(s): Design

Organizer(s): Mathilde Karsenti, Siemens EDA, San Francisco, CA

Software has many desirable characteristics. But it is slow and very energy hungry compared to hardware. When algorithms implemented as software cannot meet performance or power requirements, moving the function to hardware will improve the speed and efficiency of the system. High-Level Synthesis (HLS) takes a description of an algorithm, typically in C or C++, and produces a synthesizable RTL description suitable for implementation. Given the similarity of software source code and an algorithmic description, HLS offers a practical and easy way to migrate software functions to hardware.

This tutorial will demonstrate this transformation on an example algorithm from a full software implementation to a high performance, efficient implementation with a mix of hardware and software elements. The example will be a neural network based “wake wordâ€ detection algorithm, one commonly used to “wakeâ€ a personal assistant or other device. Since a wake word algorithm needs to run continuously even if the device is hibernating, power consumption is critical, especially if the device is battery powered.

The algorithm will start as a full software implementation running on a RISC-V core. The base design will be constructed by leveraging the Embedded Scalable Platforms (ESP) project developed at Columbia University. ESP is an open-source platform that supports research on the design and programming of heterogeneous SoC architectures. The algorithm will be characterized for performance and power consumption when implemented in a Global Foundries silicon process technology.

The algorithm will be profiled to determine the functions with the largest computational load. Using HLS, these functions will be compiled into accelerators described as synthesizable RTL. ESP’s accelerator design flow will be used to create the hardware and software interfaces for the accelerator and integrate the accelerator into the ESP design. The accelerator designs will be taken through RTL synthesis and place and route for a detailed analysis of power, performance, and area (PPA). Post synthesis, the design will be optimized for power on GlobalFoundries silicon process technology. Given the automation in the creation, integration, and optimization of the accelerator, it will be shown how it is practical to iterate over several design alternatives. PPA metrics will be collected for the complete SoC, including the processor, memory, interconnect, and accelerators. Various architectures and their PPA metrics will be presented and compared.

All sources used in the tutorial example designs will be made available as open-source code.

Presenters: Luca Carloni, Columbia University, New York, NY; Sadhvi Praveen, Siemens EDA, Portland, OR; Russell Klein, Siemens EDA, Wilsonville OR, OR; Shashank Nemawarkar, GlobalFoundries, Austin, TX

HW/SW CODESIGN FOR IN-MEMORY COMPUTING ARCHITECTURES: ADVENTURE FROM EMERGING TECHNOLOGY TO INTELLIGENT COMPUTING SYSTEMS

Time: 1:30 PM – 5:00 PM
Room: 3002, Level 3
Topics Area(s): Design

Organizer(s): Onur Mutlu, ETH Zürich, Zurich, Switzerland; Hussam Amrouch, University of Stuttgart, Stuttgart, Germany; Jian-Jia Chen, Technische Universität Dortmund, Dortmund, Germany

Breakthroughs in deep learning continuously fuel innovations that substantially enhance our daily life. However, DNNs largely overwhelm conventional computing systems because the latter is severely bottlenecked by the data movement between processing units and memory. As a result, novel and intelligent computing systems become more and more inevitable in order to improve or even replace current von-Neumann principles, which have remained unchanged for decades.

This tutorial provides a comprehensive overview on the major shortcomings of modern architectures and the ever-increasing necessity for novel designs that fundamentally reduce memory latency and energy through enabling data processing near to the memory or even inside the memory itself. The tutorial also discusses in detail the great promise of recent emerging beyond-CMOS devices like Ferroelectric Field-Effect Transistor (FeFET) and Resistive Random-Access Memory (ReRAM). It bridges the gap between the latest innovations in the underlying technology and the recent breakthroughs in computer architectures. It demonstrates how HW/SW codesign is a key to realize efficient, yet reliable in-memory and near-memory computing.

The first part (given by Hussam Amrouch, Stuttgart Uni.) will be focusing on the emerging ferroelectric (FeFET) technology and its great potential in building efficient in-memory computing architectures. It will also explain how abstracted reliability models can be developed and later employed towards realizing HW/SW codesign for robust in-memory computing. Further, it will also discuss how compact Logic-in-Memory can be built using FeFET technology and how that outstandingly synergizes with novel brain-inspired hyperdimensional computing algorithms.

The second part (given by Onur Mutlu, ETH Zurich) will be focusing on two promising novel directions: 1) processing using memory, which exploits analog operational properties of memory chips to perform massively-parallel operations in memory, with low-cost changes, 2) processing near memory, which integrates sophisticated additional processing capability in memory controllers, the logic layer of 3D-stacked memory technologies, or memory chips to enable high memory bandwidth and low memory latency to near-memory logic.

The third part (given by Jian-Jia Chen, TU Dortmund) will be covering how novel neural network models such as Binary Neural Networks (BNNs) and Spiking Neural Networks (SNNs) can be proactively trained and constructed in the presence of errors stemming from the underlying emerging technology. In addition, it will discuss how convolutional neural network (CNN) under operation unit (OU) on memory crossbar.

Presenters: Hussam Amrouch, University of Stuttgart, Stuttgart, Germany; Onur Mutlu, ETH Zürich, Zurich, Switzerland; Jian-Jia Chen, Technische Universität Dortmund, Dortmund, Germany

SCALABLE DESIGN-PROGRAM-COMPILATION OPTIMIZATIONS FOR QUANTUM ALGORITHMS: USING QUANTUM NEURAL NETWORK AS A CASE STUDY

Time: 1:30 PM – 5:00 PM
Room: 3004, Level 3
Topics Area(s): AI, Design

Organizer(s): Weiwen Jiang, George Mason University, Fairfax, VA; Bochen Tan, University of California, Los Angeles, CA; Gushu Li, University of California, Santa Barbara, CA

Along with the rapid development of quantum computers, using only 5 years to scale up the number of qubits from 5 to 127 in IBM Quantum, it provides opportunities for more applications to take full use of powerful quantum computers. Along with the increasing numbers of qubits, saying IBM plans to debut quantum computers with more than 1,000 qubits in 3 years, new challenges and questions are posed in designing, programming, synthesizing, and mapping applications to quantum computers at scale:

(1) how to synthesize and map (i.e., compile) the logical circuit to physical qubits; (2) how to program applications to adapt to quantum computing; and (3) how to design a quantum circuit with potential quantum advantage? This tutorial is composed of three talks to address all the above issues. We will start from a specific task, i.e., compilation. Based on the team's previous work, OLSQ [1], we will show how to automatically optimize and transform quantum programs to meet hardware limitations to respond to issue (1). Then, we will introduce how to systematically derive new large-scale quantum program optimizations, including the projection-based assertion and Paulihedral compiler to address the issue (2). Finally, toward the quantum advantage in issue (3), we will narrow our focus down to a case-study application, i.e., quantum neural network. We will demonstrate how to design, program, and compile the quantum neural network, which is based on the team's recent work QuantumFlow [2], published at Nature Communications. In the above three talks, the hands-on experience could be gained in optimizing quantum circuits to physic qubits and implementing the neural network on the quantum circuit through the on-site coding demonstration. All attendees will leave with code examples that they can use as the backbone implementation to their own projects.

Presenters: Jason Cong, University of California, Los Angeles, CAYufei Ding, University of California, Santa Barbara, CA; Weiwen Jiang, George Mason University, Fairfax, VA; Yiyu Shi, University of Notre Dame, Notre Dame, IN

SECURE SHARING OF FPGAS IN THE CLOUD

Time: 1:30 PM – 5:00 PM
Room: 3003, Level 3
Topics Area(s): Cloud, Security

Organizer(s): Mehdi Tahoori, Karlsruhe Institute of Technology, Karlsruhe, Germany

The shared FPGA platform in the cloud is based on the concept that the FPGA real estate can be shared among various users, probably event at different privilege levels. Such multi-tenancy comes with new security challenges, in which one user, while being completely logically isolated from another, can cause security breaches to another user on the same FPGA. In addition, such a hardware security vulnerability does not require physical access to the hardware to perform measurements or fault attacks, hence it can be done completely remotely. The main objective of this tutorial, which consists of the three components of in-depth lecture, live demo and hands-on experience is to introduce the new challenges coming from sharing FPGAs in both cloud as well as state of the art heterogeneous Systems on Chip (SoCs). It will explore the remote active and passive attacks at the electrical level for multi-tenant FPGAs in the cloud and SoCs and discusses possible countermeasures to deal with such security vulnerabilities.

The first part of this tutorial is an in-depth lecture covering the new trends in design of heterogeneous FPGASoCs as well as sharing the FPGAs in the clouds and the associated security vulnerabilities. The lecture part is given by three speakers: Amir Moradi, Mehdi Tahoori and Mirjana Stojilovic. In the first lecture by Amir Moradi, the traditional side channel and fault attacks are reviewed. The second part, given by Mehdi Tahoori covers how the power delivery network (PDN) on the chip, board and system level can be utilized as a side channel medium and how the legitimate programmable logic constructs of the FPGA can be exploited for side channel voltage fluctuation measurements as well as injecting faults on the PDN for fault attacks and denial of service. Also, various countermeasures in terms of offline bitstream checking and online approaches based on fencing and sandboxing will be covered. The third lecture by Mirjana Stojilovic discusses escalation of such security vulnerabilities and attacks it in the cloud and cloud-level considerations.

In the second part of the tutorial, we present attacks live on recent cloud FPGAs, such as the Intel Stratix 10 and the Xilinx Virtex Ultrascale+. The respective attacks, which are Correlation Power Analysis as well as a Differential Fault Attack on the AES will be explained in details to the attendees, who will be able to learn how to derive secret AES keys from faulty ciphertexts and side-channel measurements in a real system. Moreover, we demonstrate how recent FPGAs can be crashed in a Denial-of-Service attack, making recovery without power cycling impossible.

Finally, the third part is a hands-on experience using low cost Lattice iCE40-HX8K breakout boards together with a comprehensive graphical interface, which can be used to control various parameters of the measurement or fault injection process on the FPGA. On this platform, participants of the tutorial are able to perform the demonstrated attacks themselves and learn about the importance of the respective parameters as well as the details of the attacked implementation.

Mehdi Tahoori, Karlsruhe Institute of Technology; Mirjana Stojilović, École Polytechnique Fédérale de Lausanne; Dennis Gnad, Karlsruhe Institute of Technology

A JOURNEY TO SW/HW CO-DESIGN IN MACHINE LEARNING: FUNDAMENTAL, ADVANCEMENT, AND APPLICATION

Time: 3:30 PM – 5:00 PM
Room: 3001, Level 3
Topics Area(s): Al Cong Hao, Georgia Institute of Technology, Atlanta, GA; Lei Yang, University of New Mexico, Albuquerque, NM; Meng Li, Facebook, San Francisco, CA

Organizer(s):

The rapid evolution of machine learning (ML) has been enabling the integration of intelligence into various applications.

In today's ML-empowered applications, maximizing accuracy is no longer the only design objective; instead, the demands on hardware efficiency (e.g., latency, power) is sharply increasing. Driven by different objectives, two individual research threads, i.e., ML algorithm design and hardware acceleration, are being intensively investigated. However, to achieve the best accuracy-efficiency trade-off, two threads must be jointly studied and eventually merge into one journey.

In this tutorial, we aim to guide the interested audiences to the walk through the exhilarating journey towards efficient software/hardware co-design in ML-empowered systems, as well as its vast interests in a wide range of applications. Given the complexity of the topic and rich background knowledge required, we divide the tutorial into three talks, progressively leading to the goal from the fundamentals to advanced techniques, and to applications. The three talks will also cover different aspects of applications: autonomous systems, medical and drug discovery, and on-device augmented reality (AR).

Talk I aims to introduce the fundamentals of efficient ML acceleration design, as well as automated ML algorithm design, i.e., neural architecture search (NAS), which establishes the foundation for more advanced co-design techniques and applications. Talk I will also briefly introduce the co-design application in power-efficient autonomous systems. Talk II aims to discuss co-design technique advancements such as systematic co-design frameworks on top of Talk I, as well as real-world applications of co-design techniques with unique challenges and opportunities, especially fairness and privacy. Talk III specifically targets an emerging application from industry, augmented reality (AR), which has a sharply rising demand for sw/hw co-design for both vision and speech tasks.

Presenters: Cong Hao, Georgia Institute of Technology, Atlanta, GA; Lei Yang, University of New Mexico, Albuquerque, NM; Meng Li, Facebook, San Francisco, CA

Tuesday, July 12, 2022

AWARDS AND TUESDAY KEYNOTE

Time: 8:40 AM – 9:45 AM
Room: 3008-3012, Level 3
Event Type: Keynote

COMPUTATIONAL SOFTWARE AND THE FUTURE OF INTELLIGENT ELECTRONIC SYSTEM DESIGN

Anirudh Devgan, Cadence Design Systems, Inc., Atherton, CA

The EDA industry has driven orders of magnitude productivity, scalability, and quality improvements. We are now in the era of AI, where it impacts our daily lives, the products we depend on, and how we design those electronics systems. But adding AI technology to existing tools and flows is only the first step in this journey. We can now deliver optimization across multiple dimensions, intersecting domains, and historically loosely coupled components of systems. These new dimensions are transforming the industry, resulting in multiple orders of magnitude improvements in system design productivity with optimization results never before possible or even conceived.

Tuesday Sessions

THE STATE OF EDA: A VIEW FROM WALL STREET

Time: 10:15 AM – 11:15 AM
Room: DAC Pavilion, Level 2 Exhibit Hall
Event Type: Analyst Presentation
Topics Area(s): EDA

We will examine the financial performance and structure of the EDA industry through 2021, as well as the material technical trends and requirements that have affected EDA business performance and strategies. In addition, we will examine the progression of semiconductor R&D spending. Lastly, we will examine how the market value of the publicly-held EDA companies has evolved and provide our EDA industry projections for 2022 through 2024.

Speaker: Jay Vleeschhouwer, Griffin Securities, New York City, NY

POWER PLAY MUSINGS

Time: 10:30 AM – 12:00 PM
Room: 2008, Level 2
Event Type: Engineering Tracks
Topics Area(s): Back-End Design

Chair/Co-Chair: Badhri Uppiliappan, Analog Devices

PROTOTYPING AND VERIFICATION OF POWER DELIVERY NETWORK FOR A FOVEROS 3DIC DESIGN.

Amartya Mazumdar, Vineet Sreekumar, Basavaraj Kanthi, Intel Corporation, Bengaluru, India; Chandrahas Alla, Intel Corporation, Andhra Pradesh, India; Manish Kumar, Intel Corporation, Austin, TX; Alina Sebastian, Intel Corporation, Kerala, India; Tapan Ganpule, Intel Corporation, Folsom, CA

EXPERIMENTAL VALIDATION OF A NOVEL METHODOLOGY FOR ELECTROMIGRATION ASSESSMENT IN ON-CHIP POWER GRIDS

Valeriy Sukharev, Siemens EDA, Fremont, CA

VFOPT: ML-BASED OPTIMIZATION VOLTAGE/FREQUENCY EXPLORATION SYSTEM

Jaemin Seo, Yun Heo, Kunyuk Kang, Samsung Electronics, Hwaseong, South Korea; Varun Gunnala, Synopsys, Hyderabad, India; Donghyun Lee, Synopsys, San Francisco, CA

ON-CHIP DYNAMIC IR DROP INDUCED DETERMINISTIC JITTER ANALYSIS USING STA NATIVE TIMING ENGINE

Dongchul Kim, Samsung Electronics, City, South Korea

IR DROP FIXING USING TIMING ECO INTEGRATED SOLUTION WITH IR SIGNOFF TOOL

Sahil Sukheja, Amruthavalli Sreekantapuram, Mathew Kaipanatu, Google, Bengaluru, India

SIGMADVD (SDVD): HIGH COVERAGE SOLUTION FOR POWER INTEGRITY SIGNOFF

Anusha Vemuri, Emmanuel Chao, Santosh Santosh, NVIDIA, Santa Clara, CA; Piyush Jain, Ansys, San Jose, CA; Yatender Mishra, Ansys, San Francisco, CA

NEW DEVELOPMENTS IN SECURITY VERIFICATION AND CONTROLLING UNPREDICTABLE BEHAVIOR

Time: 10:30 AM – 12:00 PM
Room: 2010, Level 2
Event Type: Engineering Tracks
Topics Area(s): Front-End Design

Chair/Co-Chair: Ankit Gopani, Intel Corporation

Every day, we read about new hacks and criminal cyberattacks in the news, underscoring the continuing need to consider security in every facet of design. In this session we will learn about the latest novel ideas in security verification, as well as related concepts of preventing and detecting unknown values.

EXTRACTING SOURCE OF UNKNOWN VALUES IN TRANSISTOR-LEVEL LOGIC SIMULATION

Kwangsun Kim, Hyungjung Seo, Younsik Park, Jungyun Choi, Samsung Electronics, Hwaseong, South Korea

VERIFYING SECURITY COUNTERMEASURES FOR SIDE CHANNEL FAULT ATTACKS, IN AN INTEGRATED CIRCUIT AT RTL OR GATE LEVEL, USING FAULT ATTACK SIMULATION (FAS)

Sesha Kumar C V, Optima Design Automation, Bengaluru, India; Jamil R. Mazzawi, Optima Design Automation, Nazareth, Israel; Ayman Mouallem, Optima Design Automation, Akko, Israel

RTL DESIGN SECURITY VERIFICATION FOR RESISTING POWER SIDE-CHANNEL ANALYSIS

Kazuki Monta, Makoto Nagata, Kobe University, Kobe, Japan; Lang Lin, Ansys, Cupertino, CA; Jimin Wen, Ansys, San Jose, CA; Preeti Gupta, Ansys, Sunnyvale, CA; Norman Chang, Ansys, San Jose, CA

ROBUST UVM FRAMEWORK FOR DETECTION OF HARDWARE SECURITY VULNERABILITIES FOR SECURITY SUB SYSTEMS AND CRYPTOGRAPHIC IPS

Niharika Sachdeva, Anil Deshpande, Samsung Semiconductor, Bengaluru, India; Arjun Kumar, Samsung Semiconductor, Ghaziabad, India

ENCRYPTION INTEROPERABILITY WITH IEEE 1735

Gangadhar Naik, Glen Crasta, Nikita Tanwar Marvell India Pvt. Ltd., Bengaluru, India

EXECUTIVE PANEL: CREATING ROBUST EDA AND IP ECOSYSTEMS TO STRENGTHEN THE GLOBAL SEMICONDUCTOR SUPPLY CHAIN

Time: 10:30 AM – 12:00 PM
Room: 2012, Level 2
Event Type: Engineering Tracks
Topics Area(s): IP

Organizer(s): Shankar Hemmady, Intel Corporation, Cupertino, CA

Moderator: Rob Aitken, Synopsys

The global structure of the semiconductor supply chain, developed over the past three decades, has enabled the industry to deliver continual leaps in productivity and performance that ultimately made possible the explosion in information technology and digital services. In the past few years, several new factors have emerged that could put the successful continuation of this global model at risk. In this panel, thought leaders from leading semiconductor companies that design or produce ICs and systems, or offer foundry and design services, as well as from EDA and IP suppliers discuss how they collaborate to create robust EDA and IP ecosystems to strengthen the global semiconductor supply chain.

Panelists: Tom Beckley, Cadence Design Systems, Inc., Pittsburgh, PA; Michael Buehler-Garcia, Siemens EDA, Morgan Hill, CA; Michael Campbell, Qualcomm, Encinitas, CA; Rahul Goyal, Intel Corporation, San Francisco, CA; Bari Biswas, Synopsys, Los Altos, CA

COOL INTERCONNECTS FOR COOL ACCELERATORS ON TOP OF CONGESTION FREE PLACE & ROUTE

Time: 10:30 AM – 12:00 PM
Room: 3007, Level 3
Event Type: Research Manuscript
Topics Area(s): In-Package and On-Chip Communication and Networks-on-Chip, Physical Design and Verification, Lithography and DFM, EDA

Chair/Co-Chair: Prabal Basu, Cadence Design Systems; Supriyo Maji, Cadence Design Systems, Inc.

Data transport in advanced system-on-chip architectures significantly contributes to the power consumption and thermal footprint of the overall integrated system. Furthermore, today's VLSI solutions are severely challenged by provisioning congestion free routing and placement. This session will introduce you to latest results on thermal-aware optical-electrical routing codesign flows that minimize power dissipation and nanophotonic technologies for optical neural networks (ONN), as well as software configurable NoCs for wearable AI accelerators and hypergraph neural network models for routability-driven placement. Common denominators are the applicability of electro-optical technologies and machine learning approaches for low power on-chip signal communication as well as intra accelerator interconnects.

THERMAL-AWARE OPTICAL-ELECTRICAL ROUTING CODESIGN FOR ON-CHIP SIGNAL COMMUNICATIONS

Yu-Sheng Lu, Kuan-Cheng Chen, Yu-Ling Hsu, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

POWER-AWARE PRUNING FOR ULTRAFAST, ENERGY-EFFICIENT, AND ACCURATE OPTICAL NEURAL NETWORK DESIGN

Naoki Hattori, Yutaka Masuda, Tohru Ishihara, Nagoya University, Nagoya, Japan; Akihiko Shinya, Masaya Notomi, NTT Basic Research Laboratories, Atsugi, Japan

REACT: A HETEROGENEOUS RECONFIGURABLE NEURAL NETWORK ACCELERATOR WITH SOFTWARE-CONFIGURABLE NOCS FOR TRAINING AND INFERENCE ON WEARABLES

Mohit Upadhyay, Rohan Juneja, Bo Wang, Jun Zhou, Weng-Fai Wong, Li-Shiuan Peh, National University of Singapore, Singapore

LHNN: LATTICE HYPERGRAPH NEURAL NETWORK FOR VLSI CONGESTION PREDICTION

Bowen Wang, Pheng Ann Heng, The Chinese University of Hong Kong, Hong Kong; Guibao Shen, Guangyong Chen, Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China; Dong Li, Jianye Hao, Wulong Liu, Hongzhong Wu, Huawei, Beijing, China; Yu Huang, Huawei, Shenzhen, China; Yibo Lin, Peking University, Beijing, China

HOT APPLICATION AND COOL AUTOMATION FOR QUANTUM COMPUTING

Time: 10:30 AM – 12:00 PM
Room: 3005, Level 3
Event Type: Research Manuscript
Topics Area(s): Quantum Computing, Design

Chair/Co-Chair: Debjyoti Bhattacharjee (imec); Amlan Chakrabarti, University of Calcutta; TBA

This session highlights advances in the applications of quantum computing, covered in the first paper on noise-aware training of quantum neural networks; followed by three research manuscripts covering improved synthesis, mapping and placement methods for quantum circuits.

ROBUSTQNN: NOISE-AWARE TRAINING FOR ROBUST QUANTUM NEURAL NETWORKS

Hanrui Wang, Massachusetts Institute of Technology, Cambridge, MA; Jiaqi Gu, David Z. Pan, The University of Texas at Austin, TX; Yongshan Ding, Yale University, New Haven, CT; Zirui Li, Shanghai Jiao Tong University, Shanghai, China; Frederic Chong, University of Chicago, Chicago, IL; Song Han, Massachusetts Institute of Technology, Storrs, CT

OPTIMIZING QUANTUM CIRCUIT SYNTHESIS FOR PERMUTATIONS USING RECURSIVE METHODS

Cynthia Chen, California Institute of Technology, Pasadena, CA; Bruno Schmitt, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland; Helena Zhang, Lev Bishop, Ali Javadi-Abhari, IBM Thomas J. Watson Research Center, Yorktown Heights, NY

A FAST AND SCALABLE QUBIT-MAPPING METHOD FOR NOISYINTERMEDIATE-SCALE QUANTUM COMPUTERS

Sunghye Park, Minhyuk Kweon, Jae-Yoon Sim, Seokhyeong Kang, Pohang University of Science and Technology, Pohang, South Korea; Daeyeon Kim, POSTECH, Pohang-si, South Kore

OPTIMIZING QUANTUM CIRCUIT PLACEMENT VIA MACHINE LEARNING

Hongxiang Fan, Ce Guo, Wayne Luk, Imperial College London, London, United Kingdom

HYPERDIMENSIONAL COMPUTING FOR MACHINE LEARNING

Time: 10:30 AM – 12:00 PM
Room: 3000, Level 3
Event Type: Research Manuscript
Topics Area(s): AI/ML Security/Privacy, ML Algorithms and Applications, AI

Chair/Co-Chair: Shuhan Zhang, The University of Texas at Austin; TBA

This session presents four papers to design new HyperDimensional Computing techniques for addressing the important machine learning problems and accelerating the computational algorithms

HERO: HESSIAN-ENHANCED ROBUST OPTIMIZATION FOR UNIFYING AND IMPROVING GENERALIZATION AND QUANTIZATION PERFORMANCE

Huanrui Yang, Xiaoxuan Yang, Neil Zhenqiang Gong, Yiran Chen, Duke University, Durham, NC

NEURAL COMPUTATION FOR ROBUST AND HOLOGRAPHIC FACE DETECTION

Mohsen Imani Ali Zakeri, Hanning Chen, University of California, Irvine, CA; TaeHyun Kim, Pusan National University, Pusan, South Korea; Prathyush Poduval, Indian Institute of Science, Bengaluru, India; Hyunsei Lee, Yeseong Kim, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea; Elaheh Sadredini, University of California, Riverside, CA; Farhad Imani, University of Connecticut, Mansfield, CT

FHDNN: COMMUNICATION EFFICIENT AND ROBUST FEDERATED LEARNING FOR AIOT NETWORKS

Rishikanth Chandrasekaran, Kazim Ergun, Jihyun Lee, Dhanush Nanjunda, Jaeyoung Kang, Tajana Rosing, University of California, San Diego, CA

ODHD: ONE-CLASS HYPERDIMENSIONAL COMPUTING FOR OUTLIER DETECTION

Ruixuan Wang, Xun Jiao, Villanova University, Villanova, PA; X. Sharon Hu, University of Notre Dame, Notre Dame, IN

MACHINE LEARNING FOR SYNTHESIS AND SYNTHESIS FOR MACHINE LEARNING

Time: 10:30 AM – 12:00 PM
Room: 3004, Level 3
Event Type: Research Manuscript
Topics Area(s): RTL/Logic Level and High-level Synthesis, AI, EDA

Chair/Co-Chair: Krishnan Sundaresan, Ampere Computing; Sripada Subramanyam, Synopsys

This session shows that logic synthesis and high-level synthesis (on one side) and machine learning (on the other side) are now deeply intertwined: one cannot live without the other.

In the first two papers, graph neural networks support the designers in the optimization process of accelerators, enabling better predictions. The third paper applies graph neural networks to gate-level netlist representation extraction. The last paper shows, instead, how high-level synthesis can help design better accelerators for machine learning.

HIGH-LEVEL SYNTHESIS PERFORMANCE PREDICTION USING GNNS: BENCHMARKING, MODELING, AND ADVANCING

Nan Wu, Yuan Xie, University of California, Santa Barbara, CA; Hang Yang, Nankai University, Tianjin, China; Pan Li, Purdue University, West Lafayatte, IN; Cong Hao, Georgia Institute of Technology, Atlanta, GA

AUTOMATED ACCELERATOR OPTIMIZATION AIDED BY GRAPH NEURAL NETWORKS

Atefeh Sohrabizadeh, Yunsheng Bai, Yizhou Sun, Jason Cong, University of California, Los Angeles, CA

FUNCTIONALITY MATTERS IN NETLIST REPRESENTATION LEARNING

Ziyi Wang, Chen Bai, Zhuolun He, Qiang Xu, Tsung-Yi Ho, Bei Yu, The Chinese University of Hong Kong; Guangliang Zhang, Yu Huang, HiSilicon, Shenzhen, China

EMS: EFFICIENT MEMORY SUBSYSTEM SYNTHESIS FOR SPATIAL ACCELERATORS

Liancheng Jia, Yun Liang, Peking University, Beijing, China; Yuyue Wang, University of California, Los Angeles, CA; Jingwen Leng, Shanghai Jiao Tong University, Shanghai, China

MASK IT UP – KEEPING YOUR SECRETS 6 FEET AWAY

Time: 10:30 AM – 12:00 PM
Room: 3006, Level 3
Event Type: Research Manuscript
Topics Area(s): Hardware Security: Primitives, Architecture, Design & Test, Security

Chair/Co-Chair: Reza Azarderakhsh, FAU & PQSecure; Soheil Salehi, University of California, Davis

Generating and protecting secrets in hardware is of critical importance. The presentations in this session, therefore, provide needed insight in design methodologies and techniques to generate secrets on-chip using physically unclonable functions, to protect secrets against side-channel attacks, and to generate and protect secrets for post-quantum cryptography.

DA PUF: DUAL-STATE ANALOG PUF

Jiliang Zhang, Lin Ding, Zhuojun Chen, Wenshang Li, Hunan University, Changsha, China; Gang Qu, University of Maryland, College Park, MD

PATHFINDER: SIDE CHANNEL PROTECTION THROUGH AUTOMATIC LEAKY PATHS IDENTIFICATION AND OBFUSCATION

Haocheng Ma, Qizhi Zhang, China; Ya Gao, China; Jiaji He, Yiqiang Zhao, Tianjin University, Tianjin, China; Yier Jin, University of Florida, Gainesville, FL

LOCK & ROLL: DEEP-LEARNING POWER SIDE-CHANNEL ATTACK MITIGATION USING EMERGING RECONFIGURABLE DEVICES AND LOGIC LOCKING

Gaurav Kolhe, Tyler Sheaves, Kevin Immanuel Gubbi, Soheil Salehi, Setareh Rafatirad, Houman Homayoun, University of California, Davis, CA; Sai Manoj Pudukotai Dinakarrao, Avesta Sasan, George Mason University, Fairfax, VA

EFFICIENT ACCESS SCHEME FOR MULTI-BANK BASED NTT ARCHITECTURE THROUGH CONFLICT GRAPH

Xiangren Chen, Bohan Yang, Shouyi Yin, Shaojun Wei, Leibo Liu, Tsinghua University, Beijing, China Tsinghua University, Beijing, China; Yong Lu, HeXin Technology Co. , Ltd, Guangzhou, China

NEW NORMAL FOR IN-MEMORY COMPUTING: NOVEL CIRCUITS AND SYSTEMS

Time: 10:30 AM – 12:00 PM
Room: 3002, Level 3
Event Type: Research Manuscript
Topics Area(s): In-memory and Near-memory Computing, Design

Chair/Co-Chair: Mingu Kang, University of California, San Diego; Jungwook Choi, Hanyang University South Korea

While Compute-In-Memory offers significant advantages to improve the energy efficiency of AI hardware, several circuit and system level bottlenecks like peripheral usage, throughput, among others still limit their full potential. The session advances state-of-the-art in this domain by exploring model-aware and data-aware peripheral optimization, investigating novel photonic technologies and hybrid-precision hardware support.

INFOX: AN ENERGY-EFFICIENT RERAM ACCELERATOR DESIGN WITH INFORMATION-LOSSLESS LOW-BIT ADCS

Yintao He, Ying Wang, State Key Laboratory of Computer Architecture, Beijing, China; Songyun Qu, University of Chinese Academy of Science, Beijing, China; Bing Li, Capital Normal University, Beijing, China; Huawei Li, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Xiaowei Li, Chinese Academy of Sciences, Beijing, China

PHANES: RERAM-BASED PHOTONIC ACCELERATORS FOR DEEP NEURAL NETWORKS

Yinyi Liu, Jiaqi Liu, Yuxiang Fu, Shixi Chen, Jiaxu Zhang, Jiang Xu, Hong Kong University of Science and Technology, Hong Kong

CP-SRAM: CHARGE-PULSATION SRAM MARCO FOR ULTRA-HIGH ENERGY-EFFICIENT COMPUTING-IN-MEMORY

He Zhang, Linjun Jiang, Jianxin Wu, Tingran Chen, Junzhan Liu, Wang Kang, Weisheng Zhao, Beihang University, Beijing, China

CREAM: COMPUTING IN RERAM-ASSISTED ENERGY AND AREA-EFFICIENT SRAM FOR NEURAL NETWORK ACCELERATION

Liukai Xu, Songyuan Liu, Zhi Li, Dengfeng Wang, Yanan Sun, Weifeng He, Shanghai Jiao Tong University, Shanghai, China; Yiming Chen, Xueqing Li, Tsinghua University, Beijing, China; Shi Xu, South China Normal University, Guangzhou, China

WHAT IS THE FUTURE FOR OPEN-SOURCE EDA?

Time: 10:30 AM – 12:00 PM
Room: 3001, Level 3
Event Type: Research Panel
Topics Area(s): EDA

Organizer(s): Andrew Kahng, University of California, San Diego, CA

Moderator: Andreas Olofsson, Zero ASIC, Boston, MA

It has been four years since the DARPA IDEA and POSH programs were launched as part of the U.S. Electronics Resurgence Initiative. The 22 projects are now ending (Summer 2022). Three years ago, a DAC-2019 panel session ended with the audience seeing EDA open-sourcing more as "dawn of a golden age" than as "pipe dream". As government funding draws to a close, the urgency of transition to sustainable business models has grown. Classically, venture-funded EDA startups have always faced many IP and channel barriers, due to the industry's Big-3 structure. An open-source business model for EDA software has never been proven. And, there are concerns about EDA technology vis-a-vis geopolitical issues such as national security. On the other hand, growing a domestic VLSI design and IC innovation ecosystem, including workforce development and democratization of access, is a focus for multiple regions across the globe. With this backdrop, the panel will broadly illuminate the topic of "What is the future for open-source EDA?"

Panelists: David Byrd, Blueyard Capital, Shirley, Canada; Peter Gadfort, Army Research Labs, Washington, DC; Noel Menezes, Intel Corporation, Hillsboro, OR; Chuck Alpert, Cadence Design Systems, Inc., Austin, TX; Mamta Bansal, Qualcomm, San Diego, CA

MICROELECTRONICS AND COMPUTING IN 2030: A CO-DESIGN PERSPECTIVE FROM THE SRC/ DARPA JUMP CENTER PROGRAM

Time: 10:30 AM – 12:00 PM
Room: 3003, Level 3
Event Type: Special Session (Research)

Organizer(s): Timothy Green, SRC, Durham, NC

The Joint University Microelectronics Program ("JUMP") is a consortium of research centers funded by the Semiconductor Research Corporation (SRC) and Defense Advanced Research Projects Agency (DARPA). The goal of these collaborative, multi-university efforts is to substantially increase the performance, efficiency, and capabilities of broad classes of electronics and computing systems for both commercial and military applications in the 2030 timeframe. In JUMP's fifth and final year, this session brings together leaders from three JUMP centers to present a vertical view of cross-layer co-design – from devices to circuits, architecture and systems - and the key advances they have delivered, challenges, and perspectives to inform the road ahead. We will start with the Applications and Systems-Driven Center for Energy-Efficient Integrated NanoTechnologies (ASCENT) center, which aims to deliver the next generation of materials and device advances. Next, the Applications Driving Architectures (ADA) center will discuss their efforts towards streamlining and democratizing the design and manufacturing of next-generation computing systems. Finally, the Center for Brain-Inspired Computing (C-BRIC) will discuss advances in cognitive algorithms, hardware fabrics and applications. The session will conclude with a joint Q&A that will explore co-design challenges and opportunities across the stack.

A SYSTEMS DRIVEN APPROACH TO SEMICONDUCTOR RESEARCH AND INNOVATION

Suman Datta, University of Notre Dame, Notre Dame, IN; Sayeef Salahuddin, Ramesh Ramamoorthy, University of California, Berkeley, CA; Darrell Schlom, Cornell University, Ithaca, NY; Madhavan Swaminathan, Arijit Raychowdhury, Georgia Institute of Technology, Atlanta, GA

ADA, THE CENTER FOR APPLICATIONS DRIVING ARCHITECTURES: ACCOMPLISHMENTS AND VISION FORWARD

Valeria Bertacco, University of Michigan, Ann Arbor, MI

A CROSS-LAYER APPROACH TO COGNITIVE COMPUTING

Kaushik Roy, Purdue University, West Lafayette, IN

OPEN ARCHITECTURES TO ACCELERATE INDUSTRY GROWTH

Time: 11:30 AM – 12:30 PM
Room: DAC Pavilion, Level 2 Exhibit Hall
Event Type: Tech Talk
Topics Area(s):

There is an exponential growth in demand for workload specific compute in artificial intelligence (both training and inference), network and storage acceleration, 5G/6G edge servers, media acceleration, high performance compute (ex. Vector processing), graphics, and gaming. The industry is facing many architectural challenges to improve cost, performance, power, security, etc. to meet this demand. The solution will require a broad alignment around standardized open architectures from the ISA to the SoC level, alignment of the IP supplier ecosystem, cooperation in standards, new EDA tools, and support from foundries and packaging suppliers. These open architectures will need to support the established and growing SW ecosystem around x86 while seamlessly blending in RISC-V as the new open ISAs at the center of domain specific computation. RISC-V as a new open architecture will need industry cooperation to mature the ISA, the SoC silicon architecture, the platform architecture, and the open-source software stack. These open architectures must embrace disaggregation. The new disaggregated architectures will need new packaging technologies to be co-optimized with interconnect technologies with full support from Foundries and the IP Ecosystem. New EDA tools will be needed to optimize the overall silicon partitioning and accelerate the development cycles of each partition. This talk will highlight some of the recent progress in the industry, and a call to collaborate on enabling and supporting these new architectures.

Speaker: Bob Brennan, Intel Corporation, Santa Clara, CA

BUILDING RESILIENCY– THE NEXT IMPERATIVE IN DESIGN

Time: 1:00 PM – 1:45 PM
Room: DAC Pavilion, Level 2 Exhibit Hall
Event Type: SKYTalk
Topics Area(s): Design

Innovations in the world of design work toward ensuring that technology continues to deliver smaller and faster. This has included new methods that are beyond shrinking the transistors as Moore's Law is slowing down. Testing and Design for Test must keep up to ensure that the designs created are fully testable to prevent costly test escapes. In addition to technology, areas that require intermittent testing such as automotive and large data centers to support the cloud must also be addressed. Teresa will illustrate how some of the trends of test may be examples of how resiliency on silicon will evolve in the industry.

Speaker: Teresa McLaurin, Arm Ltd., Austin, TX

MACHINE LEARNING AND EDA: THE PRODUCTIVITY CYCLE

Time: 1:30 PM – 3:00 PM
Room: 2008, Level 2
Event Type: Engineering Tracks
Topics Area(s): AI, Back-End Design

Chair/Co-Chair: Nararajan Viswanathan, Cadence Design System

Chip design and fabrication is at a crucial stage with increasing complexity, customization, and constraints. Innovative tools and ideas are critical for the development of next generation EDA tools. Machine Learning is one such tool that both contributes to better EDA tools and simultaneously benefits from the increased computing power that these EDA tools can make available. This session includes two talks that discuss how the use of ML enhances physical design and fabrication. The third talk of the session focuses on how ML algorithms can be accelerated on heterogenous compute systems.

Presenters: Sung Kyu Lim, Georgia Institute of Technology, Atlanta, GA; Ivan Kissiov, Siemens EDA, Palo Alto, CA; Ravikumar Chakaravarthy, AMD, Chennai, India

ML FOR VERIFICATION: DOES IT WORK OR DOESN'T IT?

Time: 1:30 PM – 3:00 PM
Room: 2010, Level 2
Event Type: Engineering Tracks
Topics Area(s): Front-End Design

Chair/Co-Chair: Anupam Bakshi, Agnisys

Organizer: Avi Ziv, IBM, Haifa, Israel

Moderator: Brian Bailey, Semiconductor Engineering, Beaverton, OR

The ML contribution to verification today is limited to point solutions for internal engines. The goal of the panel is to discuss why there are no major breakthrough in the use of ML in functional verification and what can be done to change this picture. AI in general and ML specifically are hot research topics in the EDA research community. The past few years saw many tools, technologies, and methodologies that utilize the power of AI and ML influence EDA in many areas, such as place and route, timing closure, and synthesis. One area that is almost missing in this picture is functional verification. On the face of it, functional verification is a natural candidate for massive use of ML technologies. The verification process produces large amount of data that can be used to train ML-based solutions. Moreover, the highly automated verification process contains several manual bottlenecks that can benefit from ML. Examples of such bottlenecks are coverage closure and debug/triage.

Panelists: Clark Barrett, Stanford University, Stanford, CA; Erik Berg, Microsoft, Portland, OR; Shobha Vasudevan, Google, Urbana, IL; Sandeep Srinivasan, VerifAI, San Francisco, CA; Avi Ziv, IBM, Haifa, Israel

THE INTERDEPENDENCE BETWEEN ML/AI AND CHIP DESIGN AUTOMATION

Time: 1:30 PM – 3:00 PM
Room: 2012, Level 2
Event Type: Engineering Tracks
Topics Area(s): IP

Chair/Co-Chair: Navid Farazmand (Intel Corporation)

The ever-increasing popularity and practical applications of Machine Learning and AI seen within the past decade was unlocked through unprecedented computational capabilities of modern GPUs. Now, AI and ML are increasingly being tapped into for handling some of the most complex steps in designing state-of-the-art chips to improve performance, quality, and time to market, as evident from the keynote presentations in DAC58.

This session includes presentations focusing on addressing the requirements of memory-intensive use cases (multimedia, graphics, AI training and inference) through maximizing the NOC utilization, as well as in-memory-computation hardware. The session also includes presentations using AI/ML to enhance layout and design verification quality and turn-around time. Finally, this session includes submissions aiming to reduce design complexity and turnaround time by generalizing and automating ISO compliance verification IP and module interface design.

VARIATION-AWARE DESIGN VERIFICATION FOR AUTOMOTIVE SEMICONDUCTOR IP

Adam Golda, Silicon Creations Inc, Krakow, Poland; Maysam Ghovanloo, Silicon Creations Inc, Atlanta, GA; Amy Pitman, Mike Sheinin, Siemens EDA, Saskattoon, Canada; Randy Caplan, Silicon Creations Inc, Suwanee, Country; Wei Tan, Siemens EDA, Fremont, CA

EFFICIENT USE OF ON-LINE LOGICBIST TO ACHIEVE ASIL B IN A GPU IP

Lee Harrison, Siemens EDA, London, United Kingdom; Antonio Priore, Arm Ltd., Cottenham, United Kingdom

SHARED VIRTUAL OUTPUT QUEUING: MAXIMIZING NOC SWITCH UTILIZATION

Seongmin Jo, Wooil Kim, Samsung Electronics, Hwaseong, South Korea

A 28NM FULL-DIGITAL PROCESSING IN MEMORY SYSTEM FOR ULTRA-HIGH-EFFICIENCY APPLICATIONS

Yue Yang, Yaojun Zhang, Pimchip Technology, Beijing, China; Guang Jiang, Pimchip Technology, Hong Kong, Hong Kong; Jing Wang, Pimchip Technology, Fremont, CA

FLEXIBLE ACCELERATOR DESIGN WITH PROGRAMMATIC INTERFACE TYPES

Hari Angepat, Microsoft, Redmond, WA; Gwen Diebold, Microsoft, Seattle, WA

FANTASTIC SOCS AND WHAT TO LEARN!

Time: 1:30 PM – 3:00 PM
Room: 3007, Level 3
Event Type: Research Manuscript
Topics Area(s): System-on-Chip Design Methodology, EDA

Chair/Co-Chair: Shobha Vasudevan, Google, University of Illinois at Urbana-Champaign; Hui Zhao, University of North Texas

This session presents four papers on the state-of-the-art for system-on-chip (SoC) design, modeling, mapping, and optimization. The first paper develops a novel cost model to explore emerging multi-chiplet systems, followed by the second paper that proposes a scalable compiler-based approach for mapping complex loop kernels on CGRAs. The third paper develops a fast parameter tuning framework to quickly find the optimal configurations in a system with massive design space, followed by the fourth paper that develops a methodology for effectively mapping DSL applications to hardware accelerators.

CHIPLET ACTUARY: A QUANTITATIVE COST MODEL AND MULTI-CHIPLET ARCHITECTURE EXPLORATION

Yinxiao Feng, Kaisheng Ma, Tsinghua University, Beijing, China

PANORAMA: DIVIDE-AND-CONQUER APPROACH FOR MAPPING COMPLEX LOOP KERNELS ON CGRA

Dhananjaya Wijerathne, Zhaoying Li, Thilini Bandara, Tulika Mitra, National University of Singapore, Singapore

A FAST PARAMETER TUNING FRAMEWORK VIA TRANSFER LEARNING AND MULTI-OBJECTIVE BAYESIAN OPTIMIZATION

Zheng Zhang, Jiaxin Huang, Southeast University, NanJing, China; Tinghuan Chen, The Chinese University of Hong Kong, Hong Kong; Meng Zhang, Southeast University, Wuhan, China

PRIMAX: MAXIMIZING DSL APPLICATION PERFORMANCE WITH SELECTIVE PRIMITIVE ACCELERATION

Nicholas Wendt, Todd Austin, Valeria Bertacco, University of Michigan, Ann Arbor, MI

FASTER AND STRONGER: AI ACCELERATION AND RESILIENCE

Time: 1:30 PM – 3:00 PM
Room: 3005, Level 3
Event Type: Research Manuscript
Topics Area(s): AI/ML Design: System and Platform, Design

Chair/Co-Chair: TBA

ACCELERATING AND PRUNING CNNS FOR SEMANTIC SEGMENTATION ON FPGA

Pierpaolo Mori, Claudio Passerone, Politecnico di Torino, Torino, Italy; Manoj Rohit Vemparala, Alexander Frickenstein, Lukas Frickenstein, Naveen Shankar Nagaraja, BMW Group, Munich, Germany; Nael Fasfous, Saptarshi Mitra, Sreetama Sarkar, Walter Stechele, Technische Universität München, Munich, Germany; Domenik Helms, OFFIS Institute for Computer Science, Oldenburg, Germany

SOFTSNN: LOW-COST FAULT TOLERANCE FOR SPIKING NEURAL NETWORK ACCELERATORS UNDER SOFT ERRORS

Rachmad Vidya Wicaksana Putra, Muhammad Abdullah Hanif, Technische Universität Wien, Vienna, Austria; Muhammad Shafique, New York University, Abu Dhabi, United Arab Emirates

A JOINT MANAGEMENT MIDDLEWARE TO IMPROVE TRAINING PERFORMANCE OF DEEP RECOMMENDATION SYSTEMS WITH SSDS

Chun-Feng Wu, Gu-Yeon Wei, David Brooks, Harvard University, Cambridge, MA; Carole-Jean Wu, Meta, Cambridge, MA

THE LARGER THE FAIRER? SMALL NEURAL NETWORKS CAN ACHIEVE FAIRNESS FOR EDGE DEVICES

Yi Sheng, Weiwen Jiang, George Mason University, Fairfax, VA; Junhuan Yang, Lei Yang, University of New Mexico, Albuquerque, NM; Yawen Wu, Jingtong Hu, University of Pittsburgh, Pittsburgh, PA; Kevin Mao, North Allegheny Senior High School, Wexford, AL; Yiyu Shi, University of Notre Dame, Notre Dame, IN

ITERATE AND SCALE: DESIGNING STRONGER AND SAFER EMBEDDED SYSTEMS

Time: 1:30 PM – 3:00 PM
Room: 3004, Level 3
Event Type: Research Manuscript
Topics Area(s): Embedded System Design Methodologies, Time-Critical System Design, Embedded Systems, RISC-V

Chair/Co-Chair: TBA

This session focuses on exciting new ways to effectively analyze and design high-performance and low-power embedded systems. The first paper proposes a highly portable and feature-rich ISA Extensions interface that supports custom control flow, decoupled execution, multi-cycle instructions, and memory transactions in RISC-V processors. The second paper proposes a methodology that enables automated safety analysis in the design of safety-critical systems. The third paper proposes a custom symbolic simulator to enable hardware-software co-analysis and the development of hardware and software optimizations for low-power embedded systems.

SCAIE-V: AN OPEN-SOURCE SCALABLE INTERFACE FOR ISA EXTENSIONS FOR RISC-V PROCESSORS

Mihaela Damian, Julian Oppermann, Christoph Spang, Andreas Koch, Technische Universität Darmstadt, Germany

A SCALABLE SYMBOLIC SIMULATION TOOL FOR LOW POWER EMBEDDED SYSTEMS

Subhash Sethumurugan, Shashank Hegde, John Sartori, University of Minnesota, Minneapolis, MN; Hari Cherupalli, Synopsys, Sunnyvale, CA

DESIGNING CRITICAL SYSTEMS WITH ITERATIVE AUTOMATED SAFETY ANALYSIS

Ran Wei, Dalian University of Technology, Dalian, China; Zhe Jiang, Arm Ltd., Sheffield, United Kingdom; Xiaoran Guo, Specialized Services Research Department, Beijing, China; Haitao Mei, Facebook, London, United Kingdom; Athanasios Zolotas, Tim Kelly, University of York, United Kingdom

NEW ALGORITHM DESIGN AND SYSTEM OPTIMIZATION FOR MACHINE LEARNING METHODS

Time: 1:30 PM – 3:00 PM
Room: 3000, Level 3
Event Type: Research Manuscript
Topics Area(s): ML Algorithms and Applications, AI

Chair/Co-Chair: Wei Ye, Facebook; Zhuoran Zhao, Facebook

This session presents four papers to develop new algorithms and system optimization approaches for accelerating the computations of machine learning methods.

EFFICIENT ENSEMBLES OF GRAPH NEURAL NETWORKS

Amrit Nagarajan, Jacob Stevens, Anand Raghunathan, Purdue University, West Lafayette, IN

SIGN BIT IS ENOUGH: A LEARNING SYNCHRONIZATION FRAMEWORK FOR MULTI-HOP ALL-REDUCE WITH ULTIMATE COMPRESSION

Feijie Wu, Song Guo, Jie Zhang, The Hong Kong Polytechnic University, Hong Kong; Shiqi He, The University of British Columbia, Vancouver, Canada; Zhihao Qu, Hohai University, Nanjing, China; Haozhao Wang, Huazhong University of Science and Technology, Wuhan, China; Weihua Zhuang, University of Waterloo, Waterloo, Canada

GLITE: A FAST AND EFFICIENT AUTOMATIC GRAPH-LEVEL OPTIMIZER FOR LARGE-SCALE DNNS

Min Peng, Jiaqi Li, Meizheng Peng, Qingan Li, Wuhan, Mengting Yuan, Wuhan University, Wuhan, China

CONTRASTIVE QUANT: QUANTIZATION MAKES STRONGER CONTRASTIVE LEARNING

Yonggan Fu, Qixuan Yu, Xu Ouyang, Yingyan Lin, Rice University, Houston, TX; Meng Li, Vikas Chandra, Facebook, San Francisco, CA

OPTIMIZING NEURAL NETWORK HARDWARE: SPARSITY, REUSE AND SYSTEM

Time: 1:30 PM – 3:00 PM
Room: 3002, Level 3
Event Type: Research Manuscript
Topics Area(s): AI/ML Design: Circuits and Architecture, Design

Chair/Co-Chair: Linghao Song, UCLA; TBA

The performance of AI accelerators is determined by many factors, ranging from algorithm to architecture to system. This section focus on efficient techniques to optimize the performance of deep neural network hardware, from the perspective of sparsity, data reuse and system integration.

SERPENS: A HIGH BANDWIDTH MEMORY BASED ACCELERATOR FOR GENERAL-PURPOSE SPARSE MATRIX-VECTOR MULTIPLICATION

Linghao Song, Yuze Chi, Licheng Guo, Jason Cong, University of California, Los Angeles, CA

AN ENERGY-EFFICIENT SEIZURE DETECTION PROCESSOR USING EVENT-DRIVEN MULTI-STAGE CNN CLASSIFICATION AND SEGMENTED DATA PROCESSING WITH ADAPTIVE CHANNEL SELECTION

Jiahao Liu, Zirui Zhong, Yong Zhou, Hui Qiu, Jianbiao Xiao, Jiajing Fan, Zhaomin Zhang, Sixu Li, Yiming Xu, Siqi Yang, Shuisheng Lin, Liang ChangJun Zhou, University of Electronic Science and Technology of China, Chengdu, China, Weiwei Shan, Southeast University, Nanjing, China

PATTERNET: EXPLORE AND EXPLOIT FILTER PATTERNS FOR EFFICIENT DEEP NEURAL NETWORKS

Behnam Khaleghi, Uday Mallappa, Haichao Yang, Monil Shah, Jaeyoung Kang, Tajana Rosing, University of California, San Diego, CA; Duygu Yaldiz, Bilkent University, Ankara, Turkey;

E^{2}SR: AN END-TO-END VIDEO CODEC ASSISTED SYSTEM FOR SUPER RESOLUTION ACCELERATION

Zhuoran Song, Naifeng Jing, Xiaoyao Liang, Shanghai Jiao Tong University, Shanghai, China; Zhongkai Yu, Chinese Academy of Sciences, Beijing, China

SIDE CHANNELS GO MAINSTREAM !!

Time: 1:30 PM – 3:00 PM
Room: 3006, Level 3
Event Type: Research Manuscript
Topics Area(s): Embedded and Cross-Layer Security, Security

Chair/Co-Chair: Hamed Okhravi, Massachusetts Institute of Technology; Satwik Patnaik, Texas A&M University

This session explores novel side channels in processors and systems and presents an accelerator for homomorphic encryption.

MATCHA: A FAST AND ENERGY-EFFICIENT ACCELERATOR FOR FULLY HOMOMORPHIC ENCRYPTION OVER THE TORUS

Lei Jiang, Qian Lou, Nrushad Joshi, Indiana University, Bloomington, IN

VIRTEE: A FULL BACKWARD-COMPATIBLE TEE WITH NATIVE LIVE MIGRATION AND SECURE I/O

Jianqiang Wang, Pouya Mahmoody, Ferdinand Brasser, Patrick Jauernig, Ahmad-Reza Sadeghi, Technische Universität Darmstadt, Germany; Donghui Yu, Dahan Pan, Yuanyuan Zhang, Shanghai Jiao Tong University, Shanghai, China

APPLE VS. EMA: ELECTROMAGNETIC SIDE CHANNEL ATTACKS ON APPLE CORECRYPTO

Gregor Haas, Aydin Aysu, North Carolina State University, Raleigh, NC

TACKLING TRUST THROUGH VERIFICATION AND ASSESSMENT: WISHFUL THINKING OR INEVITABLE REALITY?

Time: 1:30 PM – 3:00 PM
Room: 3001, Level 3
Event Type: Research Panel
Topics Area(s): Security

Organizer(s): Sandip Ray, University of Florida, Gainesville, FL; Saverio Fazzari, DARPA, Clarksville, MD

Moderator: Rob Aitken, Arm Ltd., San Jose, CA

Microelectronics trust assurance challenges have transformed over the last decade, with exploitable vulnerabilities arising from explosion in design complexity one the one hand, and dependency on an increasingly complex, global supply chain on the other. The research community has been developing increasingly sophisticated mitigation technologies in response, ranging from architecture to physical design, packaging, and fabrication strategies. An obvious upshot is that it is now more difficult than ever to develop objective technologies for assessing the security of a finished product. Furthermore, security does not come for free. The additional complexity introduced for security has ramifications to functional correctness, performance, energy consumption, etc., all of which need to be accounted for in verification. This panel will examine the crucial challenge of security assessment and verification of modern microelectronics systems under the evolving zero-trust model. Current practices, their strengths and limitations in the new security ecosystem, emergent approaches to address these limitations will be discussed.

Panelists: Swarup Bhunia, University of Florida, Gainesville, FL; James Wilson, DARPA, Arlington, VA; Mark Labbato, Booz Allen Hamilton (BAH), Cincinnati, OH; Shobha Vasudevan, University of Illinois at Urbana-Champaign, Urbana, IL

WOMEN IN ENGINEERING: TRANSFORMING THE INNOVATION PARADIGM

Time: 2:00 PM – 2:45 PM
Room: DAC Pavilion, Level 2 Exhibit Hall
Event Type: DAC Pavilion Panel
Topics Area(s): EDA

Moderator: Ann Steffora Mutschler, Executive Editor/EDA, Semiconductor Engineering

Panelists: Radhika Shankar, Group Director, Synopsys; Geeta Pyne, Chief Enterprise Architect, Intuit; Sherry Hess, Cadence; Raji Arasu, CTO, Autodesk

Abstract: In the past decade, women have made enormous strides in the engineering workforce but much more opportunity lies ahead. What are the positive outcomes that women engineers bring to design and development? What hurdles remain? What potential lies ahead? How do we encourage and grow the next generation of women engineers? Join us for an insightful panel with key women in engineering who will discuss the challenges and opportunities they've experienced in their careers, what inspires them, and where they see the opportunities and growth in the future for women in engineering.

HANDS-ON LAB: BUILD A HYBRID BURST TO CLOUD ENVIRONMENT WITH NETAPP "DESIGN ANYWHERE" CLOUD-BURSTING EDA WORKLOADS WITH BI-DIRECTIONAL CACHING OF JOB DATA

Time: 2:15 PM – 5:15 PM
Room: Design on Cloud Pavilion, Level 2 Exhibit Hall
Event Type: Design on Cloud Training
Topics Area(s):

The ability to Burst EDA workloads to the Cloud is quickly becoming a requirement for Semiconductor companies. 5 and 3nm design processes require as much as 4-6x more compute and 4x more storage than prior project placing strains on existing engineering resources. The demands of new AI driven EDA workflows make the availability of on-demand Cloud scale a necessity during peak design periods. Hybrid Cloud for EDA workflows, enabled by NetApp's ONTAP data management platform and NetApp's Cloud Manager, provides a fast, seamless, no-scripting required way to get your design data into the cloud, where you can then take advantage of Cloud Scale computing. Get Hands-on: You will get your own AWS hybrid on-prem lab-on-demand environment. You will use NetApp's cloud manager to create a Cloud Volume ONTAP (CVO) storage management instance in AWS. You will then connect the CVO instance to the On-Prem ONTAP instance in a peering relationship. You will then create a FlexCache volume in AWS, instantly replicating EDA Tools and Libraries into the Cloud. You will get to experience first-hand how easy and instantaneous large volumes of design data can be replicated into the cloud - without the need for scripting or other automation tools for synchronizing data. You will then create a "Reverse Cacheâ€ replicating a EDA Scratch volume in AWS, back to the on-prem datacenter. The reverse cache will demonstrate how easy it is for design teams to debug cloud-based burst workloads, on-prem without having to connect to the cloud Join NetApp and AWS to learn how Hybrid Cloud works and how easy it can be to enable and migrate to Hybrid Cloud for your most demanding EDA workflows.

Presenter: Michael Johnson, NetApp, San Francisco, CA

WHAT CAN EDA AND THE ELECTRONICS ECOSYSTEM DO FOR GREENER ELECTRONICS TO SAVE THE PLANET?

Time: 3:00 PM – 3:45 PM
Room: DAC Pavilion, Level 2 Exhibit Hall
Event Type: DAC Pavilion Panel
Topics Area(s): EDA

Moderator: Frank Schirrmeister, Cadence Design Systems, Inc., San Jose, CA

We are in the midst of the roaring 20s of hyperconnectivity, fueling a golden era for semiconductors and electronic systems. We are developing 5G, hyperscale computing, autonomy & electrification in automotive, the industrial IoT, and AI/ML. From 2010 to 2018, global data center energy consumption "only" grew a surprising 6%, while workloads increased more than six-fold, internet traffic increased 10-fold, and storage capacity rose by 25X. But what will the future hold? Sustainability has become much more than lip service. Gen Z already has the largest share of the world's population and has made it crystal clear that sustainability is critical to our future and will drive their purchasing decisions. This panel will discuss the state and role of sustainability in EDA and electronics today and discuss key trends that will shape the next decade. What are the most significant areas to focus on? Will advances in semiconductor technology, processor, memory and system architectures, and electronic design automation keep power and energy consumption in check while providing the advances in performance that the era of hyperconnectivity demands? Can we transition to electric cars fast enough? Will consumer experiences in AR/VR be possible while maintaining sustainability? How central will the IoT be for the enablement of sustainable engineering?

Panelists: Dipti Vachani, Arm; Jennifer Huffstetler, Intel; David Pellerin, Amazon Web Services; Dharmesh Jani, Meta; Vojin Zivojnovic, Aggios

NEW DIRECTIONS IN SILICON SOLUTIONS

Time: 3:30 PM – 5:00 PM
Room: 2008, Level 2
Event Type: Engineering Tracks
Topics Area(s): Back-End Design

Chair/Co-Chair: Sashi Obilsetty, Synopsys

New areas of solutions are cropping up to support ever increasing silicon content in solutions all around us. In this session we will look at some solutions that are coming up to enable silicon design, security, reliability and performance.

Presenters: Yervant Zorian, Synopsys, Fremont, CA; Sudip Nag, Xilinx, San Jose, CA; Norman Chang, Ansys, San Jose, CA; Abhishek Joshi, INVBE

FUTURE PROOFING ELECTRONICS WITH SYSTEM BIOMETRICS

Time: 3:30 PM – 5:00 PM
Room: 2010, Level 2
Event Type: Engineering Tracks
Topics Area(s): IP

Chair/Co-Chair: Marc Hutner, proteanTec

How do you design systems that support high up-time, diagnosability and resilience to future requirements? How does the need for lifecycle data change how we design and bring to market mission critical systems? Are there particular segments that will require new levels of system visibility at new product introduction or in-field use? We will explore the gaps in existing approaches and highlight how new techniques in system biometrics will address the emerging problems. We will look at the need for increased data at test insertions, system integration and in-field usage. In this session we will explore these questions with three industry experts in System Architecture, DFT and Test.

Presenters: Marc Hutner, proteanTecs, Toronto, Canada; Harry Chen, MediaTek, Hsinchu City, Taiwan; Zoe Conroy, Cisco, San Jose, CA

DO NOT FORGET THE SOFTWARE: BARE METAL NEURAL ACCELERATION IS NO FUN WITHOUT IT

Time: 3:30 PM – 5:30 PM
Room: 3002, Level 3
Event Type: Research Manuscript
Topics Area(s): AI/ML Design: Circuits and Architecture, Design

Chair/Co-Chair: Iraklis Anagnostopoulos, Southern Illinois University; Xiaoxiao Liu, AMD

This session presents various design automation and optimization frameworks for energy efficient and high-performance neural network applications. The papers of this session cover among others, techniques used during building the models, such as conversion aware training and model compression optimization methods. Further, various design automation approaches for ReRAM-based in-memory computing and mapping of weights in non-volatile memory for in-memory accelerators, are presented, some emphasizing their usefulness in multi-task deep neural networks.

ALGORITHM/ARCHITECTURE CO-DESIGN FOR ENERGY-EFFICIENT ACCELERATION OF MULTI-TASK DNN

Jaekang Shin, Seungkyu Choi, Jongwoo Ra, Lee-Sup Kim, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea

EBSP: EVOLVING BIT SPARSITY PATTERNS FOR HARDWARE-FRIENDLY INFERENCE OF QUANTIZED DEEP NEURAL NETWORKS

Fangxin Liu, Wenbo Zhao, Zongwu Wang, Qidong Tang, Yongbiao Chen, Zhezhi He, Naifeng Jing, Xiaoyao Liang, Li Jiang, Shanghai Jiao Tong University, Shanghai, China

A TIME-TO-FIRST-SPIKE CODING AND CONVERSION AWARE TRAINING FOR ENERGY-EFFICIENT DEEP SPIKING NEURAL NETWORK PROCESSOR DESIGN

Dongwoo Lew, Kyungchul Lee, Jongsun Park, Korea University, Seoul, South Korea

XMA: A CROSSBAR-AWARE MULTI-TASK ADAPTION FRAMEWORK VIA SHIFT-BASED MASK LEARNING METHOD

Fan Zhang, Li Yang, Jian Meng, Jae-sun Seo, Yu Cao, Deliang Fan, Arizona State University, Tempe, AZ

SWIM: SELECTIVE WRITE-VERIFY FOR COMPUTING-IN-MEMORY NEURAL ACCELERATORS

Zheyu Yan, X. Sharon Hu, Yiyu Shi, University of Notre Dame, Notre Dame, IN

FAST AND FIDUCIUS: ACHIEVING EFFICIENT AUTONOMY WITH CONFIDENCE

Time: 3:30 PM – 5:30 PM
Room: 3000, Level 3
Event Type: Research Manuscript
Topics Area(s): Autonomous Systems (Automotive, Robotics, Drones), Autonomous Systems

Chair/Co-Chair: Susmit Jha, SRI International; Lulu Chan, NXP Semiconductors

Autonomous systems need to be trusted on one hand, and efficient, i.e., achieving high performance with limited resources, on the other, to be widely deployed. This session addresses a number of fundamental problems in autonomy along these two directions. The first three papers focus on perception efficiency and safety. The fourth paper addresses critical timing aspects in ROS2 and provides timing predictability for robotics. The last paper targets electric systems and investigates battery voltage prediction. The theoretical breakthroughs of these papers could have significant impacts in automotive, robotics, and drone applications.

ENABLING EFFICIENT DEEP CONVOLUTIONAL NEURALNETWORK-BASED SENSOR FUSION FOR AUTONOMOUSDRIVING

Xiaoming Zeng, Zhendong Wang, Yang Hu, The University of Texas at Dallas, TX

ZHUYI: PERCEPTION PROCESSING RATE ESTIMATION FOR SAFETY OF AUTONOMOUS VEHICLES

Yu-Shun Hsiao, Vijay Janapa Reddi, Harvard University, Cambridge, MA; Siva Kumar Sastry Hari, Timothy Tsai, NVIDIA, Santa Clara, CA; Michal Filipiuk, Vasu Singh, NVIDIA, Munich, Germany; Michael Sullivan, Stephen W. Keckler, NVIDIA, Austin, TX

PROCESSING-IN-SRAM ACCELERATION FOR ULTRA-LOW POWER VISUAL 3D PERCEPTION

Yuquan He, Gangliang Lin, Chinese Academy of Sciences, Beijing, China; Songyun Qu, University of Chinese Academy of Science, Beijing, China; Ying Wang, State Key Laboratory of Computer Architecture, Beijing, China; Cheng Liu, Lei Zhang, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

RESPONSE-TIME ANALYSIS FOR DEADLINE-BASED SCHEDULING OF ROS2

Abdullah Al Arafat, Sudharsan Vaidhun, Kurt Wilson, Zhishan Guo, University of Central Florida, Orlando, FL; Jinghao Sun, Dalian University of Technology, Dalian, China

VOLTAGE PREDICTION OF DRONE BATTERY REFLECTING INTERNAL TEMPERATURE

Jiwon Kim, Seunghyeok Jeon, Jaehyun Kim, Hojung Cha, Yonsei University, Seoul, South Korea

ORDERS OF MAGNITUDE ACCELERATION

Time: 3:30 PM – 5:30 PM
Room: 3005, Level 3
Event Type: Research Manuscript
Topics Area(s): SoC, Heterogeneous, and Reconfigurable Architectures, Design

Chair/Co-Chair: Albert Bosio, Lyon Institute of Nanotechnology, École Centrale de Lyon; David Novo, CNRS, LIRMM, University of Montpellier

The session starts with a near-storage accelerator for mass spectrum clustering. It continues with a high-throughput and scalable data compression architecture targeted for FPGA-enabled data centers. The third presentation accelerates transformers by using an evolutionary algorithm and exploiting sparsity. Afterwards, a fast and energy-efficient EMVS accelerator is introduced that realizes the most critical and time-consuming stages on an FPGA. The final two presentations target CGRAs with an ML-based method to accelerate the mapping of loops onto CGRAs by an order of magnitude without compromising the mapping quality, and an execution model and co-designed CGRA design that supports fine-/coarse-grained parallelism for operators/tasks, respectively.

A NEAR-STORAGE FRAMEWORK FOR BOOSTED DATA PREPROCESSING OF MASS SPECTRUM CLUSTERING

Weihong Xu, Jaeyoung Kang, Tajana Rosing, University of California, San Diego, La Jolla, CA

METAZIP: A HIGH-THROUGHPUT AND EFFICIENT ACCELERATOR FOR DEFLATE

Ruihao Gao, Yewen Li, Guangming Tan, Chinese Academy of Sciences, Beijing, China; Xueqi Li, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Xun Wang, China University of Petroleum, Qingdao, China

ENABLING FAST UNCERTAINTY ESTIMATION: ACCELERATING BAYESIAN TRANSFORMERS VIA ALGORITHMIC AND HARDWARE OPTIMIZATIONS

Hongxiang Fan, Wayne Luk, Imperial College London, United Kingdom; Martin Ferianc, University College, London, United Kingdom

EVENTOR: AN EFFICIENT EVENT-BASED MONOCULAR MULTI-VIEW STEREO ACCELERATOR ON FPGA PLATFORM

Mingjun Li, Jianlei Yang, Yingjie Qi, Yuhao Yang, Beihang University, Beijing, China; Meng Dong, Xidian University, Xi'an, China; Runze Liu, Beijing Real Imaging Medical Technology Co., Ltd., Beijing, China; Weitao Pan, Xidian University, Xi'an, China; Bei Yu, The Chinese University of Hong Kong, Hong Kong; Weisheng Zhao, Beihang University, Beijing, China

GEML: GNN-BASED EFFICIENT MAPPING METHOD FOR LARGE LOOP APPLICATIONS ON CGRA

Mingyang Kou, Jun Zeng, Jiangyuan Gu, Hailong Yao, Tsinghua University, Beijing, China; Boxiao Han, Fei Xu, China Mobile Research Institute, Beijing, China

MIXED-GRANULARITY PARALLEL COARSE-GRAINED RECONFIGURABLE ARCHITECTURE

Jinyi Deng, Linyun Zhang, Lei Wang, Jiawei Liu, Kexiang Deng, Jiangyuan Gu, Leibo Liu, Shaojun Wei, Shouyi YIN, Tsinghua University, Beijing, China; Shibin Tang, tsingmicro, Beijing, China; Boxiao Han, Fei Xu, China Mobile Research Institute, Beijing, China

PREVENTING BRAIN DRAIN: HOW TO SECURE NEXT GENERATION AI

Time: 3:30 PM – 5:30 PM
Room: 3006, Level 3
Event Type: Research Manuscript
Topics Area(s): AI/ML Security/Privacy, AI

Chair/Co-Chair: Farinaz Koushanfar, University of California, San Diego; TBA

This session presents state-of-art advances in next-generation AI/ML and machine learning security. The first three papers present advances in privacy-preserving machine learning, including work on protecting AI/ML hardware accelerators, and private deep learning inference using multi-party computation. The fourth paper secures hyper-dimensional computing hardware against fault injection attacks. The final paper describes a novel adversarial attack on spiking neural networks.

GUARDNN: SECURE ACCELERATOR ARCHITECTURE FOR PRIVACY-PRESERVING DEEP LEARNING

Weizhe Hua, Muhammad Umar, Zhiru Zhang, Edward Suh, Cornell University/Meta, Ithaca, NY

SRA: A SECURE RERAM-BASED DNN ACCELERATOR

Lei Zhao, Youtao Zhang, Jun Yang, University of Pittsburgh, PA

ABNN^2: SECURE TWO-PARTY ARBITRARY-BITWIDTH QUANTIZED NEURAL NETWORK PREDICTIONS

Liyan Shen, Jinqiao Shi, Shengli Pan, Ruisheng Shi, Beijing University of Posts and Telecommunications, Beijing, China; Ye Dong, Xuebin Wang, Chinese Academy of Sciences, Beijing, China; Binxing Fang, UESTC, Guangdong, China

ADAPTIVE NEURAL RECOVERY FOR HIGHLY ROBUST BRAIN-LIKE REPRESENTATION

Prathyush Poduval, Indian Institute of Science, Bengaluru, India; Yang Ni, Mohsen Imani, University of California, Irvine, CA; Yeseong Kim, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea; Kai Ni, Rochester Institute of Technology, Rochester, NY; Raghavan Kumar, Intel Corporation, Santa Clara, CA; Rossario Cammarota, Intel Corporation, San Diego, CA

EFFICIENCY ATTACKS ON SPIKING NEURAL NETWORKS

Sarada Krithivasan, Nitin Rathi, Kaushik Roy, Anand Raghunathan, Purdue University, West Lafayette, IN; Sanchari Sen, IBM Research, Yorktown Heights, NY

SSD: STORAGE SUPREMACY FOR LIFELONG DATA

Time: 3:30 PM – 5:30 PM
Room: 3004, Level 3
Event Type: Research Manuscript
Topics Area(s): Embedded Memory, Storage and Networking, Embedded Systems

Chair/Co-Chair: Li-Pin Chang, National Chiao-Tung University; Akash Kumar, TU Dresden

Wide adoption of solid-state drives (SSDs) introduces unprecedented opportunities and challenges for storage systems. This session includes six papers that leverage SSDs to address various challenges with new methods such as learning, hardware/software codesign, etc.

L-QOCO: LEARNING TO OPTIMIZE CACHE CAPACITY OVERLOAD PROBLEM IN STORAGE SYSTEMS

Ji Zhang, Yifan Li, Huazhong University of Science and Technology, Wuhan, China; Xijun Li, Huawei, Shenzhen, China; Xiyao Zhou, Mingxuan Yuan, Zhuo Cheng, Keji Huang, Huawei, Chengdu, China

PIPETTE: EFFICIENT FINE-GRAINED READS FOR SSDS

Shuhan Bai, Hu Wan, Yun Huang, Xuan Sun, Jason Xue, City University of Hong Kong, Hong Kong; Fei Wu, Huazhong University of Science and Technology, Wuhan, China; Changsheng Xie, Huazhong University of Science and Technology, Wuhan, China; Tei-Wei Kuo, Academia Sinica & National Taiwan University, Taipei, Taiwan; Hung-Chih Hsieh, YEESTOR Microelectronics Co., Ltd, Shenzhen, China

CDB: CRITICAL DATA BACKUP DESIGN FOR CONSUMER DEVICES WITH HIGH-DENSITY FLASH BASED HYBRID STORAGE

Longfei Luo, Dingcui Yu, Liang Shi, Chuanming Ding, Changlong Li, Edwin Hsing-Mean Sha, East China Normal University, Shanghai, China

SS-LRU: A SMART SEGMENTED LRU CACHING FOR STORAGE SYSTEM

Chunhua Li, Man Wu, Yuhan Liu, Ke Zhou, Ji Zhang, Huazhong University of Science and Technology, Wuhan, China; Yunqing Sun, Tencent Technology (Shenzhen) Co., Ltd, Shenzhen, China

NOBLSM: AN LSM-TREE WITH NON-BLOCKING WRITES FOR SSDS

Haoran Dang, Chongnan Ye, Yanpeng Hu, Chundong Wang, Shanghai Tech University, Shanghai, China

TAILCUT: IMPROVING PERFORMANCE AND LIFETIME OF SSDS USING PATTERN-AWARE STATE ENCODING

Jaeyong Lee, Myungsuk Kim, Sanggu Lee, Jihong Kim, Seoul National University, Seoul, South Korea; Wonil Choi, Hanyang University, Ansan-si, South Korea

THE LONG WAVE OF LOGIC SYNTHESIS: OLD CHALLENGES, NEW SOLUTIONS

Time: 3:30 PM – 5:30 PM
Room: 3007, Level 3
Event Type: Research Manuscript
Topics Area(s): RTL/Logic Level and High-level Synthesis, EDA

Chair/Co-Chair: Mathias Soeken, Microsoft; Cunxi Yu, University of Utah

Logic synthesis is one of the most important steps in chip design: yet too complex and expensive. This session provides new solutions to such old challenges. The first proposes an iterative flow for logic synthesis, while the second aims at using LUT-based optimization for ASIC synthesis. The third paper shifts the focus on the long runtimes, proposing to accelerate logic rewriting with GPUs. The next two papers provide techniques to optimize approximate logic synthesis. The sixth paper provides a solution to insert buffer and slitter cells for the new adiabatic quantum-flux parametron (AQFP) technology.

HIMAP: A HEURISTIC AND ITERATIVE LOGIC SYNTHESIS APPROACH

Xing Li, Lei Chen, Fan Yang, Mingxuan Yuan, Huawei, Hong Kong; Hongli Yan, Yupeng Wan, HiSilicon, Shanghai, China

IMPROVING LUT-BASED OPTIMIZATION FOR ASIC

Walter Lau Neto, Pierre-Emmanuel Gaillardon, University of Utah, Salt Lake City, UT; Luca Amaru, Synopsys, Sunnyvale, CA; Vinicius Possani, Patrick Vuillod, Jiong Luo, Synopsys, Sunnyvale, CA; Alan Mishchenko, University of California, Berkeley, CA

NOVELREWRITE: NODE-LEVEL PARALLEL AIG REWRITING

Shiju Lin, Jinwei Liu, Tianji Liu, Martin Wong, Evangeline Young, The Chinese University of Hong Kong, Hong Kong

SEARCH SPACE CHARACTERIZATION FOR APPROXIMATE LOGIC SYNTHESIS

Linus Witschen, Tobias Wiersema, Lucas Reuter, Marco Platzner, Paderborn University, Paderborn, Germany

SEALS: SENSITIVITY-DRIVEN EFFICIENT APPROXIMATE LOGIC SYNTHESIS

Chang Meng, Xuan Wang, Jiajun Sun, Sijun Tao, Weikang Qian, Shanghai Jiao Tong University, Shanghai, China; Wei Wu, Huawei, Hillsboro, OR; Zhihang Wu, Leibin Ni, Xiaolong Shen, Junfeng Zhao, Huawei, Shenzhen, China

BEYOND LOCAL OPTIMALITY OF BUFFER AND SPLITTER INSERTION FOR AQFP CIRCUITS

Siang-Yun Lee, Giovanni De Micheli, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland; Heinz Riener, Cadence Design Systems, Inc., Munich, Germany

WHAT ARE THE BIG OPPORTUNITIES IN THE NEXT RENAISSANCE OF EDA?

Time: 3:30 PM – 5:30 PM
Room: 3001, Level 3
Event Type: Research Panel
Topics Area(s): EDA

Organizer(s): X. Sharon Hu, University of Notre Dame, Notre Dame, IN

Moderator: Jason Cong, University of California, Los Angeles, CA

Existing approaches in the field of design and design automation, are facing extraordinary challenges. For example, traditional ways of improving silicon CMOS technologies or designing, verifying and testing integrated circuits and systems are approaching various limits such as physical size, power and reliability limits, as well as complexity limits. At the same time, our dependency on such systems is growing ever faster. This creates major research opportunities for new approaches beyond conventional paths. Moreover, the rise of machine learning and artificial intelligence (ML/AI) applications, the trend towards domain-specific accelerators and computing at the edge, and progress in nano-systems enabled by beyond-silicon CMOS technologies create new opportunities for customized solutions to designing electronic systems.

With these daunting challenges and exciting opportunities as well as the promise of strong funding support, it is expected that there will be a renaissance of EDA! But there are many different opinions on what research directions, funding formats, and business models will propel the arrival of the renaissance. This panel invite a group of research and industry leader as well as funding agency representatives in design and design automation to debate this topic. The panel will start with a summary of the funding landscape in the U.S.. Then, the panelists will give their opinions on issues such as:

- What are the biggest technical challenges facing the EDA field today?
- What design and design automation research areas should be prioritized for funding?
- For a given fixed amount of funding, should fewer but larger efforts or more but smaller efforts be supported?
- Since EDA methodologies can be applicable to many engineered systems, will EDA become more “distributed”?
- Should EDA follow the model in the ML/AI area to make the tools more accessible by non-expert designers?
- Design and EDA companies: what do you need the research community to work on?

Panelists: Sankar Basu, NSF, Alexandria, VA; Timothy Green, Semiconductor Research Corporation, Chapel Hill, NC; Prith Banerjee, Ansys, Palo Alto, CA; Jan Rabaey, University of California, Berkeley, CA; Tim Cheng, Hong Kong University of Science and Technology, Hong Kong, Hong Kong; Jayanthi Pallinti, APD, Gresham, OR

RE-VISIONING WHAT EDA CAN DO FOR ML, AND WHAT ML CAN DO FOR EDA

Time: 3:30 PM – 5:30 PM
Room: 3003, Level 3
Event Type: Special Session (Research)
Topics Area(s): AI, EDA

Organizer(s): Ismail Bustany, AMD, San Francisco, CA

Machine learning and artificial intelligence continue to see substantial growth in attention and resources across the design ecosystem. Numerous academic and industry efforts have reported successes. And, there is new understanding of realities with respect to scalability, training cost, need for model diagnosis and debug, or final optimization solution quality. This session gives a re-visioning of forward paths for EDA and ML: what EDA can do for ML, and what ML can do for EDA. Speakers will be asked to highlight three aspects: (1) concrete insights into novel methods and applications at the EDA-ML interface; (2) practical realities and challenges, along with potential mitigations; and (3) high-upside directions for future investment. After examples have been presented, a panel discussion will dig deeper into potential high-value forward paths. The session is designed to be of interest to attendees from academia, industry R&D in EDA and IC design, senior managers, the investment community and government organizations.

SHARED FOUNDATIONS FOR ML AND EDA

Sicun (Sean) Gao, University of California, San Diego, La Jolla, CA

USING LOGIC TO UNDERSTAND LEARNING

Satrajit Chatterjee, Mountain View, CA

UNSUPERVISED LEARNING FOR GATE SIZING

Siddhartha Nath, NVIDIA, San Jose, AL

LARGE-SCALE MODEL-FREE FEATURE SELECTION AND VISUALIZATION

Igor Markov, Facebook, Sunnyvale, CA

TUESDAY GLADIATOR POSTER BATTLE

Time: 4:30 PM – 5:30 PM

Room: DAC Pavilion, Level 2

See the 2022 Engineering Track Poster Gladiator finalist present their posters in a speed round. Poster Gladiators are chosen from all Engineering Track sessions including front-end, back-end, IP, embedded and cloud. Attendees and judges vote for the best Poster Gladiator! Come to the Pavilion and cast your vote. The 2022 Poster Gladiator will be selected at the Wednesday Poster Gladiator session.

AUTOMATED TIMING DEGRADATION RECOVERY IN INCREMENTAL TAPE-OUT OF HIGH-SPEED CPU DESIGN

Gopalakrishnan Sadagopan, Senthil Ravi, Intel Technology India Pvt. Ltd, Bengaluru, India

USING FORMAL VERIFICATION SIGNOFF FOR DIGITAL IP

David Vincenzoni, STMicroelectronics, Agrate Brianza, Italy

MACHINE LEARNING TECHNIQUES FOR PDK DEVELOPMENT EFFICIENCY

Nolan Pavek, GlobalFoundries, Miami, FL; Romain Feuillette, GlobalFoundries, Burlington, CA; Vivienne Miller, GlobalFoundries, Ellicott City, MD

OPTIMAL AND EFFICIENT POWER AWARE VERIFICATION FRAMEWORK FOR LOW POWER MIXED-SIGNAL SOC

Sooraj Sekhar, Harsh Sharma, Siddharth Sarin, Pavan Kumar Kulkarni, Ruchi Shankar, Harish Maruthiyodan, Shalini Eswaran, Gaurav Varshney, Lakshmanan Balasubramanian, Texas Instruments (India) Pvt. Ltd., Bengaluru, India; Akshay Revankar, Carnegie Mellon University, Pittsburgh, PA

TECHNOLOGY CO-OPTIMIZATION TO MITIGATE THE TECHNOLOGY IMPACT OF CONTEXT-BASED TIMING IN STANDARD CELL LIBRARY

Veny Mahajan, Anand Mishra, STMicroelectronics, Noida, India

IS FRONT-END ANALOG DESIGN AUTOMATION AN NP-TYPE OR SIMPLY A P-TYPE PROBLEM ?

Ramy Iskander, Intento Design, Paris, France

TUESDAY ENGINEERING TRACKS POSTER RECEPTION

Time: 5:00 PM – 6:00 PM
Room: Level 2 Exhibit Hall

AUTOMATED DCAP AND FILLER CELL INSERTION WITH EMBEDDED DESIGN FOR INSPECTION (DFI) SENSORS

Matthew Moe, PDF Solutions Inc., Pittsburgh, PA; Marcin Strojwas, PDF Solutions Inc., Santa Clara, CA; Fady Fouad, Siemens EDA, Cairo, Egypt; Jeff Wilson, Siemens EDA, Wilsonville, OR

CHALLENGES OF INTEGRATING AND TESTING A DESIGN WITH MULTIPLE IP VENDORS

Edward Seymour, Marvell Semiconductor, Austin, TX

A COMPREHENSIVE ELECTROMAGNETIC ANALYSIS FOR TRANSMISSION LINE IN HIGH-SPEED AMS DESIGN

Yaping Huang, Kai Fang, Sanechips Technology Co.,Ltd, Shenzhen, China; Hong Jia, Ansys, Chengdu, China; Jie Cheng, Ansys, Pudong, China

COMPUTE-IN-MEMORY SRAM ARRAY WITH NEW ENERGY EFFICIENT RECONFIGURABLE DATA SENSING TECHNIQUE FOR HARDWARE ACCELERATORS

Kavitha S, Indian Institute of Information Technology, Design and Manufacturing, Kancheepuram, Mangaluru, India; Bhupendra Reniwal, Indian Institute of Information Technology, Design and Manufacturing, Kancheepuram, Chennai, India; Devesh Dwivedi, GlobalFoundries, Malta, NY

CONCURRENT PACKAGE + INTERPOSER + DIE IR ANALYSIS USING ANSYS' REDHAWK-SC ELECTROTHERMAL

Nikhil Jayakumar, Amazon, Cupertino, CA

DEALING WITH SILICON AGING IN DIGITAL IMPLEMENTATION USING LIBRARY METRICS

Marc Zheng, Unisoc, Xiamen, China; Yilin Weng, Chen Fang, Unisoc, Shanghai, China; Xiao Yong, Empyrean, Beijing, China

DESIGN TIMING EFFECTS OF LAYER-TO-LAYER INTERCONNECT SKEW

Ayhan Mutlu, Synopsys, Los Gatos, CA; Duc Huynh, Li-Chung Hsu, Li Ding, Synopsys, San Jose, CA; Jian-Feng Chen, Synopsys, Mountain View, CA

DYNAMIC CDC VERIFICATION WITH ENHANCED JITTER MODELING IN SYNCHRONIZERS

Youngchan Lee, Samsung Electronics, Hwaseong-si, South Korea; Vikas Sachdeva, Real Intent Inc, Bengaluru, India

EFFICIENT READ/WRITE TURN-AROUND POLICY OF LPDDR5 MEMORY CONTROLLER

Taewoo Han, Samsung Electronics, Giheung, South Korea; Taehun Kim, Wooil Kim, Samsung Electronics, Hwaseong, South Korea

EFFICIENT LOW POWER ISOLATION HANDLING FOR PRE-SILICON EMULATION

Madhusudhan Gurram, Texas Instruments, Bengaluru, India; Rakesh Bansal, Texas Instruments, Karnataka, India

ENHANCING SILICON SCREENING USING OPTIMIZED CLUSTERING-BASED SDD VECTOR

Keunsoo Lee, Yun Heo, Kunhyuk Kang, Seonil Choi, Samsung Electronics, Hwaseong, South Korea; Khader Khader Abdel-Hafez, Synopsys, Sunnyvale, CA; YongJoon Kim, Synopsys, Hwaseong, South Korea

ENSURING ACCURATE CROSSTALK ANALYSIS USING CCS-NOISE LIBERTY MODEL

Anil Dwivedi, Mitu Mittal, Rahul Kumar, ST Microelectronics Pvt Ltd, Noida, India;

FAST DESIGN SPACE EXPLORATION USING RTL ARCHITECT FOR DRAM DESIGNS

Hyeonsik Son, Yonghwan Kim, Hyojin Choi, Seoklip Ki, Hyeyoun Kim, Younsik Park, Jung Yun Choi, Samsung Electronics, Hwaseong, South Korea

GENERATION AND SELECTION OF UNIVERSALLY ROUTABLE VIA MESH SPECIFICATIONS

Joe Koone, IBM, Poughkeepsie, NY; Smitha Reddy, IBM, Bengaluru, India; Michael Bowen, IBM, Wallkill, NY; Adam Matheny, IBM, Beacon, NY; Gustavo Tellez, IBM, Essex Junction, VT

IN-DESIGN IR DROP CONVERGENCE WITH ANSYS RHSC AND SNPS FUSION COMPILER

Purushotham Reddy, Usha Muruli, Intel Technology India Pvt. Ltd, Bengaluru, India

INTEGRATING LIBERTY MODEL VALIDATION, ANALYSIS, AND VISUALIZATION AS PART OF LIBRARY DESIGN AND CHARACTERIZATION

Jean-Arnaud Francois, STMicroelectronics, Crolles, France; Saurabh Srivastava, Natish Singla, STMicroelectronics, Noida, India; Austin Shirley, Siemens EDA, Saskatoon, Canada; Tina Durgia, Siemens EDA, Santa Clara, CA

LEFT SHIFT MECHANISM TO MITIGATE GATE LEVEL ASYNCHRONOUS DESIGN CHALLENGES

Rohit Sinha, Intel Technology India Pvt. Ltd, Bengaluru, India; Kavya Kotha, Intel Technology India Pvt. Ltd, Hyderabad, India

LEFT SHIFT OF MULTI-CYCLE PATHS AND FALSE PATHS SIGNOFF BY FORMAL AND DYNAMIC SIMULATION METHODOLOGIES WITH SIGNIFICANT ROI

Jebin Mohandas, Intel Corporation, Bengaluru, India

LOW POWER VERIFICATION CHALLENGES OF HIERARCHICAL UPF IN DISCRETE GRAPHICS SOC DESIGN

Monika Rawat, Deepmala Sachan, Dipankar Arya, Suhas DS, Intel Corporation, Bengaluru, India

MINIMUM REPEATER ADDITION ECOS FOR POWER EFFICIENT DESIGNS

Shiven Pandya, Bindu Rao, Intel Corporation, Bengaluru, India

POSTMASK FUNCTIONAL ECO IMPLEMENTATION FLOW USING PROGRAMMABLE CELLS

Sidharth Ranjan Panda, Mahesh Baghel, Sasi Koney, Intel Corporation, Bengaluru, India

PROTOLINT: PROTOCOL- AND IP-AWARE LINT FOR RTL INTEGRATION

Minje Jun, Minsu Kim, Yewon Lee, Sangyoun Lee, Wooil Kim, Samsung Electronics, Hwaseong, South Korea

SDR (SIMULATION-DRIVEN ROUTING): A SOLUTION TO GET ELECTROMIGRATION COMPLIANT ROUTING

Priya Meharde, Anubhuti Chopra, STMicroelectronics, Greater Noida, India; Priyanshi Shukla, Cadence Design Systems, Inc., Noida, India

SHIFT LEFT DFT SIGN-OFF METHODOLOGY FOR EDGE AI PROCESSOR

Parag Dass, Venkata Raju, Kinara Inc., Hyderabad, India; Kanad Chakraborty, Real Intent Inc, Portland, OR; Varun Sharma, Real Intent Inc, Bengaluru, India

SOLVING ANTENNA ERRORS FOR HIERARCHICAL DESIGNS

Joe Koone, IBM, Poughkeepsie, NY; Michael Bowen, IBM, Wallkill, NY; Ed Hughes, IBM, Toledo, OH; Mitchell DeHond, IBM, Essex Junction, VT; Smitha Reddy, IBM, Bengaluru, India

TCP/IP HARDWARE STACK DESIGN AND VERIFICATION CHALLENGES

Andreas Emeretlis, Dimitrios Bozikas, CAST, Inc., Patras, Greece; Tony Sousek, CAST, Inc., Brno, Czech Republic

THERMAL AWARE MEMORY CONTROLLER DESIGN WITH CHIP PACKAGE SYSTEM SIMULATION

Shiva Shankar Padakanti, Telangana, Hyderabad, India; Ravi Kollipara, Micron India, Morgan Hill, CA; Dileesh Jostin, Ansys, Bengaluru, India; Vamsi Krishna, Ansys, Pune, India

TOWARDS AN AUTOMATED WORKFLOW FOR LINK-LEVEL EXPLORATION AND OPTIMIZATION IN THE DOMAIN OF ALL-TO-ALL OPTICAL NETWORKS

Luca Ramini, Hewlett Packard Enterprise, Milpitas, CA; Ahsan Alam, Ansys, Vancouver, Canada

A UNIFIED IP QA METHODOLOGY TO IMPROVE VALIDATION COVERAGE AND THROUGHPUT

Lippika Parwani, STMicroelectronics, Greater Noida, India; Jean-Arnaud Francois, STMicroelectronics, Crolles, France; Geetanjali Sharma, STMicroelectronics, Mumbai, India; Wei-Lii Tan, Siemens EDA, Fremont, CA; Lionel Couder, Siemens EDA, Grenoble, France

WORKFLOW AUTOMATION FOR SOC PERFORMANCE VERIFICATION

Hoyoon Jun, Woorim Kim, Conextt Inc, Seoul, South Korea; Jaein Hong, Hyunman Park, Hongkyu Kim, Samsung Electronics, Hwaseong, South Korea

XMAS: AN EFFICIENT CUSTOMIZABLE FLOW FOR CROSSBARRED-MEMRISTOR ARCHITECTURE SEARCH

Yuan Ren, Wenyong Zhou, Ziyi Guan, Ngai Wong, Ziyi Guan, The University of Hong Kong, Hong Kong, Hong Kong; Rui Xie, Quan Chen, Hao Yu, Southern University of Science and Technology, Shenzhen, China

A HIGH-ACCURACY VOLTAGE-AWARE-TIMING SOLUTION FOR HPC DESIGN

Xiyu Wang, ZTE Technology Co., Ltd.; Zhijun Long, Keqing Ouyang, Junjie Chen, Ping Ding, Sanechips Technology Co.,Ltd; Dongli Song, Synopsys; Chang Zhao, Li Zou, Muhammad Zakir, Ansys

BUILDING A ROBUST POWER GRID FOR MULTI MILLION SOC USING REDHAWK-SC EARLY PG GRID ANALYSIS

Rishikanth Mekala, Arpan Bhowmik, Samsung Semiconductor; Krishna Yellamilli, Ansys

WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 PM – 7:00 PM
Room: Level 2 Lobby

ACCELERATING DATA ANALYTICS NEAR MEMORY: A K-NN SEARCH CASE STUDY

Minho Ha, Joonseop Sim, Jungmin Choi, Donguk Moon, Myunghyun Rhee, Taeyoung Ahn, Byungil Koh, Euicheol Lim, Kyoung Park, SK hynix, Icheon-si, South Korea

ADAPTIVE SPARSITY-AWARE CLOUD OFFLOADING FOR EDGE DNN INFERENCE

Marina Neseem, Brown University, Abdelrahman Hosny, Sherief Reda, Brown University, Providence, RI

ADDRESSING ORDERING WOES OF PCIE WITH FORMAL VERIFICATION

Vedprakash Mishra, Anshul Jain, Achutha KiranKumar V M, Intel Corporation, Bengaluru, India; Carlston Lim, Intel Corporation, Zhi Feng Lee, Jian Zhong Wang, Intel Corporation, Bayan Lepas, Malaysia

AI/ML DRIVEN SELF-ADAPTIVE DESIGN METHODOLOGY FOR ANALOG CIRCUITS

Koushik De, Deepthi Amuru, Andleeb Zahra, Mounika Kelam, Indian Institute of Technology, Hyderabad, Hyderabad, India; Abhishek Pullela, Ashfakh Ali, Battu Yadav, Ashutosh Pathy, Gaurav Dixit, Zia Abbas, International Institute of Information Technology, Hyderabad, India; Khanh Le, Analog Intelligent Design Inc., Morgan Hill, CA

BIT-FLEX: AN ENERGY-EFFICIENT ANALOG-DIGITAL HYBRID DNN ACCELERATOR WITH BIT-LEVEL FLEXIBLE SCALABILITY

Donghyeon Yi, Injun Choi, Gichan Yun, Edward Choi, Minkyu Je, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea; Sohmyung Ha, New York University, Abu Dhabi, Abu Dhabi, United Arab Emirates; Ik Joon Chang, Kyunghee University, Yongin-si, South Korea

BRIDGER: FAST TOKEN DELIVERY IN ELASTIC CIRCUITS

Ayatallah Elakhras, Andrea Guerrieri, Paolo Ienne, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland; Lana Josipovic, ETH Zürich, Zurich, Switzerland

BUILDING EFFICIENT PORTFOLIO-BASED HARDWARE MODEL CHECKER VIA AND-INVERTER GRAPH STRUCTURE ENCODING

Chengyu Zhang, Jiayi Zhu, Yihao Huang, Jianwen Li, Geguang Pu, East China Normal University, Shanghai, China; Moshe Vardi, Rice University, Houston, TX

CHARTM: AN EFFICIENT AND ACCURATE TIMING YIELD ANALYSIS METHOD FOR MEMORY CHARACTERIZATION BASED ON GENERALIZED PARETO DISTRIBUTION

Liang Pang, Xiao Shi, longxin Shi, Hao Yan, Southeast University, NanJing, China

CIRCUMVENTING MACHINE LEARNING-BASED ATTACKS TO LOGIC LOCKING

Yinghua Hu, Subhajit Dutta Chowdhury, Kaixin Yang, Mustafa Munir, Jatin Bollareddy, Pierluigi Nuzzo, University of Southern California, Los Angeles, CA

COCO-FL: COMMUNICATION- AND COMPUTATION-AWARE FEDERATED LEARNING VIA PARTIAL NN FREEZING AND QUANTIZATION

Kilian Pfeiffer, Martin Rapp, Joerg Henkel, Karlsruhe Institute of Technology, Karlsruhe, Germany; Ramin Khalili, Huawei, Munich

A CUSTOM MACRO SUITE FOR OPTIMIZATION OF NEUROMORPHIC TNN DESIGNS IN CMOS

Harideep Nair, John Paul Shen, Carnegie Mellon University, Mountain View, CA; Prabhu Vellaisamy, Santha Bhasuthkar, Carnegie Mellon University, Pittsburgh, PA

DEEP LEARNING EMPOWERED SPECTRUM SENSING AND ACCESS IN DISTRIBUTED COGNITIVE RADIO NETWORK

Keke Gai, Yue Zhang, Liehuang Zhu, Beijing Institute of Technology, Beijing, China; Meikang Qiu, Texas A&M University, College Station, TX

DESIGN SPACE EXPLORATION OF MIXED-PRECISION HARDWARE ACCELERATORS FOR CNNS

Cecilia Latotzke, Tim Ciesielski, Tobias Gemmeke, RWTH Aachen University, Aachen, Germany

DISPLAY PIXEL LAYOUT DESIGN WITH DEEP REINFORCEMENT LEARNING

Byeong Keun Kang, Hyung Joon Nam, In Huh, Jae Keon Bae, Jeong Hyeon Choi, Ki Seok Chang, Woohyung Lim, Il Ho Kim, Seok Woo Lee, Soo Young Yoon, LG, Seoul, South Korea

EA-PRUNE: ENVIRONMENT ADAPTIVE NEURAL NETWORK PRUNING FOR LOW-POWER ENERGY HARVESTING DEVICES

Sahidul Islam, Yufang Jin, Mimi Xie, The University of Texas at San Antonio, San Antonio, TX; Shanglin Zhou, Yueying Liang, Caiwen Ding, University of Connecticut, Storrs, CT; Ran Ran, Wujie Wen, Lehigh Unversity, Bethlehem, PA

ENABLING VERSATILE POWER MANAGEMENT FOR AIOT DEVICES

Xiaofeng Hou, Luhong Liang, ACCESS, Hong Kong, China; Xuehan Tang, Jiacheng Liu, Chao Li, Shanghai Jiao Tong University, Shanghai, China; Tim Cheng, Hong Kong University of Science and Technology, Hong Kong

ENDURANCE-AWARE DEEP NEURAL NETWORK REAL-TIME SCHEDULING ON RERAM ACCELERATORS

Shi Sha, Wilkes University, Wilkes Barre, PA; Ajinkya Bankar, Florida International University, Miami, FL; Xiaokun Yang, University of Houston, Clear Lake, Clear Lake, TX; Wujie Wen, Lehigh Unversity, Bethlehem, PA; Gang Quan, Florida International University, Miami, AL

ENERGY PROFILING OF USB DNN ACCELERATORS

Matthias Wess, Matvey Ivanov, Nikolas Alge, Christian Krieg, Axel Jantsch, Technische Universität Wien, Vienna, Austria

ES4D: ACCELERATING EXACT SIMILARITY SEARCH FOR HIGH-DIMENSIONAL VECTORS VIA VECTOR SLICING AND IN-SSD DISTANCE CALCULATION

Juhwan Kim, Jong Sun Seo, Jong-Hyeok Park, Sang-Won Lee, Hyungmin Cho, Sungkyunkwan University, Suwon, South Korea; Hongchan Roh, Seongnam, Gyeonggi-do, South Korea

EXPLORING INPUT DATA OBFUSCATION AS A COUNTERMEASURE TO MODEL EXTRACTION ATTACKS ON DEEP NEURAL NETWORKS

Brooks Olney, Robert Karam, University of South Florida, Tampa, FL

FINGERPRINTING WORKLOADS FOR RECONFIGURABLE SHARED ACCELERATORS

Parnian Mokri, Medford, MA; Mark Hempstead, Tufts University, Medford, MA

FLOW-3D: FLOW-BASED COMPUTING ON 3D NANOSCALE CROSSBARS WITH MINIMAL SEMIPERIMETER

Sven Thijssen, Rickard Ewetz, University of Central Florida, Orlando, FL; Sumit Jha, The University of Texas at San Antonio, San Antonio, TX

FSA: AN EFFICIENT FAULT-TOLERANT SYSTOLIC ARRAY-BASED DNN ACCELERATOR ARCHITECTURE

Yingnan Zhao, Ke Wang, Ahmed Louri, George Washington University, Washington, DC; Avinash Karanth, Ohio University, Athens, OH; Razvan Bunescu, University of North Carolina, Charlotte, Charlotte, NC

GRAPH PARTITIONING APPROACH FOR FAST QUANTUM CIRCUIT SIMULATION

Jaekyung Im, Sunghye Park, Seokhyeong Kang, Pohang University of Science and Technology, Pohang, South Korea

HETEROGENEOUS CHIPLET-BASED ARCHITECTURE FOR IN-MEMORY ACCELERATION OF DNNS: A BIG-LITTLE APPROACH

Gokul Krishnan, Chaitali Chakrabarti, Yu Cao, Arizona State University, Tempe, AZ; Jae-sun Seo, Arizona State University, Tempe, AZ; Sumit Mandal, Umit Ogras, University of Wisconsin, Madison, WI;

HPVM2FPGA: ENABLING TRUE HARDWARE-AGNOSTIC FPGA PROGRAMMING

Adel Ejjeh, Leon Medvinsky, Aaron Councilman, Hemang Nehra, Suraj Sharma, Vikram Adve, University of Illinois at Urbana-Champaign, Urbana, IL; Luigi Nardi, Lund University, Lund, Sweden; Eriko Nurvitadhi, Intel Corporation, Hillsboro, OR; Rob Rutenbar, University of Pittsburgh, Pittsburgh, PA

IMPLEMENTING EFFICIENT, PRECISE N-BIT OPERATIONS OF TFHE ON COMMODITY CPU-FPGA

Kevin Nam, Hyunyoung Oh, Sanghyuk Heo, Seoul National University, Seoul, South Korea; Hyungon Moon, UNIST, Ulsan, South Korea; Yunheung Paek, Inter-University Semiconductor Research Center (ISRC), Seoul, South Korea

NEURAL NETWORK LAYER ASSIGNMENT FOR DISTRIBUTED INFERENCE VIA INTEGER PROGRAMMING

JOINT RESOURCE SCHEDULING IN WIRELESS NETWORKED CONTROL SYSTEMS WITH ENERGY CONSTRAINT

Vincent Chau, Chenchen Fu, Southeast University, Nanjing, China; Shu Han, Zhejiang University, Ningbo, China; Song Han, Peng Wu, University of Connecticut, Storrs, CT; Minming Li, City University of Hong Kong, Hong Kong; Yingchao Zhao, Hong Kong Caritas Institute of Higher Education, Hong Kong

LEGO: DYNAMIC MULTI-CHIP-MODULE RESOURCE PROVISION ARCHITECTURE FOR MULTI-TENANT DNNS

Ching-Jui Lee, Yu Xuan Zhou, Tsung Tai Yeh, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

A LINEAR COLUMN-MAJOR CAPACITANCE MULTIPLIER BASED ANALOG IN-MEMORY COMPUTING ARCHITECTURE

Kailash Prasad, Aditya Biswas, Arpita Kabra, Joycee Mekie, Indian Institute of Technology, Gandhinagar, India

LOGIC LOCKING BASED TROJANS: A FRIEND TURNS FOE

Yuntao Liu, Ankur Srivastava, University of Maryland, College Park, MD Aruna Jayasena, Prabhat Mishra, University of Florida, Gainesville, FL

LOGICWISARD: MEMORYLESS SYNTHESIS OF WEIGHTLESS NEURAL NETWORKS

Igor Miranda, Federal University of Reconcavo da Bahia, Salvador, Brazil; Zachary Susskind, Aman Arora, Lizy John, The University of Texas at Austin, TX; Luis Villon, Rafael Katopodis, Diego Dutra, Priscila Lima, Felipe França, Federal University of Rio de Janeiro, Rio de Janeiro, Brazil; Leandro Araújo, Fluminense Federal University, Niteroi, Brazil; Mauricio Breternitz, Instituto Universitário de Lisboa, Lisbon, Portugal

MENTHA: ENABLING SPARSE-AWARE COMPUTATION ON SYSTOLIC ARRAYS

Minjin Tang, Mei Men, Yasong Cao, Junzhong Shen, Jianchao Yang, Jiawei Fei, Yang Guo, Sheng Liu, National University of Defense Technology, Changsha, China

MULTI-PHASE CLOCKING FOR MULTI-THREADED GATE-LEVEL-PIPELINED SUPERCONDUCTIVE LOGIC

Xi Li, Peter Beerel, University of Southern California, Los Angeles, CA; Min Pan, Tong Liu, Synopsys, Mountain View, CA

MUZERO-GUIDED SIMULATED ANNEALING FOR NANOMETER CIRCUIT PLACEMENT

Wei-Hao Chang, Gao-Yi Chao, Yu-Hsun Chen, Chen-Feng Chiang, Chia-Shun Yeh, Chia-Yu Tsai, MediaTek Inc., Hsinchu, Taiwan; Chin-Tang Lai, MediaTek Inc., Hsinchu, Taiwan; Hung-Hao Shen, MediaTek Inc., Hsinchu, Taiwan; Kai-En Yang, National Tsing Hua University, Hsinchu, Taiwan; Yen-Min Tsai, Sau-Loong Low, Bun-Suan Heng, MediaTek Singapore Pte. Ltd., Singapore, Singapore

NOVEL ML BASED RECONFIGURABLE MACRO PLACEMENT FOR SOC DESIGN

Sudarshanam Kommanaboyina, Intel Corporation, Hyderabad, India

ON THE (IN)SECURITY OF MEMORY PROTECTION UNITS

Michele Grisafi, Bruno Crispo, University of Trento, Trento, Italy; Mahmoud Ammar, Huawei, Munich, Germany

PAR-GEM5: PARALLELIZING GEM5'S ATOMIC MODE

Niko ZurstrassenJosé Cubero-Cascante, Jan Joseph, Rainer Leupers, RWTH Aachen University, Aachen, Germany; Li Yichao, Xie Xinghua, Huawei, Shanghai, China

PHYSICS-CONSISTENT THERMAL SPICE AND MULTI-CORRELATED RECURRENT NEURAL NETWORKS TO SIMULATE SOPHISTICATED FINFET CIRCUITRY

Chia-Che Chung, Tao Chou, Bo-Wei Huang, Cheng Lin, Chia-Jung Tsen, C. W. Liu, National Taiwan University, Taipei, Taiwan

POWERSYNTH 2: A HIGH-DENSITY AND HETEROGENEOUS POWER ELECTRONICS PHYSICAL DESIGN AUTOMATION FRAMEWORK

Imam Al Razi, Quang Le, H. Alan Mantooth, Yarui Peng, University of Arkansas, Fayetteville, AR

A PROPOSITION FOR COMPUTING SYSTEM DESIGN AUTOMATICITY AND CORRECTNESS POTENTIAL

Tage Mohammadat, KTH Royal Institute of Technology, Stockholm, Sweden

PULP-TRAINLIB: ENABLING ON-DEVICE TRAINING FOR RISC-V MULTI-CORE MCUS THROUGH PERFORMANCE-DRIVEN AUTOTUNING

Davide Nadalini, Politecnico di Torino, Torino, Italy; Manuele Rusci, Giuseppe Tagliavini, Leonardo Ravaglia, Luca Benini, Francesco Conti, University of Bologna, Italy

QUANTUM MULTIPLE-VALUED DECISION DIAGRAMS WITH LINEAR TRANSFORMATIONS

Yonghong Li, Hao Miao, Haipeng Che, Liangda Fang, Quanlong Guan, Huanming Zhang, Jinan University, Guangzhou, China

RANKNAS: A DIFFERENTIAL NAS BASED AUTO RANK SEARCH TOWARDS VIDEO LSTM NETWORKS ON EDGE

Changhai Man, Chenchen Ding, Ao Shen, Hongwei Ren, Shaobo Luo, Hao Yu, Southern University of Science and Technology, Shenzhen, China Cheng Chang, University of California, Los Angeles, CA; Ziyi Guan, The University of Hong Kong, Hong Kong; Yuan Cheng, Shanghai Jiao Tong University, Shanghai, China

RFR: AN STT-MRAM CACHE MANAGEMENT SCHEME FOR RETENTION FAILURE REDUCTION

Abdollah Mohammadi, Elham Cheshmikhani, Hossein Asadi, Sharif University of Technology, Tehran, Iran

RUBIK'S OPTICAL NEURAL NETWORKS: MULTI-TASK LEARNING WITH PHYSICS-AWARE SYSTEM AND ALGORITHMS

Yingjie Li, Weilu Gao, Cunxi Yu, University of Utah, Salt Lake City, UT

A SECURE DESIGN METHODOLOGY TO PREVENT TARGETED TROJAN INSERTION DURING FABRICATION

Arjun Suresh, Siva Nishok Dhanuskodi, Daniel Holcomb, University of Massachusetts, Amherst, MA

TACKLING RESOURCE UTILIZATION IN DNN ACCELERATORS

Iris Uwizeyimana, Natalie Enright Jerger, University of Toronto, Canada

TRUSTTOKEN, TRUSTED SOC SOLUTION FOR NON-TRUSTED INTELLECTUAL PROPERTY (IP)S.

Muhammed Kawser Ahmed, Sujan Kumar Saha, Joel Mandebi Mbongue, Christophe Bobda, University of Florida, Gainesville, FL

TWO-LEVEL HIERARCHICAL CLUSTER-NODE SCHEDULING FOR HETEROGENEOUS DATACENTERS

Wenkai Guan, Cristinel Ababei, Marquette University, Milwaukee, WI

UNRAVELING LATCH LOCKING USING MACHINE LEARNING, BOOLEAN ANALYSIS, AND ILP

Dake Chen, Xuan Zhou, Peter Beerel, University of Southern California, Los Angeles, CA

X-ON-X SIMULATION: DISTRIBUTED PARALLEL SYSTEMC TLM VIRTUAL PLATFORMS FOR HETEROGENEOUS SYSTEMS

Lukas Jünger, Simon Winther, Rainer Leupers, RWTH Aachen University, Aachen, Germany

YOU ALREADY HAVE IT: A GENERATOR-FREE LOW-PRECISION DNN TRAINING FRAMEWORK USING STOCHASTIC ROUNDING

Geng Yuan, Sung-En Chang, Jin, Yanyu Li, Yushu Wu, Zhenglun Kong, Yanyue Xie, Peiyan Dong, Xiaolong Ma, Yanzhi Wang, Northeastern University, Boston, MA; Alec Lu, Zhenman Fang, Simon Fraser University, Burnaby, Canada; Xulong Tang, University of Pittsburgh, Pittsburgh, PA; Minghai Qin, Milpitas, CA

WESCO: WEIGHT-ENCODED RELIABILITY AND SECURITY CO-DESIGN FOR IN-MEMORY COMPUTING SYSTEMS

Jiangwei Zhang, Chong Wang, Yi Cai, Zhenhua Zhu, Guohao Dai, Huazhong Yang, Yu Wang, Tsinghua University, Wuhan, China Donald Kline, Jr, Intel Corporation, Hillsboro, OR;

Wednesday, July 13, 2022

AWARDS AND WEDNESDAY KEYNOTE

Time: 8:40 AM – 9:45 AM
Room: 3008-3012, Level 3
Event Type: Keynote

MACHINE LEARNING FOR REAL: WHY PRINCIPLES, EFFICIENCY, AND UBIQUITY MATTER

Steve Teig, Perceive, Palo Alto, CA

Marc Andreessen famously opined that "software is eating the world." Recently, various people have suggested that AI is eating software. Deep learning seems to touch every discipline these days, but behind its startling magic tricks, it is surprisingly primitive. Most deep learning today requires vast data centers whose power consumption burdens an already overstressed planet. Add in the latency and loss of privacy, and it is clear that society would benefit from gadgets that do not require connection to the cloud to be "smart". Even more concerning, however, is the strong dependence of today's deep learning on folklore: on recipes and anecdotes, rather than scientific principles and explanatory mathematics. Instead, we can develop rigorous, scalable machine learning guided by information theory to create models that are predictive, power-efficient, and cost-effective.

Wednesday Sessions

HOW TO RUN EDA TOOLS ON THE AZURE CLOUD

Time: 10:15 AM – 1:15 PM
Room: Design on Cloud Pavilion, Level 2 Exhibit Hall
Event Type: Design on Cloud Training

This session will cover how customers can bring chip development software to the Azure cloud. We will cover the advantages and disadvantages, issues around migrating data, the choices in storage available, security, and the tools Azure provides to help customers migrate their workloads. This session will include a demonstration on what it takes to bring a workload to the cloud and run a job.

Speakers: Richard Paw, Microsoft, Cupertino, CA

ENGINEERING PLENARY SESSION: SILENT ERRORS FROM COMPUTING HARDWARE: A CAMBRIAN EXPLOSION IN NEW INNOVATIONS IS DEAD AHEAD

Time: 10:30 AM – 12:00 PM
Room: 2008, Level 2
Event Type: Engineering Tracks
Topics Area(s): Back-End Design, Embedded Systems, Front-End Design, IP

Organizer(s): Subhasish Mitra, Stanford University, Stanford, CA

Moderator: Subhasish Mitra, Stanford University, Stanford, CA;

Undetected errors produced by computing systems, also called silent errors, have major consequences ranging from loss of data and services, to financial and productivity losses, or even loss of human life. Silent errors produced by computing hardware have been recently identified as a highly critical challenge in several articles by Google, Meta, and New York Times. Is this business as usual or do we need a paradigm shift? Will industrial teams alone be able to drive ground-breaking solutions? How can academia seize this golden opportunity to create radically new design and test solutions? What collaborations between device technologies, hardware design and test, EDA, IP ecosystem, and software systems are essential? What are the barriers to such collaborations today? Please join this diverse panel and brainstorm out-of-the-box solutions that can have a lasting impact on the computing industry, from (self-driving) cars to cloud computing in the data center. We look forward to the wisdom and insights from the panelists, firing line experts, and, very importantly, YOU - the audience.

Presenters: Shawn Blanton, Carnegie Mellon University, Pittsburgh, PA; Ambar Sarkar, NVIDIA, Boston, MA; Rob Chappell, Microsoft, Phoenix, AZ; Harish Dixit, Meta, Mountain View, CA; Jeffrey Hicks, Intel Corporation, Hillsboro, OR; Peter Hochschild, Google, New York City, NY; Jeff Rearick, AMD, Fort Collins, CO; Pradip Bose, IBM, Yorktown Heights, NY; Jennifer Dworak, Southern Methodist University, Dallas, TX

DOMAIN-SPECIFIC PIM ACCELERATORS FROM CLIENT TO CLOUD

Time: 10:30 AM – 12:00 PM
Room: 3002, Level 3
Event Type: Research Manuscript
Topics Area(s): In-memory and Near-memory Computing, Cloud, Design

Chair/Co-Chair: Jianlei Yang, Beihang University; TBA

As Moore's Law enters its twilight years, domain-specific designs have emerged as a primary mechanism to deliver ever-increasing levels of performance under strict energy-efficiency requirements. The papers in this session cover a wide range of domain-specific PIM solutions, from network architecture search techniques targeting in-memory compute platforms, to accelerators for graph neural networks, stereo matching, recommendation systems, and beyond.

NAX: NEURAL ARCHITECTURE AND MEMRISTIVE XBAR BASED ACCELERATOR CO-DESIGN

Shubham Negi, Indranil Chakraborty, Kaushik Roy, Purdue University, West Lafayette, IN; Aayush Ankit, Microsoft, Mountain View, CA

MC-CIM: A RECONFIGURABLE COMPUTATION-IN-MEMORY FOR EFFICIENT STEREO MATCHING COST COMPUTATION

Zhiheng Yue, Yabing Wang, Leibo Liu, Shaojun Wei, Shouyi Yin, Tsinghua University, Beijing, China

AN IN-MEMORY-COMPUTING ARCHITECTURE FOR RECOMMENDATION SYSTEMS

Mengyuan Li, Ann Franchesca Laguna, Dayane Reis, Michael Niemier, X. Sharon Hu, University of Notre Dame, Notre Dame, IN; Xunzhao Yin, Zhejiang University, Hangzhou, China

REGNN: A RERAM-BASED HETEROGENEOUS ARCHITECTURE FOR GENERAL GRAPH NEURAL NETWORKS

Cong Liu, Haikun Liu, Hai Jin, Xiaofei Liao, Yu Zhang, Zhuohui Duan, Jiahong Xu, Huize Li, Huazhong University of Science and Technology, Wuhan, China

HOW FAST CAN YOU GO? IT IS A MAD, MAD, MAD, MAD PLACEMENT WORLD!

Time: 10:30 AM – 12:00 PM
Room: 3007, Level 3
Event Type: Research Manuscript
Topics Area(s): Physical Design and Verification, Lithography and DFM, EDA

Chair/Co-Chair: Siddhartha Nath, Synopsys; TBA

This session covers advanced techniques that accelerate and consider timing for placement. The first paper presents a graph attention network-based floorplanner capable of speeding up subsequent placement, while the second paper gives a fast and extensible global placer using GPU accelerator. The third paper addresses timing driven global placement based on a differentiable timing engine, and the last paper introduces an AQFP-capable placement flow for various timing constraints.

FLOORPLANNING WITH GRAPH ATTENTION

Yiting Liu, Ziyi Ju, Zhengming Li, Mingzhi Dong, Fan Yang, Xuan Zeng, Li Shang, Fudan University, shanghai, China; Hai Zhou, ICBench Inc., Evanston, IL; Jia Wang, Illinois Institute of Technology, Chicago, IL

XPLACE: AN EXTREMELY FAST AND EXTENSIBLE GLOBAL PLACEMENT FRAMEWORK

Lixin Liu, Bangqi Fu, Martin Wong, Evangeline Young, The Chinese University of Hong Kong, Hong Kong

DIFFERENTIABLE TIMING DRIVEN GLOBAL PLACEMENT

Zizheng Guo, Yibo Lin, Peking University, Beijing, China

TAAS: A TIMING-AWARE ANALYTICAL STRATEGY FOR AQFP-CAPABLE PLACEMENT AUTOMATION

Peiyan Dong, Yanyue Xie, Hongjia Li, Mengshu Sun, Yanzhi Wang, Northeastern University, Boston, MA; Olivia Chen, Tokyo City University, Tokyo, Japan; Nobuyuki Yoshikawa, Yokohama National University, Yokohama, Japan

LITTLE DEVICES DOING BIG THINGS: ML TECHNIQUES FOR RESOURCE-CONSTRAINED EMBEDDED DEVICES

Time: 10:30 AM – 12:00 PM
Room: 3004, Level 3
Event Type: Research Manuscript
Topics Area(s): Embedded System Design Methodologies, Embedded Systems

Chair/Co-Chair: Ashish Ranjan, IBM Thomas J. Watson Research Center; Yiyu Shi, University of Notre Dame

Resource-constrained computing remains an important challenge in embedded systems, especially as these systems become more complex and feature-rich. This session covers cutting-edge research to enable efficient computation in emerging embedded systems applications. The first paper proposes a lightweight hardware-aware differentiable network architecture search framework to find the best architecture in a single search pass. The second paper proposes a method to reduce the energy consumption of sensor fusion in difficult autonomous driving contexts. The third paper explores the use of human emotions to facilitate energy-efficient hardware system management in edge devices.

YOU ONLY SEARCH ONCE: ON LIGHTWEIGHT DIFFERENTIABLE ARCHITECTURE SEARCH FOR RESOURCE-CONSTRAINED EMBEDDED PLATFORMS

Xiangzhong Luo, Di Liu, Hao Kong, Shuo Huai, Hui Chen, Weichen Liu, Nanyang Technological University, Singapore

ECOFUSION: ENERGY-AWARE ADAPTIVE SENSOR FUSION FOR EFFICIENT AUTONOMOUS VEHICLE PERCEPTION

Arnav Malawade, Trier Mortlock, Mohammad Al Faruque, University of California, Irvine, CA

EXPLORATION OF HUMAN EMOTION BASED REAL-TIME MEMORY AND COMPUTATION MANAGEMENT ON RESOURCE-LIMITED EDGE DEVICES

Yijie Wei, Zhiwei Zhong, Jie Gu, Northwestern University, Evanston, IL

MACHINE LEARNING FOR RESOURCE MANAGEMENT: FROM EDGE TO CLOUD

Time: 10:30 AM – 12:00 PM
Room: 3000, Level 3
Event Type: Research Manuscript
Topics Area(s): ML Algorithms and Applications, AI, Cloud

Chair/Co-Chair: Jyotikrishna Dass, Rice University; Khadeer Ahmed, Synopsys

HIERARCHICAL MEMORY-CONSTRAINED OPERATOR SCHEDULING OF NEURAL ARCHITECTURE SEARCH NETWORKS

Zihan Wang, Yuting Chen, Shanghai Jiao Tong University, Shanghai, China; Chengcheng Wan, University of Chicago, IL; Ziyi Lin, Alibaba Group, Shanghai, China; He Jiang, Dalian University of Technology, Dalian, China; Lei Qiao, Beijing Institute of Control Engineering, Beijing, China

MIME: ADAPTING A SINGLE NEURAL NETWORK FOR MULTI-TASK INFERENCE WITH MEMORY-EFFICIENT DYNAMIC PRUNING

Abhiroop Bhattacharjee, Yeshwanth Venkatesha, Abhishek Moitra, Priyadarshini Panda, Yale University, New Haven, CT

SNIPER: CLOUD-EDGE COLLABORATIVE INFERENCE SCHEDULING WITH NEURAL NETWORK SIMILARITY MODELING

Weihong Liu, Jiawei Geng, Zongwei Zhu, Jing Cao, Zirui Lian, University of Science and Technology of China, Su Zhou, China

LPCA: LEARNED MRC PROFILING BASED CACHE ALLOCATION FOR FILE STORAGE SYSTEMS

Yibin Gu, Yifan Li, Hua Wang, Li Liu, Ke Zhou, Huazhong University of Science and Technology, Wuhan, China; Wei Fang, Gang Hu, Jinhu Liu, Zhuo Cheng, Huawei, Chengdu, China

ROBUST QUANTUM COMPUTING: WILD GOOSE CHASE?

Time: 10:30 AM – 12:00 PM
Room: 3005, Level 3
Event Type: Research Manuscript
Topics Area(s): Quantum Computing, Design

Chair/Co-Chair: Yufei Ding, University of California, Santa Barbara; Rolf Drechsler, University of Bremen, DFKI

In this session, we have 4 papers covering various aspects of robust quantum computing flow. There are two presentations that address scalable verification approaches by equivalence checking and BDD-based unitary operator manipulation, respectively. Another paper presents the case of handling non-unitaries in equivalence checking of quantum circuits. The last paper of the session proposes a compression technique for reducing resource requirements for topological quantum error correction circuits.

EQUIVALENCE CHECKING PARADIGMS IN QUANTUM CIRCUIT DESIGN: A CASE STUDY

Tom Peham, Lukas Burgholzer, Robert Wille, Johannes Kepler University Linz, Linz, Austria

ACCURATE BDD-BASED UNITARY OPERATOR MANIPULATION FOR SCALABLE AND ROBUST QUANTUM CIRCUIT VERIFICATION

Chun-Yu Wei, Yuan-Hung Tsai, Chiao-Shan Jhang, Jie-Hong Roland Jiang, National Taiwan University, Taipei, Taiwan:

HANDLING NON-UNITARIES IN QUANTUM CIRCUIT EQUIVALENCE CHECKING

Lukas Burgholzer, Robert Wille, Johannes Kepler University Linz, Linz, Austria

A BRIDGE-BASED ALGORITHM FOR SIMULTANEOUS PRIMAL AND DUAL DEFECTS COMPRESSION ON TOPOLOGICALLY QUANTUM-ERROR-CORRECTED CIRCUITS

Wei-Hsiang Tseng, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

STAY (FAR) AWAY FROM MY DEVICE: REMOTE ATTACKS AND DEFENSES

Time: 10:30 AM – 12:00 PM
Room: 3006, Level 3
Event Type: Research Manuscript
Topics Area(s): Hardware Security: Attack and Defense, Security

Chair/Co-Chair: Seetal Potluri, North Carolina State University; TBA

Side-channel analysis exploits information that originate from side-channels such as the power consumption or the timing behavior of a system. This session deals with side-channel attacks and defenses that are exploited remotely. Two papers concentrate on defense mechanisms against timing side-channel attacks in cache memories. One paper exploits speculative execution to bypass existing countermeasures against cache timing side-channel attacks. The fourth paper proposes a defense against remote power side-channel analysis attacks in multi-tenant FPGAs.

FASE: FAST SELECTIVE FLUSHING TO MITIGATE CONTENTION-BASED CACHE TIMING ATTACKS

Tuo Li, Sri Parameswaran, University of New South Wales, Sydney, Australia

CONDITIONAL ADDRESS PROPAGATION: AN EFFICIENT DEFENSE MECHANISM AGAINST TRANSIENT EXECUTION ATTACKS

Peinan Li, Rui Hou, Lutan Zhao, Yifan Zhu, Dan Meng, Chinese Academy of Sciences, Beijing, China

TIMED SPECULATIVE ATTACKS EXPLOITING STORE TO LOAD FORWARDING BYPASSING CACHE-BASED COUNTERMEASURES

Anirban Chakraborty, Debdeep Mukhopadhyay, Indian Institute of Technology, Kharagpur, Kharagpur, India; Nikhilesh Singh, Chester Rebeiro, Indian Institute of Technology, Madras, Madras, India; Sarani Bhattacharya, KU Leuven, Leuven, Belgium

DARPT:DEFENSE AGAINST REMOTE PHYSICAL ATTACK BASED ON TDC IN MULTI-TENANT SCENARIO

Fan Zhang, Zhiyong Wang, Haoting Shen, Bolin Yang, Qianmei Wu, Kui Ren, Zhejiang University, Hangzhou, China

WHAT IS THE ROLE OF THE EDA COMMUNITY IN FUTURE LIFE SCIENCE BREAKTHROUGHS?

Time: 10:30 AM – 12:00 PM
Room: 3001, Level 3
Event Type: Research Panel
Topics Area(s): EDA

Organizer(s): Iris Bahar, Colorado School of Mines, Golden, CO

Moderator: Apurva Kalia, Tufts University, Medford, MA

Biological processes are rapidly becoming better understood. In fact, there is now an increasing application of computational methods to solve several biological processes - from COVID-19 predictions to genome sequencing to drug and vaccine development. Synthetic biology has seen a convergence of chip design and biology. Therefore, it stands to reason that electronic design automation should be a natural contributor to this growth, in both the synthetic biology space, as well as skill and knowledge transfer from electronics design problems to biology problems. However, there continue to be barriers to entry for this convergence. This panel will discuss how the EDA community can get involved. Key topics to be discussed include technological challenges (especially at the interface between electronics and biology), applications wherein there exists a value-added proposition of a hybrid electronic/biological system, challenges for large scale deployment of such systems for expedited diagnostics and/or drug/vaccine development, applying knowledge and skills from already solved electronic problems to biology problems and questions related to ethical issues as well as privacy/security in such systems.

Panels: Lou Scheffer, HHMI, Chevy Chase, MD; Jacob Beal, Raytheon Technologies, Iowa City, IA; Kate Adamala, University of Minnesota, MN; Sameer Sonkusale, Tufts University, Medford, MA

COMPUTING-IN-MEMORY: INDUSTRY PERSPECTIVES

Time: 10:30 AM – 12:00 PM
Room: 3003, Level 3
Event Type: Special Session (Research)
Topics Area(s): Embedded Systems

Organizer(s): Swagath Venkataramani, IBM T.J. Watson Research Center, West Lafayette, IN

Data-intensive applications in critical domains such as deep learning, bioinformatics, and data analytics have posed significant challenges to traditional computing systems. The large working set of these workloads lead to frequent data transfers between the memory and computing sub-systems substantially limiting overall performance and efficiency. Compute-in-memory is a new design paradigm that alleviates the processor-memory (von Neumann) bottleneck by directly embedding computing capabilities within the memory sub-system. Computing-in-memory systems require innovations throughout the compute stack starting from primitive compute devices and circuits, architecture design and software. Numerous

Computing-in-memory designs across memory technologies (SRAM, DRAM, NAND Flash, ReRAM, PCM, MRAM) have been explored in the research community. Beyond academic prototypes, Computing-in-memory is beginning to be embraced by the semiconductor industry through compelling research demonstrations and roadmaps. This special session aims to bring together experts from leading companies to share their views on the prospects and challenges in developing and adopting Computing-in-memory technologies.

ACCELERATING DEEP NEURAL NETWORKS WITH ANALOG-MEMORY-BASED HARDWARE ACCELERATORS: TECHNOLOGY, ALGORITHMS AND ARCHITECTURE

Stefano Ambrogio, IBM, San Jose, CA

MRAM IN-MEMORY COMPUTING CROSSBAR ARRAY

Seungchul Jung, Samsung Electronics, City, CA

CHALLENGES AND OPPORTUNITIES FOR IN-MEMORY COMPUTE

Ameen Akeel, Micron, City, ID

CO-DESIGN FOR EDGE INTELLIGENCE: PERCEPTION, CONTROL, COMPUTING

Time: 11:30 AM – 12:30 PM
Room: DAC Pavilion, Level 2 Exhibit Hall
Event Type: Tech Talk
Topics Area(s): Autonomous Systems

Autonomous vehicles combine machine learning-based perception with planning and control. Co-design introduces the opportunity for new types of optimizations for perception that range across accuracy, execution time, and power consumption. The requirements on embedded computer vision for autonomy include accuracy, latency, and power consumption. These requirements interact---for example, long latencies can interfere with control performance. This talk will explore the use of co-design to create highly capable and efficient autonomous systems.

Speaker: Marilyn Wolf, University of Nebraska, Lincoln, NE

IT'S GETTING CLOUDY OUT THERE

Time: 1:00 PM – 1:45 PM
Room: DAC Pavilion, Level 2 Exhibit Hall
Event Type: SKYTalk
Topics Area(s): Cloud, Design

Cloud is everywhere - for chip design, companies large, medium, and small are evaluating their options in using high-performance computing (HPC) infrastructure to accelerate and differentiate their designs. In this session, we will discuss the drivers and challenges of moving EDA workloads to the cloud and how leading design teams are maximizing the benefits of moving to the cloud.

Speaker: Sandeep Mehndiratta, Synopsys, Palo Alto, CA

LIFECYCLE OF DESIGN ELEMENTS

Time: 1:30 PM – 3:00 PM
Room: 2008, Level 2
Event Type: Engineering Tracks
Topics Area(s): Back-End Design

Chair/Co-Chair: Divya Prasad, AMD

CHARACTERIZATION CHALLENGES IN SYSTEM LEVEL IO INTERFACE

Harsh Garg, STMicroelectronics, Patiata, India; Natish Singla, Saurabh Srivastava, STMicroelectronics, Noida, India; Mihir Pratap, STMicroelectronics, Delhi, India; Matthieu Fillaud, Siemens EDA, Grenoble, France

NOVEL DESIGN OF REAL TIME CLOCK MACRO FOR ADVANCED FINFET TECHNOLOGY NODES

Krishnan Sukumar, Animesh Jain, Ravindra Ayyagari, Santosh Vodnala, Rajesh R, AMD India Pvt Ltd, Bengaluru, India

PYTHON BASED STANDALONE TOOLKIT FOR STANDARD CELL LIBRARY & RTL POWER STATISTICAL ANALYSIS

Aman Jain, Guneet Singh, Intel Technology India Pvt. Ltd, Bengaluru, India

THERMAL-AWARE POWER AND PERFORMANCE SIMULATOR

Yunhyeok Im, Samsung Electronics, Hwaseong-si, South Korea

THERMAL TUNING POWER BUDGETING WITH STATISTICAL AND TEMPERATURE VARIATION FOR MICRORING-BASED DWDM 3D SILICON PHOTONICS

Jinsung Youn, Marco Fiorentino, Hewlett Packard Enterprise, Milpitas, CA; Ahsan Alam, Leanne Dias, Zeqin Lu, James Pond, Ansys, Vancouver, Canada; Norman Chang, Ansys, San Jose, CA; Raymond Beausoleil, Hewlett Packard Enterprise, Seattle, WA

AN AREA AND TEST-TIME EFFICIENT IN-FIELD MEMORY TEST FRAMEWORK WITH TUNABLE GUARD BANDS

Devanathan Varadarajan, Texas Instruments, Dallas, TX; Frank Cano, Texas Instruments, Sugar Land, TX

DESIGNING AND VERIFYING FOR POWER AT THE FRONT END

Time: 1:30 PM – 3:00 PM
Room: 2010, Level 2
Event Type: Engineering Tracks
Topics Area(s): Front-End Design

Chair/Co-Chair: Krish Sundaresan, Ampere

MAXIMIZE GPGPU PERFORMANCE-PER-WATT ACROSS REAL SCENARIOS WITH 10X EFFICIENT POWER SOLUTION

Sushil Mittal, Shixuan Que, Ling Sun, Lili Dai, Yuanyuan Ling, Iluvatar, Shanghai, China; Zhenbang Wang, Ansys, Pittsburgh, PA

INNOVATIVE LOW POWER UPF GENERATION AND HIERARCHICAL MODELING OF CUSTOM BLOCKS

Archanna Srinivasan, Intel Corporation, SAN JOSE, CA; Mei War Kan, Intel Corporation, Bayan Lepas, Singapore

FULLY AUTOMATED MODULAR METHOD FOR COMPREHENSIVE LOW POWER SIMULATION COVERAGE

Harsh Sharma, Texas Instruments, Banglore, India; Sooraj Sekhar, Texas Instruments (India) Pvt. Ltd., Bengaluru, India; Parth Shah, Texas Instruments (India) Pvt. Ltd., Mumbai, India; Lakshmanan Balasubramanian, Texas Instruments (India) Pvt. Ltd., Bengaluru, India; Venkatraman Ramakrishnan, Texas Instruments (India) Pvt. Ltd., Bengaluru, India

LOW POWER CLASSES AS EXTENSION TO UVM PACKAGE LIBRARY

Shikhadevi Katharia, Silicon Interfaces, Mumbai, India; Avnita Pal, Silicon Interfaces, Mumbai, India; Suchitha A S, Silicon Interfaces, Mumbai, India; Swetha Chiliveri, Silicon Interfaces, Mumbai, India

CAPABILITIES

Zhi Sheng Teh, Intel Corporation, Kedah, Malaysia; Arthur Kalsing, Defacto Technologies, East York, Canada

LEARNING-BASED POWER MODELING FOR VERSAL AI ENGINE

Seokjoong Kim, AMD, San Jose, CA; Tim Tuan, AMD, San Jose, CA

RISC-V: OPEN AND FLEXIBLE, BUT STILL A STANDARD? HOW WELL HAS RISC-V PERFORMED AS AN OPEN STANDARD ISA THAT ENCOURAGES INNOVATION WITHOUT CHAOS AND FRAGMENTATION?

Time: 1:30 PM – 3:00 PM
Room: 2012, Level 2
Event Type: Engineering Tracks
Topics Area(s): IP, RISC-V

Organizer(s): Himanshu Sanghavi, Meta, Fremont, CA

Moderator: Edward Sperling, Semiconductor Engineering, San Jose, CA

The RISC-V ISA was born out of academic research in 2010. Today, there are many commercial and open-source vendors of RISC-V IP, hardware and software. Many semiconductor and systems companies have deployed RISC-V based processors ranging from tiny microcontrollers to data center server class designs. The factors driving this unprecedented interest in RISC-V include the promise of lower total cost of ownership and the availability of hardware from multiple vendors providing solutions across the area/performance/energy curve. The ability of customers to add their custom ISA extensions, the promise of software portability between different implementations and the availability of software development tools from multiple independent vendors, including open-source developers, are addition attractions of RISC-V. But have the promises of RISC-V panned out for commercial users of RISC-V IP cores in actual deployments? Is there a lower total cost of ownership? Has anyone had a “seamless” software porting experience across HW/IP suppliers? Is the software development ecosystem demonstrably better than other ISAs? The panel will discuss the current state of the RISC-V ecosystem from the perspectives of hardware and software IP vendors as well as users/customers.

Presenters: Pierre Selwan, Microchip, Fremont, CA; Yunsup Lee, SiFive, San Francisco, CA; Hong-Men Charlie Hsu, Andes, Hsinchu City, Taiwan; Larry Lapides, Imperas, Dublin, CA; Jim Wang, Meta, San Francisco, CA

ACCELERATING THE INFERENCE: TRANSFORMERS, GRAPHS AND OTHERS

Time: 1:30 PM – 3:00 PM
Room: 3002, Level 3
Event Type: Research Manuscript
Topics Area(s): AI/ML Design: Circuits and Architecture, Design

Chair/Co-Chair: Muhammad Shafique, New York University, Abu Dhabi; Jeff (Jun) Zhang, Harvard University

GNNIE: GNN INFERENCE ENGINE WITH LOAD-BALANCING AND GRAPH-SPECIFIC CACHING

Sudipta Mondal, Susmita Dey Manasi, Kishor Kunal, Ramprasath S, Sachin S. Sapatnekar, University of Minnesota, Minneapolis, MN

SALO: AN EFFICIENT SPATIAL ACCELERATOR ENABLING HYBRID SPARSE ATTENTION MECHANISMS FOR LONG SEQUENCES

Guan Shen, Jieru Zhao, Quan Chen, Jingwen Leng, Chao Li, Minyi Guo, Shanghai Jiao Tong University, Shanghai, China

NN-LUT: NEURAL APPROXIMATION OF NON-LINEAR OPERATIONS FOR EFFICIENT TRANSFORMER INFERENCE

Joonsang Yu, NAVER CLOVA, Seoul, South Korea; Junki Park, Samsung Electronics, Suwon, South Korea; Seongmin Park, Minsoo Kim, Sihwa Lee, Jungwook Choi, Hanyang University, Seoul, South Korea; Dong Hyun Lee, Samsung Electronics, Seoul, South Korea

SELF ADAPTIVE RECONFIGURABLE ARRAYS (SARA): LEARNING FLEXIBLE GEMM ACCELERATOR CONFIGURATION AND MAPPING-SPACE USING ML

Ananda Samajdar, Eric Qin, Tushar Krishna, Georgia Institute of Technology, Atlanta, GA; Michael Pellauer, NVIDIA, Boston, MA

BE WATER: ADAPTIVE AI FOR DYNAMIC SYSTEMS

Time: 1:30 PM – 3:00 PM
Room: 3005, Level 3
Event Type: Research Manuscript
Topics Area(s): AI/ML Design: System and Platform, Design

Chair/Co-Chair: Xiang Chen, George Mason University; TBA

ENABLING HARD CONSTRAINTS IN DIFFERENTIAL NEURAL NETWORK AND ACCELERATOR CO-SEARCH

Deokki Hong, Kanghyun Choi, Hye Yoon Lee, Joonsang Yu, Noseong Park, Youngsok Kim, Jinho Lee, Yonsei University, Seoul, South Korea; NAVER CLOVA, Seoul, South Korea

HEURISTIC ADAPTABILITY TO INPUT DYNAMICS FOR SPMM ON GPUS

Guohao Dai, Shang Yang, Zhongming Yu, Hengrui Zhang, Huazhong Yang, Yu Wang, Tsinghua University, Wuhan, China; Guyue Huang, Yufei Ding, Yuan Xie, University of California, Santa Barbara, CA

H2H: HETEROGENEOUS MODEL TO HETEROGENEOUS SYSTEM MAPPING WITH COMPUTATION AND COMMUNICATION AWARENESS

Xinyi Zhang, Peipei Zhou, Alex Jones, Jingtong Hu, University of Pittsburgh, PA; Cong Hao, Georgia Institute of Technology, Atlanta, GA

PARIS AND ELSA: AN ELASTIC SCHEDULING ALGORITHM FOR RECONFIGURABLE MULTI-GPU INFERENCE SERVERS

Yunseong Kim, Yujeong Choi, Minsoo Rhu, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea

FROM MACHINE LEARNING TO GRAPHS: A NEW WAVE TOWARDS ANALOG DESIGN

Time: 1:30 PM – 3:00 PM
Room: 3004, Level 3
Event Type: Research Manuscript
Topics Area(s): Analog Design, Simulation, Verification and Test, AI, EDA

Chair/Co-Chair: Jiang Hu (Texas A&M University); Umamaheswara Rao Tida (North Dakota State University)

PURSUING MORE EFFECTIVE GRAPH SPECTRAL SPARSIFIERS VIA APPROXIMATE TRACE REDUCTION

Zhiqiang Liu, Wenjian Yu, Tsinghua University, Beijing, China

ACCELERATING DC CIRCUIT SIMULATION WITH REINFORCEMENT LEARNING

Zhou Jin, Haojie Pei, China University of Petroleum, Beijing, China; Yichao Dong, Dan Niu, Southeast University, Nanjing, China; Xiang Jin, Beihang University, Beijing, China; Xiao Wu, Huada Empyrean Software Co. Ltd, Beijing, China; Wei Xing, Beihang University, Beijing, China

A FINE-TUNING ASSISTED LAYOUT SIZING SCHEME FOR ANALOG/RF CIRCUITS

Zhikai Wang, Wenfei Hu, Zuochang Ye, Wenyuan Zhang, Ruitao Wang, Jian Zhang, Yang Wang, Tsinghua University, Shang Hai, China; Jingbo Zhou, Dejing Dou, Baidu Research, Beijing, China;

AN EFFICIENT YIELD OPTIMIZATION METHOD FOR ANALOG CIRCUITS VIA GAUSSIAN PROCESS CLASSIFICATION AND VARYING-SIGMA SAMPLING

Xiaodong Wang, Changhao Yan, Fan Yang, Xuan Zeng, Fudan University, Shanghai, China; Dian Zhou, The University of Texas at Dallas, Richardson, TX

LEARN ABOUT ADVANCED PLACEMENT ALGORITHMS FOR HYPERSCALER CHIPS!

Time: 1:30 PM – 3:00 PM
Room: 3007, Level 3
Event Type: Research Manuscript
Topics Area(s): Physical Design and Verification, Lithography and DFM, Design

Chair/Co-Chair: Wuxi Li, AMD

PARTITION AND PLACE FINITE ELEMENT MODEL ON WAFER SCALE ENGINE

Jinwei Liu, Xiaopeng Zhang, Shiju Lin, Xinshi Zang, Jingsong Chen, Bentian Jiang, Martin Wong, Evangeline Young, The Chinese University of Hong Kong, Hong Kong

CNN-INSPIRED ANALYTICAL GLOBAL PLACEMENT FOR LARGE-SCALE HETEROGENEOUS FPGAS

Huimin Wang, Xingyu Tong, Chenyue Ma, Runming Shi, Jianli Chen, Kun Wang, Jun Yu, Fudan University, Shanghai, China; Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

HIGH-PERFORMANCE PLACEMENT FOR LARGE-SCALE HETEROGENEOUS FPGAS WITH CLOCK CONSTRAINTS

Ziran Zhu, Yangjie Mei, Southeast University, Nanjing, China; Zijun Li, Jingwen Lin, Fuzhou University, Fuzhou, China; Jianli Chen, Fudan University, Shanghai, China; Jun Yang, Southeast University, Nanjing, China; Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

MULTI-ELECTROSTATIC FPGA PLACEMENT CONSIDERING SLICEL-SLICEM HETEROGENEITY AND CLOCK FEASIBILITY

Jing Mai, Yibai Meng, Yibo Lin, Peking University, Beijing, China; Zhixiong Di, Southwest Jiaotong University, Chengdu, China

PUSHING THE BOUNDARIES OF PRACTICAL AI: EFFICIENCY AND ROBUSTNESS

Time: 1:30 PM – 3:00 PM
Room: 3000, Level 3
Event Type: Research Manuscript
Topics Area(s): ML Algorithms and Applications, AI

Chair/Co-Chair: Yingyan Lin, Rice University; TBA

ON-CHIP QNN: TOWARDS EFFICIENT ON-CHIP TRAINING OF QUANTUM NEURAL NETWORKS

Hanrui Wang, Song Han, Massachusetts Institute of Technology, Cambridge, CT; Zirui Li, Shanghai Jiao Tong University, Shanghai, China; Jiaqi Gu, David Z. Pan, The University of Texas at Austin, TX; Yongshan Ding, Yale University, New Haven, CT;

MEMORY-EFFICIENT TRAINING OF BINARIZED NEURAL NETWORKS ON THE EDGE

Mikail Yayla, Technische Universität Darmstadt, Darmstadt, Germany; Jian-Jia Chen, Technische Universität Dortmund, Dortmund, Germany

DEEPGATE: LEARNING NEURAL REPRESENTATIONS OF LOGIC GATES

Min Li, Sadaf Khan, Zhengyuan Shi, Qiang Xu, The Chinese University of Hong Kong, Hong Kong, Hong Kong; Naixing Wang, Yu Huang, HiSilicon, Shenzhen, China

BIPOLAR VECTOR CLASSIFIER FOR FAULT-TOLERANT DEEP NEURAL NETWORKS

Suyong Lee, Sungkyunkwan University, Suwon-si, South Korea; Insu Choi, Joon-Sung Yang, Yonsei University, Seoul, South Korea

SECURITY OF AI AND AI FOR SECURITY

Time: 1:30 PM – 3:00 PM
Room: 3006, Level 3
Event Type: Research Manuscript
Topics Area(s): Hardware Security: Attack and Defense, Security

Chair/Co-Chair: Sri Parameswaran, UNSW; TBA

HDLOCK: EXPLOITING PRIVILEGED ENCODING TO PROTECT HYPERDIMENSIONAL COMPUTING MODELS AGAINST IP STEALING

Shijin Duan, Xiaolin Xu, Northeastern University, Boston, MA; Shaolei Ren, University of California, Riverside, Riverside, CA

TERMINATOR ON SKYNET: A PRACTICAL DVFS ATTACK ON DNN HARDWARE IP FOR UAV OBJECT DETECTION

Junge Xu, Bohan Xuan, Anlin Liu, Mo Sun, Fan Zhang, Zeke Wang, Kui Ren, Zhejiang University, Hangzhou, China

AL-PA: CROSS-DEVICE PROFILED SIDE-CHANNEL ATTACK USING ADVERSARIAL LEARNING

Pei Cao, Hongyi Zhang, Dawu Gu, Shanghai Jiao Tong University, Shanghai, China; Yan Lu, State Grid Liaoning Electric Power Company Limited Electric Power Research Institute, Shenyang, China; Yidong Yuan, Beijing Smartchip Microelectronics Technology Company Limited, Beijing, China

DETERRENT: DETECTING TROJANS USING REINFORCEMENT LEARNING

Vasudev Gohil, Satwik Patnaik, Hao Guo, Dileep Kalathil, Jeyavijayan Rajendran, Texas A&M University, College Station, TX

CRYOGENIC COMPUTING, SUPER COOL OR NOT?

Time: 1:30 PM – 3:00 PM
Room: 3001, Level 3
Event Type: Research Panel
Topics Area(s): Design

Organizer(s): Jaydeep Kulkarni, The University of Texas at Austin, TX

Moderator: Suman Datta, University of Notre Dame, Notre Dame, IN

Currently, data center power consumption accounts for over 1% of the world's energy usage. With this figure expected to increase significantly over the next decade, it is imperative to identify new ways to reduce computing power consumption. With recent advancements in cryogenic cooling technology, it is timely to explore the applicability of cryogenic computing technologies in solving the data center energy problem. Additionally, such cryogenic systems could also have applications in quantum computing. Such quantum computers offer the promise to provide an exponential speedup for certain compute applications, which are pervasive across multiple segments of the economy. Low-temperature CMOS operation results in higher threshold voltage and improved subthreshold slope, leading to low leakage power consumption. Despite these advantages, cryogenic CMOS operations need to operate at moderately higher supply voltage due to higher threshold voltage for achieving the same operating frequency. Higher supply voltage leads to higher switching energy dissipation resulting in increased cooling cost. Hence, there is a critical need to investigate the usefulness of cryogenic computing across various bottom-up levels of abstractions (process, device, circuits, EDA) and from top-down application-level perspectives (such as quantum computing, high-performance computing CMOS booster). This panel brings together leading researchers in this field to provide their perspective on this timely and important topic which would benefit the entire DAC community.

Panelists: Jamil Kawa, Synopsys, Mountain View, AL; Effendi Leobandung, IBM Research, Albany, NY; Ravi Pillarisetty, Intel Corporation, Portland, OR; Arijit Raychowdhury, Georgia Institute of Technology, Atlanta, GA

BREAKING DOWN PHYSICAL DESIGN BARRIERS WITH OPEN AND AGILE FLOW TOOLS

Time: 1:30 PM – 3:00 PM
Room: 3003, Level 3
Event Type: Special Session (Research)
Topics Area(s): EDA

Organizer(s): Christopher Batten, Cornell University, Ithace, NY

HAMMER: A MODULAR AND REUSABLE PHYSICAL DESIGN FLOW TOOL

Harrison Liew, Daniel Grubb, John Wright, Colin Schmidt, Nayiri Krzysztofowicz, Adam Izraelevitz, Edward Wang, Krste Asanovic, Jonathan Bachrach, Borivoje Nikolic, University of California, Berkeley, CA

MFLOWGEN: A MODULAR FLOW GENERATOR AND ECOSYSTEM FOR COMMUNITY-DRIVEN PHYSICAL DESIGN

Alex Carsello, James Thomas, Ankita Nayak, Po-Han Chen, Mark Horowitz, Priyanka Raina, Christopher Torng, Stanford University, Stanford, CA

A DISTRIBUTED APPROACH TO SILICON COMPILATION

Andreas Olofsson, William Ransohoff, Noah Moroze, Zero ASIC, Boston, MA

BESPOKE SILICON – TAILOR-MADE FOR MAXIMUM PERFORMANCE

Time: 2:00 PM – 2:45 PM
Room: DAC Pavilion, Level 2 Exhibit Hall
Event Type: DAC Pavilion Panel
Topics Area(s): Embedded Systems

Moderator: John Lee, Ansys, San Jose, CA

Bespoke (or tailored) silicon refers to chips and 3D-IC systems developed by a company for its exclusive use in its systems. Leading system companies such as Google, Tesla, Amazon, Apple and Microsoft have newly built or acquired IC design teams to design bespoke silicon to give themselves an advantage over their competitors using off-the-shelf chips. They are bringing their systems expertise into the 3D-IC chip design world and this is changing the dynamics of the semiconductor market in sometimes unexpected ways. This Pavilion roundtable gathers senior designers of Bespoke Silicon to discuss their motivations and experiences in this emerging market.

Panelists: Prashant Varshney, Microsoft, Washington, DC; Mathew Kaipanatu, Google, Bengaluru, India; Kam Kittrell, Cadence Design Systems, Inc., Austin, TX

GOOGLE CLOUD TRAINING

Time: 2:15 PM – 5:15 PM
Room: Design on Cloud Pavilion, Level 2 Exhibit Hall
Event Type: Design on Cloud Training
Topics Area(s):

Join Google Cloud for an interesting and interactive Google Cloud hands-on workshop. Google Cloud experts will start from basic concepts and help you build a scalable setup for EDA infrastructure on Google Cloud - step by step. You will learn about Cloud fundamentals and concepts, understand the cost aspects of relevant offerings, and do the following hands-on

- Configure & understand basic IAM and Security
- Setup basic Cloud Networking
- Create and Scale with Virtual Machines (VMs) - Type of VMs, Custom VMs, Images
- Create different types of Storage options – Cloud, File, and Block storage

Besides the hands-on setup, we will also review and discuss EDA on GCP Architecture options for Burst setup.

Presenter: Peeyush Tugnawat, Google, San Jose, CA

HOW ROBUST IS YOUR HARDWARE SECURITY PROGRAM?

Time: 3:00 PM – 3:45 PM
Room: DAC Pavilion, Level 2 Exhibit Hall
Event Type: DAC Pavilion Panel
Topics Area(s): Security

Moderator: Andreas Kuehlmann, Tortuga Logic, San Francisco, CA

Establishing semiconductor security is a relatively new requirement. It is not just about inserting a hardware root of trust into the chip and trusting it to provide complete security assurance. It is also not another engineering task like validating functionality, timing, power, etc. that can simply be delegated to the R&D team. Security has many stakeholders ranging from marketing & product management, product security, engineering, and legal & compliance. As a result, building security into a chip is more than a technical problem and poses new organizational as well as process challenges. Establishing an effective and scalable security program starts with aligning the key stakeholders on the business objectives and continues with compiling them into technical requirements, validating their correct implementation throughout the design process and finally obtaining security signoff from all participants. In this panel we discuss key technical, organizational, and process challenges encountered in the emerging field of semiconductor security and how to build an effective security program addressing them. The panelist includes security experts and practitioners with diverse backgrounds and from leading semiconductor design organizations.

Panels: Debra Delise, Analog Devices, Tampa, FL; Jason Fung, Intel Corporation, Santa Clara, CA; Joe Tostenrude, Microsoft, Irvine, CA; Vivek Vedula, Arm Ltd., Austin, TX

PUSHING BOUNDARIES – CHALLENGES FOR NEXT-GENERATION CHIP DESIGN

Time: 3:30 PM – 5:00 PM
Room: 2008, Level 2
Event Type: Engineering Tracks
Topics Area(s): Back-End Design

Chair/Co-Chair: Sabya Das, Synopsys

Advanced technology nodes such as 5nm and 3nm, 2.5D/3D stacking, MCMs, and design size - all pose unique challenges for EDA tools, design methodologies, integration, and testing. This session show cases real-world challenges and solutions for next-generation high-performance chip design and test in both 2.xD and 3D. Talks feature leading-edge back-end design flows, disaggregated product architecture methodologies, and test solutions for high bandwidth memories.

Presenters: Jeanne Trinko-Mechler, Marvell Semiconductor, Essex Junction, VT; Sabyasachi Dey, Intel Corporation, Hillsboro, OR; Sandeep Bhatia, Google, San Jose, CA

DIGITAL TWIN REIMAGINED – ONE MODEL TO RULE THEM ALL?

Time: 3:30 PM – 5:00 PM
Room: 2010, Level 2
Event Type: Engineering Tracks
Topics Area(s): Front-End Design

Organizer(s): Anoop Saha, Siemens EDA

Moderator: Anoop Saha, Siemens EDA

This DAC special session will present the opportunities but also the challenges of bringing together Digital Twin technologies with semiconductor, electronics HW and SW development techniques. Different speakers will cover the characteristics of a Digital Twin, the available modeling, simulation and virtualization platforms, and proposals how to efficiently integrate the different models and/or frameworks to shape the Digital Twin ecosystem.

Panelists: Bryan Ramirez, Siemens EDA, Windsor, CO; Manfred Thanner, NXP Semiconductors, Austin, TX; Fred Hannert, General Motors, Milford, MI

BUILD BACK SECURE - ARCHITECTURE INFRASTRUCTURE FOR SECURITY

Time: 3:30 PM – 5:30 PM
Room: 3005, Level 3
Event Type: Research Manuscript
Topics Area(s): Hardware Security: Primitives, Architecture, Design & Test, RISC-V, Security

Chair/Co-Chair: TBA

Building secure architectures for current and next-gen computing systems requires novel methods in addition to rethinking of current practices. The presentations in this session build back more secure computing architectures through techniques that protect data from the memory and compute units through the instruction level and operating system. In addition, architectures that leverage post-quantum cryptography algorithms will also be presented.

EXPLOITING DATA LOCALITY IN MEMORY FOR ORAM TO REDUCE MEMORY ACCESS OVERHEADS

Jinxi Kuang, Minghua Shen, Yutong Lu, Nong Xiao, Sun Yat-Sen University, Guangzhou, China

HWST128: COMPLETE MEMORY SAFETY ACCELERATOR ON RISC-V WITH METADATA COMPRESSION

Hsu-Kang Dow, Tuo Li, Sri Parameswaran, University of New South Wales, Sydney, Australia

REGVAULT: HARDWARE ASSISTED SELECTIVE DATA RANDOMIZATION FOR OPERATING SYSTEM KERNELS

Jinyan Xu, Haoran Lin, Ziqi Yuan, Wenbo Shen, Yajin Zhou, Rui Chang, Lei Wu, Kui Ren, Zhejiang University, Hangzhou, China

RECONCILING ASYNCHRONOUS REAL-TIME OPERATIONS AND PROOFS OF EXECUTION IN SIMPLE EMBEDDED SYSTEMS

Adam Caulfield, Ivan De Oliveira Nunes, Rochester Institute of Technology, Rochester, NY; Norrathep Rattanavipanon, Prince of Songkla University, Phuket, Thailand;

TOWARDS A FORMALLY VERIFIED HARDWARE ROOT-OF-TRUST FOR DATA-OBLIVIOUS COMPUTING

Lucas Deutschmann, Johannes Müller, Mohammad Rahmani Fadiheh, Dominik Stoffel, Wolfgang Kunz, Technische Universität Dresden, Kaiserslautern, Germany

A SCALABLE SIMD RISC-V BASED PROCESSOR WITH CUSTOMIZED VECTOR EXTENSIONS FOR CRYSTALS-KYBER

Huimin Li, Stjepan Picek, Technische Universität Delft, Delft, Netherlands; Nele Mentens, KU Leuven, Leuven, Belgium;

FUTURE UNLEASHED: BEYOND-CMOS MEETS THE REAL WORLD

Time: 3:30 PM – 5:30 PM
Room: 3002, Level 3
Event Type: Research Manuscript
Topics Area(s): Emerging Device Technologies, Design

Chair/Co-Chair: Hussam Amrouch, University of Stuttgart; TBA

The session covers a wide range of emerging technologies, starting from ferroelectric transistors and resistive memories all the way to more long-term quantum dots and Skyrmion gates. The session aims at demonstrating the promise of such emerging technologies along with the new challenges that they bring to EDA. The session will present five papers, starting with novel ferroelectric-based CAM cell design and new design automation methodologies for silicon dangling bond logic. It will then also cover how ICs can be protected using camouflaged Skyrmion gates and how novel graph neural network algorithms can be employed to increase prediction accuracy in microfluidic chips. Finally, a novel error correction scheme to increase the reliability of compute-in-memory circuits is presented.

HEXAGONS ARE THE BESTAGONS: DESIGN AUTOMATION FOR SILICON DANGLING BOND LOGIC

Marcel Walter, Technische Universität München, Munich, Germany; Samuel Ng, Konrad Walus, University of British Columbia, Vancouver, Canada; Robert Wille, Johannes Kepler University Linz, Linz, Austria

IMPROVING COMPUTE IN-MEMORY ECC RELIABILITY WITH SUCCESSIVE CORRECTION

Brian Crafton, Zishen Wan, Samuel Spetalnick, Arijit Raychowdhury, Georgia Institute of Technology, Atlanta, GA; Jong-Hyeok Yoon, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea; Wei Wu, Carlos Tokunaga, Vivek De, Intel Corporation, Hillsboro, OR

ENERGY EFFICIENT DATA SEARCH DESIGN AND OPTIMIZATION BASED ON A COMPACT FERROELECTRIC FET CONTENT ADDRESSABLE MEMORY

Jiahao Cai, Zhejiang University, Hangzhou, China; Mohsen Imani, University of California, Irvine, CA; Kai Ni, Rochester Institute of Technology, Rochester, NY; Grace Li Zhang, Bing Li, Ulf Schlichtmann, Technische Universität München, Germany; Cheng Zhuo, Xunzhao Yin, Zhejiang University, Hangzhou, China

CAMSKYGATE: CAMOUFLAGED SKYRMION GATES FOR PROTECTING ICS

Yuqiao Zhang, Chunli Tang, Peng Li, Ujjwal Guin, Auburn University, Auburn, AL

GNN-BASED CONCENTRATION PREDICTION FOR RANDOM MICROFLUIDIC MIXERS

Weiqing Ji, Xingzhuo Guo, Shouan Pan, Hailong Yao, Tsinghua University, Beijing, China; Tsung-Yi Ho, The Chinese University of Hong Kong, Hong Kong; Ulf Schlichtmann, Technische Universität München, Munich, Germany

HARDWARE SECURITY POTPOURRI: LOGIC LOCKING, HARDWARE TROJANS, AND MEMORY ATTACKS

Time: 3:30 PM – 5:30 PM
Room: 3006, Level 3
Event Type: Research Manuscript
Topics Area(s): Hardware Security: Attack and Defense, Hardware Security: Primitives, Architecture, Design & Test, AI, Security

Chair/Co-Chair: TBA

DESIGNING ML-RESILIENT LOCKING AT REGISTER-TRANSFER LEVEL

Dominik Sisejkovic, Rainer Leupers, RWTH Aachen University, Aachen, Germany; Luca Collini, Christian Pilato, Politecnico di Milano, Milan, Italy; Benjamin Tan, University of Calgary, Calgary, Canada; Ramesh Karri, New York University, New York, NY

O'CLOCK: LOCK THE CLOCK VIA CLOCK-GATING FOR SOC IP PROTECTION

Mohammad Rahman, Rui Guo, Hadi Mardani Kamali, Fahim Rahman, Farimah Farahmandi, Mark Tehranipoor, University of Florida, Gainesville, FL; Mohamed Abdel-Moneum, Intel Corporation, Hillsboro, OR

ALICE: AN AUTOMATIC DESIGN FLOW FOR EFPGA REDACTION

Chiara Muscari Tomajoli, Luca Collini, Christian Pilato, Politecnico di Milano, Milan, Italy; Jitendra Bhandari, Abdul Khader Thalakkattu Moosa, Ramesh Karri, New York University, New York, NY; Benjamin Tan, University of Calgary, Calgary, Canada; Xifan Tang, Pierre-Emmanuel Gaillardon, University of Utah, Salt Lake City, UT

DELTA: DESIGNING A STEALTHY TRIGGER MECHANISM FOR ANALOG HARDWARE TROJANS AND ITS DETECTION ANALYSIS

Nishant Gupta, Mohil Desai, Mark Wijtvliet, Shubham Rai, Akash Kumar, Technische Universität Dresden, Dresden, Germany

VIPR-PCB: A MACHINE LEARNING BASED GOLDEN-FREE PCB ASSURANCE FRAMEWORK

Aritra Bhattacharyay, Prabuddha Chakraborty, Jonathan Cruz, Swarup Bhunia, University of Florida, Gainesville, FL

CLIMBER: DEFENDING PHASE CHANGE MEMORY AGAINST INCONSISTENT WRITE ATTACKS

Zhuohui Duan, Haobo Wang, Haikun Liu, Xiaofei Liao, Hai Jin, Yu Zhang, Fubing Mao, Huazhong University of Science and Technology, Wuhan, China

IS PERSISTENT MEMORY REAL?

Time: 3:30 PM – 5:30 PM
Room: 3004, Level 3
Event Type: Research Manuscript
Topics Area(s): Embedded Memory, Storage and Networking, Embedded Systems

Chair/Co-Chair: Jingtong Hu, University of Pittsburgh; TBA

This session includes presentations from leading-edge research on logic locking techniques, hardware Trojans and memory attacks. Two logic locking papers investigate locking mechanisms at the register transfer level (RTL) and via clock gating. In the third presentation, RTL modules are used among multiple reconfigurable fabrics to protect intellectual property. Trojan detection techniques for stealthy Trojans are presented in the fourth paper. The fifth presentation shows a machine learning based PCB assurance technique. The session ends with the presentation of a novel countermeasure to protect memory against inconsistent write attacks.

RETHINKING KEY-VALUE STORE FOR BYTE-ADDRESSABLE OPTANE PERSISTENT MEMORY

Sung-Ming Wu, Li-Pin Chang, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

LIBCRPM: IMPROVING THE CHECKPOINT PERFORMANCE OF NVM

Feng RenKang Chen, Yongwei Wu, Tsinghua University, Beijing, China

SCALABLE CRASH CONSISTENCY FOR SECURE PERSISTENT MEMORY

Ming Zhang, Yu Hua, Xuan Li, Hao Xu, Huazhong University of Science and Technology, Wuhan, China

DON'T OPEN ROW: RETHINKING ROW BUFFER POLICY FOR IMPROVING PERFORMANCE OF NON-VOLATILE MEMORIES

Yongho Lee, Osang Kwon, Seokin Hong, Sungkyunkwan University, Suwon, South Korea

SMART: ON SIMULTANEOUSLY MARCHING RACETRACKS TO IMPROVE THE PERFORMANCE OF RACETRACK-BASED MAIN MEMORY

Xiangjun Peng, Ming-Chang Yang, Ho Ming Tsui, Chi Ngai Leung, The Chinese University of Hong Kong, Hong Kong; Wang Kang, Beihang University, Beijing, China

SAPREDICTOR: A SIMPLE AND ACCURATE SELF-ADAPTIVE PREDICTOR FOR HIERARCHICAL HYBRID MEMORY SYSTEM

Yujuan Tan, Wei Chen, Zhulin Ma, Dan Xiao, Duo Liu, Xianzhang Chen, Chongqing University, Chongqing, China; Zhichao Yan, Hewlett Packard Enterprise, Morrisville, NC

REPEAL MURPHY'S LAW: AVOID ERRORS

Time: 3:30 PM – 5:30 PM
Room: 3007, Level 3
Event Type: Research Manuscript
Topics Area(s): Manufacturing Test and Reliability, EDA

Chair/Co-Chair: TBA

Robust designs are always desired. This session helps push state of the art in this area by introducing fault-tolerant designs with Winograd convolution and SEU-tolerant latches, pioneering the deployment of defect tolerance and defect-aware synthesis to improve yield, developing aging and variation-aware dynamic timing analyzer and an application-based dynamic-voltage-accuracy-frequency-scaling (DVAFS) design flow, and enabling resilient analog in-memory deep learning via data layout re-organization.

AVATAR: AN AGING- AND VARIATION-AWARE DYNAMIC TIMING ANALYZER FOR APPLICATION-BASED DVAFS

Zuodong Zhang, Zizheng Guo, Yibo Lin, Runsheng Wang, Ru Huang, Peking University, Beijing, China

A DEFECT TOLERANCE FRAMEWORK FOR IMPROVING YIELD

Shiva Shankar Thiagarajan, Yiorgos Makris, The University of Texas at Dallas, TX; Suriya Natarajan, Intel Corporation, San Jose, CA

WINOGRAD CONVOLUTION: A PERSPECTIVE FROM FAULT TOLERANCE

Xinghua Xue, Lei Zhang, Chinese Academy of Sciences, Beijing, China; Haitong Huang, University of Chinese Academy of Science, Beijing, China; Cheng Liu, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Ying Wang, State Key Laboratory of Computer Architecture, Beijing, China; Tao Luo, Agency for Science Technology and Research, Singapore, Singapore, Singapore

TOWARDS RESILIENT ANALOG IN-MEMORY DEEP LEARNING VIA DATA LAYOUT RE-ORGANIZATION

Muhammad Rashedul Haq Rashed, Rickard Ewetz, University of Central Florida, Orlando, FL; Amro Awad, North Carolina State University, Raleigh, NC; Sumit Kumar Jha, The University of Texas at San Antonio, TX

SEM-LATCH: A LOST-COST AND HIGH-PERFORMANCE LATCH DESIGN FOR MITIGATING SOFT ERRORS IN NANOSCALE CMOS PROCESS

Zhong-Li Tang, Chia-Wei Liang, Ming-Hsien Hsiao, Hung-Pin (Charles) Wen, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

THINKING FAST AND ACTING SMART: ACCELERATED AND INTELLIGENT IOT

Time: 3:30 PM – 5:30 PM
Room: 3000, Level 3
Event Type: Research Manuscript
Topics Area(s): Design of Cyber-physical Systems, Cloud Computing and IoT, Cloud, Design

Chair/Co-Chair: Arne Hamann, Robert Bosch GmbH; Ganapati Bhat, Washington State University

BLUESEER: AI-DRIVEN ENVIRONMENT DETECTION VIA BLE SCANS

Valentin Poirot, Oliver Harms, Hendric Martens, Olaf Lansiedel, Kiel University, Kiel, Germany

COMPRESSIVE SENSING BASED ASYMMETRIC SEMANTIC IMAGE COMPRESSION FOR RESOURCE-CONSTRAINED IOT SYSTEM

Yujun Huang, Jianghui Zhang, Han Qiu, Shutao Xia, Tsinghua University, Shenzhen, China; Bin Chen, Harbin Institute of Technology, Shenzhen, Shenzhen, China

R2B: HIGH-EFFICIENCY AND FAIR I/O ALLOCATION FOR MULTI-TENANT WITH DIFFERENTIATED DEMANDS

Diansen Sun, Yunpeng Chai, Chaoyang Liu, Weihao Sun, Renmin University of China, Beijing, China; Qingpeng Zhang, City University of Hong Kong, Hong Kong, China

FAST AND SCALABLE HUMAN POSE ESTIMATION USING MMWAVE POINT CLOUD

Sizhe An, Umit Ogras, University of Wisconsin, Madison, WI

VWR2A: A VERY-WIDE-REGISTER RECONFIGURABLE-ARRAY ARCHITECTURE FOR LOW POWER EMBEDDED DEVICES

Benoît Denkinger, Miguel Peón Quirós, David Atienza, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland; Mario Konijnenburg, imec, Eindhoven, Netherlands; Francky Catthoor, imec, Leuven, Belgium

ALLEVIATING DATAPATH CONFLICTS AND DESIGN CENTRALIZATION IN GRAPH ANALYTICS ACCELERATION

Haiyang Lin, Mingyu Yan, Duo Wang, Mo Zou, Xiaochun Ye, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Fengbin Tu, Yizhou Sun, Jason Cong, University of California, Los Angeles, CA

NEW PERSPECTIVES IN HIGH-LEVEL SYNTHESIS

Time: 3:30 PM – 5:30 PM
Room: 3003, Level 3
Event Type: Special Session (Research)
Topics Area(s): EDA

Organizer: Antonino Tumeo, Pacific Northwest National Laboratory, Richland, WA

The ever-increasing complexities in semiconductor manufacturing are driving a renewed interests in techniques and approaches to generate hardware implementation quickly and effectively starting from high-level algorithmic specifications. High-Level Synthesis (HLS) has been subject of research for several decades, leading to numerous tools able to convert specifications written in general purpose languages (typically C or C++, with progressively more coverage of the syntaxes) to implementations in hardware description languages, used for both field programmable gate arrays (FPGAs) and Application-Specific Integrated Circuit (ASIC). However, new requirements and challenges brought by new technology nodes are leading HLS to explore new applications and creating new opportunities. These include ability to synthesize starting from higher level, high productivity programming frameworks (for data science and machine learning), their integration in agile hardware design flows, complex parallel accelerator architectures, integration of novel methods (including artificial intelligence and surrogate models) and dimensions for design space exploration (real time and security guarantees), and even new applications (e.g., HLS to enable functional verification of complex ASICs). This special session investigates all these new perspectives for HLS with four talks for leading experts of the area.

DEMOCRATIZING CUSTOMIZED COMPUTING WITH AUTOMATED ACCELERATOR SYNTHESIS

Atefeh Sohrabizadeh, Yunsheng Bai, Yizhou Sun, Jason Cong, University of California, Los Angeles, CA

ACCELERATOR DESIGN WITH DECOUPLED HARDWARE CUSTOMIZATIONS: BENEFITS AND CHALLENGES

Debjit Pal, Shaojie Xiang, Zhiru Zhang, Cornell University, Ithaca, NY; Yi-Hsiang Lai, Amazon Web Services, Santa Clara, CA; Zhenkun Yang, Pasquale Cocchini, Jin Yang, Intel Corporation, Hillsboro, OR; Louis-Noël Pouchet, Colorado State University, Fort Collins, CO

SCALEHLS: A SCALABLE HIGH-LEVEL SYNTHESIS FRAMEWORK ON MLIR

Hanchen Ye, Hyunmin Jeong, Gregory Jun, Deming Chen, University of Illinois at Urbana-Champaign, Urbana, IL; Stephen Neuendorffer, Xilinx, San Jose, CA

THE SODA APPROACH: LEVERAGING HIGH-LEVEL SYNTHESIS FOR HARDWARE/SOFTWARE CODESIGN AND HARDWARE SPECIALIZATION

Nicolas Bohm Agostini, Northeastern University, Boston, MA; Serena Curzel, Fabrizio Ferrandi, Politecnico di Milano, Milan, Italy; Ismet Dagli, Colorado School of Mines, Golden, CO; Ankur Limaye, University of Arizona, Tucson, AZ; Cheng Tan, Vinay Amatya, Marco Minutoli, Vito Giovanni Castellana, Joseph Manzano, Antonino Tumeo, Pacific Northwest National Laboratory, Richland, WA

WEDNESDAY GLADIATOR POSTER BATTLE

Time: 4:30 PM – 5:30 PM
Room: DAC Pavilion, Level 2

This is the last day to see the Gladiators in battle. Poster Gladiator finalist present their posters in the last speed round and the 2022 Poster Gladiator will be selected at today's final session. Poster Gladiators are chosen from all Engineering Track sessions including front-end, back-end, IP, embedded and cloud. Attendees and judges vote for the best Poster Gladiator! Come to the Pavilion and cast your vote.

A SCALABLE FRAMEWORK TO VALIDATE INTERCONNECT-BASED FIREWALLS TO ENHANCE SOC SECURITY COVERAGE

Ashutosh Mishra, Intel Technology India Pvt. Ltd, Bengaluru, India

TOWARDS AN AUTOMATED WORKFLOW FOR LINK-LEVEL EXPLORATION AND OPTIMIZATION IN THE DOMAIN OF ALL-TO-ALL OPTICAL NETWORKS

Luca Ramini, Hewlett Packard Enterprise, Milpitas, CA; Ahsan Alam, Ansys, Vancouver, Canada

DYNAMIC CDC VERIFICATION WITH ENHANCED JITTER MODELING IN SYNCHRONIZERS

Youngchan Lee, Samsung Electronics, Hwaseong-si, South Korea; Vikas Sachdeva, Real Intent Inc, Bengaluru, India

PRE AND POST SILICON ANALYSIS IN THE DESIGN AND VALIDATION OF AI ENABLED HIGH PERFORMANCE MICROPROCESSORS

Nagu Dhanwada, IBM, Poughkeepsie, NY; Karthik Swaminathan, IBM Research, Yorktown Heights, NY; Kartik Acharya, IBM, Atlanta, GA; Khajista Fattu, Anurag Umbarkar,IBM, Austin, TX; Ramon Bertran, IBM Research, New York City, NY

BILLION INSTANCE TIMING SIGN-OFF

Tim Helvey, Marvell, Rochester, MN; David Lawson, Marvell, Orange County, CA

WEDNESDAY ENGINEERING TRACKS POSTER RECEPTION

Time: 5:00 PM – 6:00 PM
Room: Level 2 Exhibit Hall

AI ASSISTED SMART ANALYSIS (AISA) FOR SYSTEM LEVEL ISSUE LOCALIZATION IN POST SILICON VALIDATION

Amaresh Chellapilla, Pandithurai Sangaiyah, Intel Technology India Pvt. Ltd, Bengaluru, India; Nagi Reddy Emani, Intel Technology India Pvt. Ltd, Andhra Pradesh, India

AI-BASED NEURAL NETWORK APPROACH FOR PERFORMANCE ESTIMATION OF COMPLEX SYSTEM-ON-CHIP

Manoj Munigala, Surinder Sood, Madhusudhan N, Intel Technology India Pvt. Ltd, Bengaluru, India

AUTOMATED TIMING DEGRADATION RECOVERY IN INCREMENTAL TAPE-OUT OF HIGH-SPEED CPU DESIGN

Gopalakrishnan Sadagopan, Senthil Ravi, Intel Technology India Pvt. Ltd, Bengaluru, India

CHATBOT AS A VIRTUAL ASSISTANT TO RETRIEVE INFORMATION FROM DATASHEETS

khaled Salah, Siemens EDA, Fremont, CA; Esraa Mohsen, Anss Khaled, Abdelrhman Tarek, Menna Hussien, Haidy Samir, Ain Shams University, Cairo, Egypt

CLOCK SCRIPTING FOR RELIABLE DESIGN FLOW

Gary Ellis, Marvell, Norman, OK

CONVERGING THE "WORLD'S DENSESTÂ" PNR DESIGN ON TSMC N5P - BEATING CUSTOM SRAM TRANSISTOR DENSITIES IN SYNTHESIZED PLACE & ROUTED DESIGN

Bhuoender Kumar, Guneet Singh, Goutami Aenuganti, Intel Corporation, Bengaluru, India; Raghav Gupta, Intel Corporation, Portland, OR

DESIGN INTENT DRIVEN ANALOG ROUTING METHODOLOGY

Rajeev Singh, Devendra Gupta, STMicroelectronics Pvt. Ltd., Delhi, India; Atul Bhargava, STMicroelectronics, New Delhi, India; Gautam Kumar, Cadence Design Systems, Inc., Delhi, India; Alexandre Soyer, Cadence Design Systems, Inc., Nice, France; Vishesh Kumar, Cadence Design Systems, Inc., Bengaluru, India

DIAGNOSIS OF FAULTS BY FAULT SIMULATION ON PCIE

Priyanka Gharat, Shikhadevi Katharia, Silicon Interfaces, Mumbai, India; Sushant Gawade, Silicon Interfaces, Thane, India

EFFICIENT STIMULUS GENERATION TECHNIQUES FOR A UVM TB

Pavan Yeluri, Intel Corporation, Hyderabad, India

FORMAL BASED AUTOMATION FRAMEWORK TO VERIFY COHERENT CONNECTIVITY OF MULTI-INSTANCE IPS

Somesh Gode, Texas Instruments, Bengaluru, India

FPOPT: ML-BASED CHIP FLOORPLAN OPTIMIZATION

Jaemin Seo, Yun Heo, Kunhyuk Kang, Seonil Brian Choi, Samsung Electronics, Hwaseong, South Korea; Joe R Walston, Synopsys, Durham, NC; Varun Gunnala, Synopsys, Hyderabad, India; Donghyun Lee, Synopsys, San Francisco, CA

HISTORY BASED PHYSICAL SYNTHESIS

Lakshmi Reddy, IBM Research, Yorktown Heights, NY; Cindy Washburn, IBM Systems, Poughquag, NY; Nancy Zhou, IBM, Austin, TX; Alex Suess, IBM Systems, Hopewell Junction, NY; Ben Trombley, IBM Systems, Pleasant Valley, NY; Dan Lewis, IBM Systems, Burlington, Canada; Josiah Hamilton, IBM Systems, Poughkeepsie, NY

IS FRONT-END ANALOG DESIGN AUTOMATION AN NP-TYPE OR SIMPLY A P-TYPE PROBLEM ?

Ramy Iskander, Intento Design, Paris, France

FSDB BASED SELF-GATING TECHNIQUE FOR POWER SAVING AND FEV VERIFICATION APPROACHES

Aman Jain, Sidarth Panda, Intel Technology India Pvt. Ltd, Bengaluru, India

HIGH SPEED, LOW POWER HYBRID ADC FOR DIRECT TO RF SAMPLING APPLICATIONS

Ken Potts, Alphacore Inc, Tempe, AZ

IMPROVING POWER GRID IR DROP WITH AN AUTOMATED LAYOUT ENHANCEMENT FLOW

Sumit Jha, Google, San Antonio, TX; Greg Davis, Siemens EDA, Wilsonville, OR; Fady Fouad, Siemens EDA, Cairo, Egypt; Gurpreet Lamba, Smitha Kamathi, Siemens EDA, Bengaluru, India; Jeffery Wilson, Siemens EDA, Canby, OR

THE INTRODUCTION AND BEST PRACTICES OF SEMICONDUCTOR CHIP DESIGN MODEL ON THE CLOUD

Taeil Kim, Naya Ha, Jongho Kim, Kyungtae Do, Sangyun Kim, Samsung Electronics, Hwaseong, South Korea

MERGING FORMAL AND SIMULATION VERIFICATION METRICS FOR COVERAGE CLOSURE

Pradeep Valipe, Xilinx, Hyderabad, India

MINIMIZE POWER CONSUMPTION WITH A NOVEL POWER ECO FLOW

Jianfeng Liu, Eunju Hwang, YeongYeong Shin, Seokhoon Kim, Jun Seomun, Sangyun Kim, Samsung Electronics, Hwaseong, South Korea

MITIGATION OF SOFT-ERRORS IN STORAGE ELEMENTS THROUGH LAYOUT AND CIRCUIT DESIGN TECHNIQUES

Sumit Wadkar, Parag Upadhyay, Intel Corporation, Bengaluru, India; Shrisagar Dwivedi, Intel Corporation, Sunnyvale, CA;

A NOVEL DUTY-CYCLE ADJUSTER CIRCUIT, TO BE USED AS PART OF AUTOMATIC CLOCK DUTY-CYCLE CORRECTOR CIRCUIT

Ayan Dutta, OpenFive, Bengaluru, India

ON-CHIP EMBEDDED SENSOR IN 18NM TECHNOLOGY TO MONITOR THE EFFECTS OF PROCESS VARIATIONS ON STANDARD CELLS LOGIC AND INTERCONNECT DELAYS

Rohit Goel, STMicroelectronics, Noida, India

OPTIMAL AND EFFICIENT POWER AWARE VERIFICATION FRAMEWORK FOR LOW POWER MIXED-SIGNAL SOC

Sooraj Sekhar, Harsh Sharma, Siddharth Sarin, Pavan Kumar Kulkarni, Ruchi Shankar, Harish Maruthiyodan, Shalini Eswaran, Gaurav Varshney, Lakshmanan Balasubramanian, Texas Instruments (India) Pvt. Ltd., Bengaluru, India; Akshay Revankar, Carnegie Mellon University, Pittsburgh, PA

PATH-FINDING THROUGH VARIABILITY-AWARE DTCO-FLOW

Markus Karner, Gerhard Rzepa, Oskar Baumgartner, Zlatan Stanojevic, Global TCAD Solutions, Wien, Austria

PERFORMANCE OPTIMIZATION OF EMBEDDED FPGA

Michael Ji, Flex-Logix Technologies, Mountain View, CA

PORTING SOFTWARE TO HARDWARE USING XLS/DSLX

Johan Euphrosine, Google, Tokyo, Japan

PRE-SILICON DESIGN QUALITY AND TEST READINESS THROUGH EFFICIENT VERIFICATION METHODOLOGY

Harsh Sharma, Sagar Jogur, Sooraj Sekhar, Harish Maruthiyodan, Lakshmanan Balasubramanian, Texas Instruments (India) Pvt. Ltd., Bengaluru, India; Narava Kumar, Texas Instruments (India) Pvt. Ltd., Andhra Pradesh, India; Kavya S, Karmic Design Private Limited, Karnataka, India; Avinash Chaudhary, Ruchi Shankar, Texas Instruments (India) Pvt. Ltd., West Delhi, India; Einar Ellingsen, Stefan Dannenberger, Texas Instruments, Oslo, Norway; Mikael Kromer, Texas Instruments, McKinney, TX; Anand G, Texas Instruments (India) Pvt. Ltd., Maharashtra, India

PROCESS MONITORING BLOCKS - FOR MONITORING ANALOG PERFORMANCE

Priya Talwar, Anand Mishra, STMicroelectronics, Noida, India

SCIENCE WITHOUT BOUNDARIES: A PROVEN METHOD TO ACHIEVE SEAMLESS DESIGN COLLABORATION BETWEEN CROSS-INSTITUTIONAL PROJECT TEAMS

Carl Grace, Lawrence Berkeley National Lab, San Francisco, CA; Simon Rance, Cliosoft, Fremont, CA

SHIFT LEFT PERFORMANCE VERIFICATION USING FORMAL METHODS FOR ML ASICS

Puneet Anand, Facebook, Richmond Hill, Canada

STREAMLINED SOLUTION FOR CAD VIEWS GENERATION & VALIDATION OF AMS IP FOR SOC ENABLEMENT

Lippika Parwani, Bhupendra Singh, Gaurav Goel, STMicroelectronics, Noida, India; Frederic Esteban, STMicroelectronics, Grenoble, France

TECHNOLOGY CO-OPTIMIZATION TO MITIGATE THE TECHNOLOGY IMPACT OF CONTEXT-BASED TIMING IN STANDARD CELL LIBRARY

Veny Mahajan, Anand Mishra, STMicroelectronics, Noida, India

PHYSICALLY UNCLONABLE FUNCTION COMPLIANT WITH ISO/IEC 20897-1:2020

Sylvain Guilley, Guillaume Patrigeon, Secure-IC

LATE BREAKING RESULTS POSTERS

Time: 6:00 PM – 7:00 PM
Room: Level 2 Exhibit Hall

EFFICIENT TIMING PROPAGATION WITH SIMULTANEOUS STRUCTURAL AND PIPELINE PARALLELISMS

Cheng-Hsiang Chiu, Tsung-Wei Huang, University of Utah, Salt Lake City, UT

A FAST AND LOW-COST COMPARISON-FREE SORTING ENGINE WITH UNARY COMPUTING

Amir Hossein Jalilvand, Samaneh Naderi, Iran University of Science and Technology, Tehran, Iran; Seyedeh Newsha Estiri, M. Hassan Najafi, University of Louisiana at Lafayette, Lafayette, LA; Mohsen Imani, University of California Irvine, CA

FLEXIBLE CHIP PLACEMENT VIA REINFORCEMENT LEARNING

Fu-Chieh Chang, Yu-Wei Tseng, MediaTek, Taipei, Taiwan; Ya-Wen Yu, Ssu-Rui Lee, I-Lun Tseng, MediaTek, Hsinchu, Taiwan; Alexandra Cioba, MediaTek, Cambridge, United Kingdom; Da-shan Shiu, MediaTek, Taipei, Taiwan; Jhih-Wei Hsu, Cheng-Yuan Wang, Ren-Chu Wang, National Taiwan University, Taipei, Taiwan; Yao-Wen Chang, National Taiwan University, Taipei, Taiwan; Chien-Yi Yang, Maxeda Technology Inc., Taipei, Taiwan; Tai-Chen Chen, Tung-Chieh Chen, Maxeda Technology Inc., Hsinchu, Taiwan

FPGA-AWARE AUTOMATIC ACCELERATION FRAMEWORK FOR VISION TRANSFORMER WITH MIXED-SCHEME QUANTIZATION

Mengshu Sun, Zhengang Li, Geng Yuan, Yanyu Li, Miriam Leeser, Xue Lin, Northeastern University, Boston, MA; Yanyue Xie, Northeastern University, Boston, MA; Alec Lu, Zhenman Fang, Simon Fraser University, Burnaby, Canada; Haoyu Ma, University of California, Irvine, CA; Hao Tang, ETH Zürich, Switzerland; Zhangyang Wang, The University of Texas at Austin, TX

HARDWARE-EFFICIENT STOCHASTIC ROUNDING UNIT DESIGN FOR DNN TRAINING

Sung-En Chang, Geng Yuan, Mengshu Sun, Yanyu Li, Xiaolong Ma, Zhengang Li, Yanyue Xie, Xue Lin, Yanzhi Wang, Northeastern University, Boston, MA; Alec Lu, Zhenman Fang, Simon Fraser University, Burnaby, Canada; Minghai Qin, Milpitas, MA

PLACEMENT INITIALIZATION VIA A PROJECTED EIGENVECTOR ALGORITHM

Pengwen Chen, National Chung Hsing University, Taichung, Taiwan; Chung-Kuan Cheng, Albert Chern, Chester Holtz, Aoxi LI, Yucheng Wang, University of California San Diego, CA

SUBGRAPH MATCHING BASED REFERENCE PLACEMENT FOR PCB DESIGNS

Miaodi Su, Shu Zhang, Haiyuan Su, Fuzhou University, Fuzhou, China; Yifeng Xiao, University of Southern California, Los Angeles, CA; Jiacen Xu, Huan He, Huawei, Hangzhou, China; Ziran Zhu, Southeast University, Nanjing, China; Jianli Chen, Fudan University, Shanghai, China; Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

THERMAL-AWARE DRONE BATTERY MANAGEMENT

Hojun Choi, Youngmoon Lee, Hanyang University, Ansan, South Korea

WAVEFORM-BASED PERFORMANCE ANALYSIS OF RISC-V PROCESSORS

Lucas Klemmer, Daniel Grosse, Johannes Kepler University Linz, Linz, Austria

WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 PM – 7:00 PM
Room: Level 2 Lobby

AGGRESSIVE PERFORMANCE IMPROVEMENT ON PIM DEVICES BY ADOPTING HUGEPAGES

Paulo Cesar Santos, Bruno Endres Forlin, Augusto Exenberger Becker, Luigi Carro, Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil; Marco Antonio Zanata Alves, UFPR, Curitiba, Brazil

AGILE: A COLLABORATIVE AIR-GROUND IOT EDGE FRAMEWORK FOR SUSTAINABLE REMOTE MONITORING

Wen Zhang, Chen Pan, Wenlu Wang, Texas A&M University, Corpus Christi, TX; Mehdi Sookhak, Texas A&M University, Corpus Christi, Corpus Christi, TX; Yanzhi Wang, Northeastern University, Boston, MA; Mimi Xie, The University of Texas at San Antonio, TX

AGING-AWARE CRITICAL PATH SELECTION VIA GRAPH ATTENTIONAL NETWORKS

Yuyang Ye, Southeast University, Nanjing, China; Tinghuan Chen, Bei Yu, The Chinese University of Hong Kong, Hong Kong; Jingyu Yang, University of Birmingham, Shenzhen, China; Yifei Gao, Hao Yan, Longxing Shi, Southeast University, Nanjing, China

AGING-AWARE MEMRISTOR FOR RELIABLE AND ENERGY-EFFICIENT DEEP LEARNING ACCELERATION

Dharanidhar Dang, San Diego, AL; Aurosmita Khansama, Rabi N. Mahapatra, Texas A&M University, College Station, TX; Bill Lin, Debashis Sahoo, University of California, San Diego, CA

AMBIENT TEMPERATURE ESTIMATION USING NEURAL NETWORKS AND DEVICE CONTEXTUAL INFORMATION

Aditya Jhawar, Aditi Jaiswal, Nikhil Sahni, Vaisakh Chirayil S B, Renju Nair, Samsung Electronics, Bengaluru, India

AMBITION: AMBIENT TEMPERATURE AWARE VM ALLOCATION FOR ENERGY EFFICIENT EDGE DATA CENTERS

Seung Hun Choi, Young Geun Kim, Sung Woo Chung, Korea University, Seoul, South Korea; Seon Young Kim, Electronics and Telecommunications Research Institute, Daejeon, South Korea; Joonho Kong, Kyungpook National University, Daegu, South Korea

ATTACKING THE TIMINGCAMOUFLAGE+ ALGORITHM

Priya Mittu, Yuntao Liu, Abhishek Chakraborty, Ankur Srivastava, University of Maryland, College Park, College Park, MD

AUTOMATIC GENERATION OF CELL BASED STRUCTURED CIM MACROS

Christian Lanius, Jie Lou, Tobias Gemmeke, RWTH Aachen University, Aachen, Germany

AUTOMATION OF FUNCTIONAL SAFETY AND SECURITY METHODS FOR DESIGN AND VERIFICATION

Nikita Gulliya, Agnisys Inc., Noida, India; Freddy Nunez, Agnisys Inc., Los Angeles, CA; Neena Chandawale, Agnisys Inc., San Francisco, CA

AUTOPILOT: COMPUTE DESIGN AUTOMATION FOR AUTONOMOUS DRONES

Srivatsan Krishnan, Sabrina Neuman, Gu-Yeon Wei, David Brooks, Vijay Janapa Reddi, Harvard University, Cambridge, MA; Zishen Wan, Georgia Institute of Technology, Atlanta, GA; Kshitij Bhardwaj, LLNL, Livermore, CA; Paul Whatmough, Arm Ltd., Cambridge, CA; Aleksandra Faust, Google, Mountain View, CA

BOUNDED BAT: BOUNDED BACKUP TIME FOR INTERMITTENT POWER DEVICES

SatyaJaswanth Badri, Indian Institute of Technology, Ropar, Ropar, India; Mukesh Saini, Neeraj Goel, Indian Institute of Technology, Ropar, India

A BUILT-IN ADAPTIVE NDA FOR HIGH-LEVEL LANGUAGE ACCELERATION

Rafael de Moura, Joao Paulo Lima, Luigi Carro, Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil

CFU PLAYGROUND: FULL-STACK OPEN-SOURCE FRAMEWORK FOR TINY MACHINE LEARNING (TINYML) ACCELERATION ON FPGAS

Shvetank Prakash, Colby Banbury, Vijay Janapa Reddi, Harvard University, Cambridge, MA; Tim Callahan, Pete Warden, Google, Mountain View, CA; Tim Ansell, Google, Mountain View, CA; Joseph Bushagour, Purdue University, West Lafayette, IN; Alan Green, Google, Sydney, Australia

CONSTRUCTING LARGE BUFFERS WITH HETEROGENEOUSSTT-RAM CELLS FOR DNN ACCELERATORS

Yongjun Kim, Kwangeun Byun, Seokin Hong, Sungkyunkwan University, Suwon, South Korea

A COQ FRAMEWORK FOR MORE TRUSTWORTHY DRAM CONTROLLERS

Felipe Lisboa Malaquias, Florian Brandner, Lirida Naviner, Télécom Paris, Palaiseau, France; Mihail Asavoae, University of Paris, Saclay, Saclay, France

DEEP REINFORCEMENT LEARNING EMPOWERED CONTENT CACHING IN MOBILE SOCIAL NETWORKS

Keke Gai, Ziyue Hu, Liehuang Zhu, Beijing Institute of Technology, Beijing, China; Meikang Qiu, Texas A&M University, College Station, TX

DESIGN SPACE EXPLORATION OF STREAMING IMPLEMENTATIONS OF CNNS ON THE XILINX AIENGINE PROCESSOR ARRAY

Louis Coulon, Paolo Ienne, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland; Kristof Denolf, Jack Lo, Xilinx, Longmont, CO; Stephen Neuendorffer, Kees Vissers, Xilinx, San Jose, CA

A DOMAIN-SPECIFIC SYSTEM-ON-CHIP DESIGN FOR ENERGY EFFICIENT WEARABLE EDGE AI APPLICATIONS

Yigit Tuncel, Anish Krishnakumar, Aishwarya Chithra, Younghyun Kim, Umit Ogras, University of Wisconsin, Madison, WI

DVFS VIRTUALIZATION FOR ENERGY MINIMIZATION OF MIXED-CRITICALITY DUAL-OS PLATFORMS

Takumi Komori, Yutaka Masuda, Tohru Ishihara, Nagoya University, Nagoya, Japan

AN EFFICIENT ANALOG CONVOLUTIONAL NEURAL NETWORK HARDWARE ACCELERATOR ENABLED BY A NOVEL MEMORYLESS ARCHITECTURE FOR INSECT-SIZED ROBOTS

Iman Dadras, Saoni Banerji, Alvo Aabloo, University of Tartu, Estonia; Mohammad Hasani Ahmadilivani, Jaan Raik, Tallinn University of Technology, Tallinn, Estonia

EFFICIENT SCHEDULING OF SYNCHRONOUS DATAFLOW GRAPHS ON COMMUNICATION COST-AWARE HETEROGENEOUS PLATFORMS

Pengfei Sun, Xue-Yang Zhu, Chinese Academy of Sciences, Beijing, China

AN ENERGY-EFFICIENT MULTI-BITWIDTH SYSTOLIC RERAM ACCELERATOR FOR NAS OPTIMIZED CNN NETWORKS

Dingbang Liu, Haoxiang Zhou, Jun Liu, Changhai Man, Mingqiang Huang, Wei Mao, Shaobo Luo, Quan Chen, Hao Yu, Southern University of Science and Technology, Shenzhen, China; Mingsong Lv, The Hong Kong Polytechnic University, Hong Kong

EQUIVALENCE CHECKING FOR AGILE HARDWARE DESIGN

Yanzhao Wang, Fei Xie, Portland State University, Portland, OR; Zhenkun Yang, Pasquale Cocchini, Jin Yang, Intel Corporation, Hillsboro, OR

ERROR DISTRIBUTION MODELING FOR BEHAVIOR-LEVEL APPROXIMATE COMPUTING

Lakshmi Sathidevi, Cong Hao, Georgia Institute of Technology, Atlanta, GA; Abhinav Sharma, Indian Institute of Information Technology, Guwahati, India; Nan Wu, University of California, Santa Barbara, CA; Xun Jiao, Villanova University, Villanova, PA

FPGNN-ATPG: AN EFFICIENT FAULT PARALLEL AUTOMATIC TEST PATTERN GENERATOR

Yuyang Ye, Zonghui Wang, Luoyu Mei, Ziqi Wang, Hao Yan, Longxing Shi, Southeast University, Nanjing, China

HYBRID GRAPH MODELS FOR LOGIC OPTIMIZATION VIA SPATIO-TEMPORAL INFORMATION

Nan Wu, Yuan Xie, University of California, Santa Barbara, CA; You-Young Lee, Cong Hao, Georgia Institute of Technology, Atlanta, GA

IMPROVING GPU PERFORMANCE VIA COORDINATED KERNEL SLICING AND MULTI CUDA STREAMING

Zhuo Tang, Bingting Jiang, Yunchun Liu, Changsha, China; Kenli Li, Hunan University, Changsha, China; Yaohua Wang, National University of Defense Technology, Changsha, China

INSTANT DATA SANITIZATION ON MULTI-LEVEL-CELL NAND FLASH MEMORY

Md Raquibuzzaman, Matchima Buddhanoy, Aleksandar Milenkovic, Biswajit Ray, University of Alabama, Huntsville, AL

INSTRUCTION-AWARE LEARNING-BASED TIMING ERROR MODELS THROUGH SIGNIFICANCE-DRIVEN APPROXIMATIONS

Styliani Tompazi, Ioannis Tsiokanos, Jesus Martinez del Rincon, Lev Mukhanov, Georgios Karakonstantis, Queen's University Belfast, United Kingdom

LDAVPM: A LATCH DESIGN WITH ALGORITHM-BASED VERIFICATION PROTECTED AGAINST MULTIPLE-NODE-UPSETS IN HARSH RADIATION ENVIRONMENTS

Aibin Yan, Zhixing Li, Qi Wang Jie Cui, Anhui University, Hefei, China; Tianming Ni, Anhui Polytechnic University, Wuhu, China; Zhengfeng Huang, Hefei University of Technology, Hefei, China; Xiaoqing Wen, Kyushu Institute of Technology, Fukuoka, Japan; Patrick Girard, CNRS, LIRMM, University of Montpellier, Montpellier, France

LEVERAGING LAYOUT-BASED EFFECTS FOR LOCKING ANALOG ICS

Muayad Aljafar, Samuel Pagliarini, Tallinn Technology University, Tallinn, Estonia; Florence Azaïs, Marie-Lise Flottes, CNRS, LIRMM, University of Montpellier, France

A METHOD FOR HIERARCHICAL, TRANSISTOR-LEVEL CIRCUIT SIMULATION

Henry Cao, ICEE Solutions LLC, Cupertino, CA

ML-ASSISTED VMIN BINNING WITH MULTIPLE GUARD BANDS FOR LOW POWER CONSUMPTION

Wei-Chen Lin, Chun Chen, Chao-Ho Hsieh, Cheng-Yun Hsieh, James Li, National Taiwan University, Taipei City, Taiwan; Eric Fang, Sung Hsueh, MediaTek Inc., Hsinchu City, Taiwan

A MODEL-BASED EVALUATION FRAMEWORK FOR BATTERY CELL BALANCING TECHNIQUES

Seongik Jang, Ajou University, Suwon, South Korea; Hoeseok Yang, Santa Clara University, Suwon, South Korea

MODULAR SOFTWARE FOR REAL-TIME QUANTUM CONTROL SYSTEMS

Leon Riesebos, Brad Bondurant, Jacob Whitlow, Mark Kuzyk, Tianyi Chen, Samuel Phiri, Jungsang Kim, Kenneth Brown, Duke University, Durham, NC; Junki Kim, Sungkyunkwan University, Suwon, South Korea

ON-DEMAND REDUNDANCY GROUPING: SELECTABLE SOFT-ERROR TOLERANCE FOR A MULTICORE CLUSTER

Michael Rogenmoser, Nils Wistoff, Pirmin Vogel, Frank Gurkaynak, ETH Zürich, Zurich, Switzerland; Luca Benini, University of Bologna, Bologna, Italy

A PAGE-MAPPING CONSISTENCY PROTECTING METHOD FOR SOFT ERROR DAMAGE IN FLASH-BASED STORAGE

Jung-Hoon Kim, Young-Sik Lee, Samsung Electronics, Hwaseong, South Korea

PARTITIONPIM: PRACTICAL MEMRISTIVE PARTITIONS FOR FAST PROCESSING-IN-MEMORY

Orian Leitersdorf, Ronny Ronen, Shahar Kvatinsky, Technion - Israel Institute of Technology, Haifa, Israel

PERFORMANCE IMPACT OF INTER-PIM COMMUNICATION

Bruno Endres Forlin, Paulo Cesar Santos, Augusto Exenberger Becker Luigi Carro, Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil; Marco Antonio Zanata Alves, UFPR, Curitiba, Brazil

POWERING MULTI-TASK FEDERATED LEARNING WITH COMPETITIVE GPU RESOURCE SHARING

Yongbo Yu, Fuxun Yu, Zirui Xu, Xiang Chen, George Mason University, Fairfax, VA; Di Wang, Minjia Zhang, Microsoft, Redmond, WA; Ang Li, Duke University, Durham, NC; Shawn Bray, Chenchen Liu, University of Maryland, Baltimore, MD

PRIME: A PROCESSING IN MEMORY HARDWAREEMULATION FRAMEWORK

Andrew Dervay, Binghamton University, Binghamton, AL; Wenfeng Zhao, Binghamton University, Vestal, NY

QUALIFICATION OF METAMORPHIC RELATIONS FOR SYSTEM LEVEL AMS MODELS USING DATA FLOW COVERAGE

Muhammad Hassan, Cyber Physical Systems, Bremen, Germany; Rolf Drechsler, University of Bremen/DFKI, Bremen, Germany

REAL-TIME, PERSONALIZED PREDICTION OF SEPSIS ONSET USING FUSION OF ELECTRONIC MEDICAL RECORDS AND IN-SENSOR ANALOG CLASSIFIER

Sudarsan Sadasivuni, University of Buffalo, Buffalo, NY; Monjoy Saha, National Institutes of Health, Bethesda, MD; Sumukh Prashant Bhanushali, Arindam Sanyal, Arizona State University, Tempe, AZ; Imon Banerjee, Mayo Clinic, Tempe, AZ

A RISC-V POWER CONTROLLER FOR HPC PROCESSORS WITH PARALLEL CONTROL-LAW COMPUTATION ACCELERATION

Alessandro Ottaviano, Robert Balas, ETH Zürich, Zurich, Switzerland; Giovanni Bambini, Corrado Bonfanti, Antonio Mastrandrea, Luca Benini, Simone Benatti, Davide Rossi, Andrea Bartolini, University of Bologna, Italy

RISCYROP: AUTOMATED RETURN-ORIENTED PROGRAMMING ATTACKS ON RISC-V AND ARM64

Tobias Cloosters, Oussama Draissi, David Paassen, Lucas Davi, University of Duisburg-Essen, Germany; Patrick Jauernig, Emmanuel Stapf, Jianqiang Wang, Ahmad-Reza Sadeghi, Technische Universität Darmstadt, Germany

SALSA: SIMULATED ANNEALING BASED LOOP-ORDERING SCHEDULER FOR DNN ACCELERATORS

Victor Jung, Arne Symons, Linyan Mei, Marian Verhelst, KU Leuven, Heverlee, Belgium

SELF-ORGANIZING AND PARALLEL-PROCESS DRIVEN FAST GENERATION OF ADVERSARIAL EXAMPLES FOR 3D POINT CLOUDS

Wei Jiang, Chen Bian, Jinyu Zhan, Zhenyu Liu, Hong Lei, Ziwei Song, Xiangyu Wen, University of Electronic Science and Technology of China, Chengdu, China

SOC PLATFORM FOR HETEROGENEOUS MULTIPLE IP CORE EVALUATION

Atsushi Hasegawa, Tadahiko Shimazu, The University of Tokyo, Bunkyo-ku, Japan; Makoto Ikeda, The University of Tokyo, Bunkyo-ku, Japan; Ichiro Naka, Shinichi Ouchi, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan

SOFT TILES: CAPTURING PHYSICAL IMPLEMENTATION FLEXIBILITY FOR TIGHTLY-COUPLED PARALLEL PROCESSING CLUSTERS

Gianna Paulin, Matheus Cavalcante, Paul Scheffler, Luca Bertaccini, Yichao Zhang, Frank Gurkaynak, ETH Zürich, Switzerland; Luca Benini, University of Bologna, Bologna, Italy

SYSTEM-LEVEL DESIGN AND TARGET AGNOSTIC HIGH-LEVEL OPTIMIZATIONS FOR HLS

Nicolas Bohm Agostini, David Kaeli, Northeastern University, Boston, MA; Serena Curzel, Politecnico di Milano, Milan, Italy; Vinay Amatya, Marco Minutoli, Cheng Tan, Vito Giovanni Castellana, Joseph Manzano, Antonino Tumeo, Pacific Northwest National Laboratory, Richland, WA

THERMAL AND SIGNALING CONSIDERATIONS FOR 2.5D INTEGRATION OF ARM-BASED 7NM HIGH-PERFORMANCE SYSTEMS

Ankit Kaul, Lingjun Zhu, Georgia Institute of Technology, Atlanta, GA; Muhannad Bakir, Georgia Institute of Technology, Atlanta, GA; Rahul Mathur, Jim Dodrill, Arm Ltd., Austin, TX

TOO BIG TO FAIL? ACTIVE FEW-SHOT LEARNING GUIDED LOGIC SYNTHESIS

Animesh Basak Chowdhury, Ramesh Karri, Siddharth Garg, New York University, Brooklyn, NY; Benjamin Tan, University of Calgary, Calgary, Canada

TRANSFORMED DATA AND FASTER-SPDZ : TECHNIQUES FOR PRIVACY-PRESERVING DEEP LEARNING IN REAL-WORLD APPLICATIONS

Shubham Jain, Aditya JhawarSharmila Mani, Nikhil Sahni, Samsung Electronics, Bengaluru, India

A UNIFIED CRYPTOPROCESSOR FOR LATTICE-BASED SIGNATURE AND KEY-EXCHANGE

Aikata Aikata, Ahmet Can Mert, David Jacquemin, Sujoy Sinha Roy, Graz University of Technology, Graz, Austria; Amitabh Das, Donald Matthews, AMD, Austin, TX; Santosh Ghosh, Intel Corporation, Hillsboro, OR

VECTOR IN MEMORY ARCHITECTURE FOR SIMPLE AND HIGH EFFICIENCY COMPUTING

Marco Antonio Zanata Alves, Aline Cordeiro, Francis Moreira, UFPR, Curitiba, Brazil; Sairo Santos, Universidade Federal do Semi-árido, Curitiba, Brazil; Paulo Cesar Santos, Luigi Carro, Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil

WHAT HELPER DATA REALLY LEAKS: A PRACTICAL APPROACH TO ESTIMATE THE MIN-ENTROPY IN PUFS USING THEIR RESPONSE MASS FUNCTION

Christoph Frisch, Michael Pehl, Technische Universität München, Germany; Florian Wilde, Siemens EDA, Munich, Germany; Thomas Holzner, Lauterbach Engineering GmbH &Co. KG, Höhenkirchen-Siegertsbrunn, Germany

Thursday, July 14, 2022

DAC BEST PAPER/PRESENTATION AWARDS AND THURSDAY KEYNOTE

Time: 8:40 AM – 9:45 AM
Room: 3008-3012, Level 3
Event Type: Keynote

STRANGE LOOPS IN DESIGN AND TECHNOLOGY

Giovanni De Micheli, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland

Strong ties link the evolution of computing, semiconductor technology and design automation. The unprecedented growth of system solutions, services and markets are due to the cross-fertilization of various areas of science and technology, where often new problems motivate new solutions in a circular way. Design automation has led engineers in sailing through uncharted territories, in shaping our digital society on robust grounds and in providing us with a launchpad for the future.

CAN WE ACHIEVE A SECURE, ROBUST, AND ENERGY-EFFICIENT CLOUD-EDGE CONTINUUM?

Time: 10:30 AM – 12:00 PM
Room: 3000, Level 3
Event Type: Research Manuscript
Topics Area(s): Design of Cyber-physical Systems, Cloud Computing and IoT, Cloud, Design

Chair/Co-Chair: Pu Zhao, Northeastern University; Fanxin Kong, Syracuse University

This session presents techniques for secure, robust, and efficient design of cyber-physical and cloud systems. The papers in the session cover cross-layer topics spanning from sensors to data centers. Innovation techniques include real-time adaptive sensor attack detection in CPS, energy-efficient BNN-based perception, and correct-by-construction control learning with verification for CPS. Additionally, this session features a paper on hyperdimensional computing based hashing to improve the cloud efficiency and robustness.

HYPERDIMENSIONAL HASHING: A ROBUST AND EFFICIENT DYNAMIC HASH TABLE

Mike Heddes, Igor Nunes, Tony Givargis, Alexandru Nicolau, Alexander Veidenbaum, University of California, Irvine, CA

IN-SITU SELF-POWERED INTELLIGENT VISION SYSTEM WITH INFERENCE-ADAPTIVE ENERGY SCHEDULING FOR BNN-BASED ALWAYS-ON PERCEPTION

Maimaiti Nazhamaiti, Han Xu, Zheyu Liu, Fei Qiao, Qi Wei, Tsinghua University, Beijing, China; Haijin Su, Li Luo, Beijing Jiaotong University, Beijing, China; Zidong Du, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Xinghua Yang, Beijing Forestry University, Beijing, China

ADAPTIVE WINDOW-BASED SENSOR ATTACK DETECTION FOR CYBER-PHYSICAL SYSTEMS

Lin Zhang, Zifan Wang, Mengyu Liu, Fanxin Kong, Syracuse University, Syracuse, NY

DESIGN-WHILE-VERIFY: CORRECT-BY-CONSTRUCTION CONTROL LEARNING WITH VERIFICATION IN THE LOOP

Yixuan Wang, Zhaoran Wang, Zhilu Wang, Qi Zhu, Northwestern University, Evanston, IL; Chao Huang, University of Liverpool, United Kingdom

HIGHLY-OPTIMIZED YET FLEXIBLE NEUROMORPHIC PROCESSORS

Time: 10:30 AM – 12:00 PM
Room: 3005, Level 3
Event Type: Research Manuscript
Topics Area(s): AI/ML Design: Circuits and Architecture, Design

Chair/Co-Chair: Subhendu Roy, Cadence Design Systems, Inc.; TBA

The quest for ever increasing energy-efficiency and performance results in highly optimized multicore processors. However, the value added by aggressive optimizations can diminish unless these processors facilitate reuse and programmability. The state-of-the are papers in this session present novel approaches that consider these conflicting objectives.

GABAN: A GENERIC AND FLEXIBLY PROGRAMMABLE VECTOR NEURO-PROCESSOR ON FPGA

Jiajie Chen, Le Yang, Youhui Zhang, Tsinghua University, Beijing, China

ADEPT: AUTOMATIC DIFFERENTIABLE DESIGN OF PHOTONIC TENSOR CORES

Jiaqi Gu, Hanqing Zhu, Chenghao Feng, Zixuan Jiang, Mingjie Liu, Shuhan Zhang, Ray T. Chen, David Z. Pan, The University of Texas at Austin, TX

UNICORN: A MULTICORE NEUROMORPHIC PROCESSOR WITH FLEXIBLE FAN-IN AND UNCONSTRAINED FAN-OUT FOR NEURONS

Zhijie Yang, Lei Wang, Yao Wang, Linghui Peng, Xiaofan Chen, Xun Xiao, Yaohua Wang, Weixia Xu, National University of Defense Technology, Changsha, China

EFFECTIVE ZERO COMPRESSION ON RERAM-BASED SPARSE DNN ACCELERATORS

Hoon Shin, Rihae Park, Seung Yul Lee, Yeonhong Park, Hyunseung Lee, Jae W. Lee, Seoul National University, Seoul, South Korea

NOVEL APPROACHES FOR SCALING ROUTING AND DFM CHALLENGES

Time: 10:30 AM – 12:00 PM
Room: 3007, Level 3
Event Type: Research Manuscript
Topics Area(s): Physical Design and Verification, Lithography and DFM, EDA

Chair/Co-Chair: Atsushi Takahashi, Tokyo Institute of Technology; Chung-Kuan Cheng, University of California, San Diego

This session focuses on novel approaches for routing and lithography modeling. The first paper presents a new flip-chip router based on Y-architecture. The second paper introduces a federated learning based method for routability estimation. The third paper presents a GPU-accelerated framework equipped with spatial attention for inverse lithography technology, while the last paper introduces a fast neural network based method for lithography simulation.

Y-ARCHITECTURE-BASED FLIP-CHIP ROUTING WITH DYNAMIC PROGRAMMING-BASED BEND MINIMIZATION

Szu-Ru Nie, Yen-Ting Chen, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

TOWARDS COLLABORATIVE INTELLIGENCE: ROUTABILITY ESTIMATION BASED ON DECENTRALIZED PRIVATE DATA

Jingyu Pan, Chen-Chia Chang, Zhiyao Xie, Ang Li, Minxue Tang,; Tunhou Zhang, Yiran Chen, Duke University, Durham, NC; Jiang Hu, Texas A&M University, College Station, TX

A2-ILT: GPU ACCELERATED ILT WITH SPATIAL ATTENTION MECHANISM

Qijing Wang, Bentian Jiang, Martin Wong, Evangeline Young, The Chinese University of Hong Kong, Hong Kong

GENERIC LITHOGRAPHY MODELING WITH DUAL-BAND OPTICS-INFORMED NEURAL NETWORKS

Haoyu Yang, Mark Kilgard, Brucek Khailany, Haoxing Ren, NVIDIA, Austin, TX; Zongyi Li, NVIDIA, Pasadena, CA; Kumara Sastry, Saumyadip Mukhopadhyay, Vivek Singh, NVIDIA, Portland, OR; Anima Anandkumar, California Institute of Technology, Pasadena, CA

RESIST FAULTS AND MAKE MEMORIES SMARTER

Time: 10:30 AM – 12:00 PM
Room: 3002, Level 3
Event Type: Research Manuscript
Topics Area(s): In-memory and Near-memory Computing, Design

Chair/Co-Chair: Arman Roohi, University of Nebraska, Lincoln; Shaahin Angizi, New Jersey Institute of Technology

Resistive RAM based In-Memory Computing offers a promising path to break the von-Neumann bottleneck. This session pushes the frontiers in this novel computing paradigm by exploring algorithmic techniques to address fundamental challenges related to noise and fault tolerance. Application-hardware co-design demonstrates the potential of such In-Memory computing platforms for graph based vector search and string processing applications.

STATISTICAL COMPUTING FRAMEWORK AND DEMONSTRATION FOR IN-MEMORY COMPUTING SYSTEMS

Bonan Zhang, Peter Deaville, Naveen Verma, Princeton University, Princeton, NJ

WRITE OR NOT: PROGRAMMING SCHEME OPTIMIZATION FOR RRAM-BASED NEUROMORPHIC COMPUTING

Ziqi Meng, Yanan Sun, Weikang Qian, Shanghai Jiao Tong University, Shanghai, China

RESMA: ACCELERATING APPROXIMATE STRING MATCHING USING RERAM-BASED CONTENT ADDRESSABLE MEMORY

Huize Li, Hai Jin, Long Zheng, Yu Huang, Xiaofei Liao, Zhuohui Duan, Dan Chen, Chuangyi Gui, Huazhong University of Science and Technology, Wuhan, China

VSTORE: IN-STORAGE GRAPH BASED VECTOR SEARCH ACCELERATOR

Shengwen Liang, Ziming Yuan, Ying Wang, State Key Laboratory of Computer Architecture, Beijing, China; Cheng Liu, Huawei Li, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Xiaowei Li, Chinese Academy of Sciences, Beijing, China

APPROXIMATE COMPUTING, FICTION OR REALITY?

Time: 10:30 AM – 12:00 PM
Room: 3001, Level 3
Event Type: Research Panel
Topics Area(s): Design

Organizer(s): Laura Pozzi, USI Lugano, Lugano, Switzerland

Moderator: Kaushik Roy, Purdue University, West Lafayette, IN

Approximate Computing is a design paradigm postulating that accuracy of result is just another metric that can be tampered with. Traditionally, we played with metrics such as, for example, area and delay: “I will accept a larger implementation, as long as it is fast”. And we are used to synthesis tools for hardware, and compilation tools for software, that given one specification in input can generate hundreds of different implementation versions, and these may vary in terms of energy efficiency, delay, memory usage, etc. But playing with the accuracy of the output was not ever something that was on the table. What if it is. What if I can automatically tell my design tools: “and this is what I am prepared to pay in terms of accuracy loss”. Then we can say: “give me a less accurate implementation, as long as it’s _both_ smaller and faster”. That sounds great; but what are the challenges that AC poses, and hence how far are we from seeing Approximate Computing everywhere? Are there enough and significant applications that can tolerate a loss in accuracy? Are synthesis tools mature enough to generate designs that efficiently trade off accuracy, as if it were any other metric? Should we consider AC just in software, before we commit into generating inaccurate hardware? Let’s ask our panelists what their view is on the subject.

Panelists: Akash Kumar, Technische Universität Dresden, Dresden, Germany; Kailash Gopalakrishnan, IBM, New York City, NY; Sherief Reda, Brown University, Providence, RI; Vijay Raghunathan, Purdue University, West Lafayette, IN

SOFTWARE TOOLS FOR QUANTUM COMPUTING: HOW TO DESIGN THE NEXT BIG THING?

Time: 10:30 AM – 12:00 PM
Room: 3003, Level 3
Event Type: Special Session (Research)
Topics Area(s): Design

Organizer(s): Jie-Hong Roland Jiang, National Taiwan University, Taipei, Taiwan

Quantum computers are becoming "the next big thing." Recent accomplishments in their physical realization and a substantially increased interest from various stakeholders have led to numerous quantum computing applications that are currently being investigated–several of them with a promising near-term perspective. However, the best quantum computer is useless without proper software methods and frameworks to use them. Accordingly, several industrial and academic players recently introduced software tools and techniques for quantum computing–all addressing the respective design tasks with a unique and special perspective. This session gives an overview of different and complementary software tools for quantum computing–including references and links to advanced material and corresponding implementations.

QUANTUM INFORMATION SCIENCE WITH QISKIT

Ali Javadi-Abhari, IBM, Yorktown Heights, NY

AUTOMATIC ORACLE GENERATION IN MICROSOFT'S QUANTUM DEVELOPMENT KIT USING QIR AND LLVM PASSES

Mathias Soeken, Mariia Mykhailova, Microsoft, Zurich, Switzerland

QUANTUM ALGORITHM DESIGN: A NEW TOOL FOR THE DESIGN AUTOMATION OF QUANTUM COMPUTING CIRCUITS

Yuval Boger, Classiq, Haifa, Israel; Nir Minerbi, Classiq, Haifa, Israel

THE BASIS OF DESIGN TOOLS FOR QUANTUM COMPUTING: ARRAYS, DECISION DIAGRAMS, TENSOR NETWORKS, AND MORE

Robert Wille, Lukas Burgholzer, Stefan Hillmich, Alexander Ploier, Tom Peham, Johannes Kepler University Linz, Austria; Thomas Grurl, University of Applied Sciences Upper Austria, Hagenberg, Austria

COST-EFFICIENT ANALOG AND STOCHASTIC COMPUTING TECHNIQUES FOR DEEP LEARNING

Time: 1:30 PM – 3:00 PM
Room: 3007, Level 3
Event Type: Research Manuscript
Topics Area(s): AI/ML Design: Circuits and Architecture, Digital and Analog Circuits, Design

Chair/Co-Chair: Steven Hsu, Intel Corporation; TBA

This session presents a fundamental challenge: Cost-efficient and practical implementation of deep learning techniques. The solutions offered to this challenge span a broad range, from novel stochastic computation techniques to analog memristive neural network accelerators. The research presented in this session also describes how domain-specific knowledge and cost-efficient methods can help analog and RF circuit parameter optimization and stochastic time to digital conversion.

SCALED COUNTING-BASED STOCHASTIC COMPUTING MULTIPLICATION FOR IMPROVED ACCURACY

Shuyuan Yu, Sheldon Tan, University of California, Riverside, CA

TAILOR: REMOVING REDUNDANCY IN MEMRISTIVE ANALOG NEURAL NETWORK ACCELERATORS

Xingchen Li, Zhihang Yuan, Guangyu Sun, Peking University, Beijing, China; Liang Zhao, Zhichao Lu, Hefei Reliance Memory Ltd., Hefei, China

DOMAIN KNOWLEDGE-INFUSED DEEP LEARNING FOR AUTOMATED ANALOG/RF CIRCUIT PARAMETER OPTIMIZATION

Weidong Cao, Xuan Zhang, Washington University, St. Louis, MO; Mouhacine Benosman, Rui Ma, Mitsubishi Electric Research Laboratories, Boston, MA

A COST-EFFICIENT FULLY SYNTHESIZABLE STOCHASTIC TIME-TO-DIGITAL CONVERTER DESIGN BASED ON INTEGRAL NONLINEARITY SCRAMBLING

Qiaochu Zhang, Shiyu Su, Mike Chen, University of Southern California, Los Angeles, CA

EMBEDDED SYSTEMS IN THE AGE OF AI – SMART(ER) TOOLS AND FRAMEWORKS

Time: 1:30 PM – 3:00 PM
Room: 3004, Level 3
Event Type: Research Manuscript
Topics Area(s): Embedded Software, AI, Embedded Systems, RISC-V

Chair/Co-Chair: TBA

The session reflects recent trends in embedded systems design. Motivated by exciting new hardware architectures and software applications, the session will introduce new techniques to improve system performance using graph networks as well as enhance the efficiency of graph executions. In addition, a novel kernel debugging tool will be presented for RISC-V architecture, as well as methods for embedded code generation for Simulink models.

USING MACHINE LEARNING TO OPTIMIZE GRAPH EXECUTION ON NUMA MACHINES

Hiago Rocha, Janaina Schwarzrock, Antonio Carlos Schneider Beck, Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil; Arthur Lorenzon, Federal University of Pampa, Alegrete, Brazil

HCG: OPTIMIZING EMBEDDED CODE GENERATION OF SIMULINK WITH SIMD INSTRUCTION SYNTHESIS

Zhuo Su, Zehong Yu, Yixiao Yang, Yu Jiang, Jiaguang Sun, Tsinghua University, Beijing, China; Dongyan Wang, Renmin University of China, Beijing, China; Rui Wang, Capital Normal University, Beijing, China; Wanli Chang, University of York, York, United Kingdom

RAVEN: A NOVEL KERNEL DEBUGGING TOOL ON RISC-V

Hongyi Lu, Fengwei Zhang, Southern University of Science and Technology, Shenzhen, China

GTUNER: TUNING DNN COMPUTATIONS ON GPU VIA GRAPH ATTENTION NETWORK

Qi Sun, Xinyun Zhang, Hao Geng, Yuxuan Zhao, Yang Bai Bei Yu, The Chinese University of Hong Kong, Hong Kong; Haisheng Zheng, SmartMore, Shenzhen, China

FROM CORES TO MEMORY AND BACK

Time: 1:30 PM – 3:00 PM
Room: 3005, Level 3
Event Type: Research Manuscript
Topics Area(s): SoC, Heterogeneous, and Reconfigurable Architectures, Design

Chair/Co-Chair: TBA

This session presents four innovative contributions related to cores and memories for SoC systems. The first paper analyzes data-prefetching techniques for commercial in-order cores followed by a paper on improving the performance of Propane NVM systems using DDR5 memory. The third contribution describes a framework for the processing of graphs using hybrid memory cubes. The fourth contribution AxoNN introduces techniques for energy-aware execution of neural network inference on multi-accelerator SoCs.

PREF-X: A FRAMEWORK TO REVEAL DATA PREFETCHING IN COMMERCIAL IN-ORDER CORES

Quentin Huppert, Lionel Torres, University of Montpellier, Montpellier, France; Francky Catthoor, imec, Leuven, Belgium; David Novo, CNRS, LIRMM, University of Montpellier, Montpellier, France

ARCHITECTING DDR5 DRAM CACHES FOR NON-VOLATILE MEMORY SYSTEMS

Xin Xin, University of Pittsburgh, Pittsburgh, PA; Wanyi Zhu, Alibaba Group, Hangzhou, China; Li Zhao, Alibaba Group, Sunnyvale, CA

GRAPHRING: AN HMC-RING BASED GRAPH PROCESSING FRAMEWORK WITH OPTIMIZED DATA MOVEMENT

Zerun Li, Xiaoming Chen, Yinhe Han, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

AXONN: ENERGY-AWARE EXECUTION OF NEURAL NETWORK INFERENCE ON MULTI-ACCELERATOR HETEROGENEOUS SOCS

Ismet Dagli, Alexander Cieslewicz, Jedidiah McClurg, Mehmet Belviranli, Colorado School of Mines, Golden, CO

NOVEL CIRCUITS FOR PIM

Time: 1:30 PM – 3:00 PM
Room: 3002, Level 3
Event Type: Research Manuscript
Topics Area(s): In-memory and Near-memory Computing, Design

Chair/Co-Chair: Zhezhi He, Shanghai Jiao Tong University; Ramtin Zand, University of South Carolina

Although processing-in-memory has been around for decades, cutting-edge circuit level techniques are considerably expanding the scope of functionality and efficacy on key performance indicators for PIM systems. The papers in this session cover such circuit level innovations applicable to PIM systems built from ultra-efficient ternary activations using SRAM, pre-charge-free DRAM, innovative uses of ROM, and emerging memories.

PIPF-DRAM: PROCESSING IN PRECHARGE-FREE DRAM

Nezam Rohbani, Institute for Research in Fundamental Sciences (IPM), Tehran, Iran; Mohammad Arman Soleimani, Hamid Sarbazi-Azad, Sharif University of Technology, Tehran, Iran

TAIM: TERNARY ACTIVATION IN-MEMORY COMPUTING HARDWARE WITH 6T SRAM ARRAY

Nameun Kang, Hyungjun Kim, Hyunmyung Oh, Pohang University of Science and Technology, Pohang, South Korea; Jae-Joon Kim, Seoul National University, Seoul, South Korea

PIM-DH: RERAM-BASED PROCESSING-IN-MEMORY ARCHITECTURE FOR DEEP HASHING ACCELERATION

Fangxin Liu, Wenbo Zhao, Yongbiao Chen, Zongwu Wang, Zhezhi He, Rui Yang, Qidong Tang, Tao Yang, Li Jiang, Shanghai Jiao Tong University, Shanghai, China; Cheng Zhuo, Zhejiang University, Hangzhou, China

YOLOC: DEPLOY LARGE-SCALE NEURAL NETWORK BY ROM-BASED COMPUTING-IN-MEMORY USING RESIDUAL BRANCH ON A CHIP

Yiming Chen, Guodong Yin, Zhanhong Tan, Mingyen Lee, Zekun Yang, Yongpan Liu, Huazhong Yang, Kaisheng Ma, Xueqing Li, Tsinghua University, Beijing, China

AUTOMATING ANALOG LAYOUT – HAS THE TIME FINALLY COME?

Time: 1:30 PM – 3:00 PM
Room: 3001, Level 3
Event Type: Research Panel
Topics Area(s): AI, EDA

Organizer(s): Brucek Khailany, NVIDIA, Austin, TX; Tom Gray, NVIDIA, Apex, NC

Moderator: Tom Lee, Stanford University, Stanford, CA

Despite decades of progress in automating digital design, performing layout of analog/mixed-signal (AMS) integrated circuits (ICs) is still almost exclusively a manual tedious task in industry, despite many attempts over the years at automation. Some of the challenges include the complexity of mixed-signal layout and design rules in modern CMOS processes, the high sensitivity of analog circuit performance and functionality to layout parasitics, and perhaps an inherent lack of trust by analog design teams of automation tools. Recently, with new algorithms, analog layout generators, and the use of machine learning in many automation tasks, recent research has renewed the push towards analog layout automation, with the claim that it may now finally be possible. Is this true? On one hand, we have seen new algorithms and machine learning solve many problems previously unsolvable in domains such as natural language processing and computer vision. On the other hand, such probabilistic approaches may not be suitable to many chip design tasks. In this panel, experts from academia and industry spanning the EDA and analog design space will discuss the opportunities, promises, and pitfalls to analog design and layout automation.

Panelists: Steven Burns, Intel Corporation, Hillsboro, OR; Elad Alon, University of California, Berkeley, CA; Ting-Sheng Ku, NVIDIA; Weikai Sun, Synopsys, Santa Clara, CA

TINYML: HOW TINY CAN WE GET?

Time: 1:30 PM – 3:00 PM
Room: 3003, Level 3
Event Type: Special Session (Research)
Topics Area(s): AI

Organizer(s): Vijay Janapa Reddi, Harvard University, Cambridge, MA

The next wave of growth in AI will be driven in good part by embedding intelligence into ubiquitous devices such including wearables, implanted devices, smart home devices. Most of these devices present extremely tight size, cost, weight and power constraints. Tiny machine learning (TinyML) is a fast-growing sub-field of ML that addresses the design of algorithms, software frameworks, hardware and systems for such applications. This session will feature three experts in the field of TinyML who will outline the unique challenges.

PROSPECTS AND CHALLENGES FOR TINYML

Vijay Janapa Reddi, Harvard University, Cambridge, MA

SOFTWARE FRAMEWORKS FOR TINYML

Pete Warden, Google, Mountain View, CA

CO-DESIGNING ALGORITHMS AND HARDWARE FOR EFFICIENT TINYML

John Brown, Arm Ltd., Marion, MA

AI AND ML ON NEXT GENERATION COMPUTING PLATFORMS

Time: 3:30 PM – 5:30 PM
Room: 3005, Level 3
Event Type: Research Manuscript
Topics Area(s): Emerging Models of Computation, Design

Chair/Co-Chair: Priyadarshini Panda, Yale University; Qinru Qiu, Syracuse University

In this session, novel brain-inspired and physics-based computing models are presented with their implementation on emerging computing platforms. The papers cover different computing models from spiking neural networks, hyperdimensional computing, ising machine, to path-based in-memory computing. Algorithm and hardware co-design are implemented on platforms such as ReRAM, FPGA, embedded systems.

ASTERS: ADAPTABLE THRESHOLD SPIKE-TIMING NEUROMORPHIC DESIGN WITH TWIN-COLUMN RERAM SYNAPSES

Ziru Li, Qilin Zheng, Yiran Chen, Duke University, Durham, NC; Bonan Yan, Ru Huang, Peking University, Beijing, China; Bing Li, Technische Universität München, Beijing, China

SATO: SPIKING NEURAL NETWORK ACCELERATION VIA TEMPORAL-ORIENTED DATAFLOW AND ARCHITECTURE

Fangxin Liu, Wenbo Zhao, Zongwu Wang, Yongbiao Chen, Tao Yang, Zhezhi He, Xiaokang Yang, Li Jiang, Shanghai Jiao Tong University, Shanghai, China

LEHDC: LEARNING-BASED HYPERDIMENSIONAL COMPUTING CLASSIFIER

Shijin Duan, Xiaolin Xu, Northeastern University, Boston, MA; Yejia Liu, Shaolei Ren, University of California, Riverside, CA

GENERIC: HIGHLY EFFICIENT LEARNING ENGINE ON EDGE USING HYPERDIMENSIONAL COMPUTING

Behnam Khaleghi, Jaeyoung Kang, Hanyang Xu, Justin Morris, Tajana Rosing, University of California, San Diego, CA

SOLVING TRAVELING SALESMAN PROBLEMS VIA A PARALLEL FULLY CONNECTED ISING MACHINE

Qichao Tao, Jie Han, University of Alberta, Edmonton, Canada

PATH: EVALUATION OF BOOLEAN LOGIC USING PATH-BASED IN-MEMORY COMPUTING

Sven Thijssen, Rickard Ewetz, University of Central Florida, Orlando, FL; Sumit Jha, The University of Texas at San Antonio, San Antonio, TX

HARD(WARE) LEARNING IS COOL!!

Time: 3:30 PM – 5:30 PM
Room: 3002, Level 3
Event Type: Research Manuscript
Topics Area(s): AI/ML Design: System and Platform, Design

Chair/Co-Chair: TBA

Machine learning applications have shifted from general-purpose processors to specialized hardware accelerators to achieve high performance and energy efficiency. This session presents six papers on efficient and scalable hardware implementations of machine learning. The papers range from traditional deep learning acceleration to continual learning as well as reinforcement learning. In order to improve efficiency, these papers propose transformative improvement in techniques such as weight pruning and model partitioning. Improving neural compilation using mathematical embeddings of target hardware and efficient hardware-software co-design approaches are also introduced.

A LENGTH ADAPTIVE ALGORITHM-HARDWARE CO-DESIGN OF TRANSFORMER ON FPGA THROUGH SPARSE ATTENTION AND DYNAMIC PIPELINING

Hongwu Peng, Shaoyi Huang, Bingbing Li, Jinbo Bi, Caiwen Ding, University of Connecticut, Storrs, CT; Shiyang Chen, Hang Liu, Stevens Institute of Technology, Hoboken, NJ; Tong Geng, Ang Li, Pacific Northwest National Laboratory, Richland, WA; Weiwen Jiang, George Mason University, Fairfax, VA; Wujie Wen, Leiden University, Bethlehem, PA

HDPG: HYPERDIMENSIONAL POLICY-BASED REINFORCEMENT LEARNING FOR CONTINUOUS CONTROL

Yang Ni, Mariam Issa, Danny Abraham, Mohsen Imani, University of California, Irvine, CA; Mahdi Imani, Northeastern University, Boston, MA; Xunzhao Yin, Zhejiang University, Hangzhou, China

CARM: HIERARCHICAL EPISODIC MEMORY FOR CONTINUAL LEARNING

Soobee Lee, Minindu Weerakoon, Myeongjae Jeon, UNIST, Ulsan, South Korea; Jonghyun Choi, Yonsei University, Gwangju, South Korea; Minjia Zhang, Di Wang, Microsoft, Redmond, WA

SHFL-BW: ACCELERATING DEEP NEURAL NETWORK INFERENCE WITH TENSOR-CORE AWARE WEIGHT PRUNING

Guyue Huang, Yufei Ding, Yuan Xie, University of California, Santa Barbara, CA; Haoran Li, Alibaba Group, Shanghai, China; Minghai Qin, Milpitas, CA; Fei Sun, Alibaba Group, Sunnyvale, CA

QUILTNET: EFFICIENT DEEP LEARNING INFERENCE ON MULTI-CHIP ACCELERATORS USING MODEL PARTITIONING

Jongho Park, Hyukjun Kwon, Seowoo Kim, Junyoung Lee, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea; Minho Ha, Euicheol Lim, SK hynix, Icheon-si, South Korea; Mohsen Imani, University of California, Irvine, CA; Yeseong Kim, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea

GLIMPSE: MATHEMATICAL EMBEDDING OF HARDWARE SPECIFICATION FOR NEURAL COMPILATION

Byung Hoon Ahn, Sean Kinzer, Hadi Esmaeilzadeh, University of California, San Diego, CA

KEEP MOVING UP AND LOOKING SIDEWAYS WITH VERIFICATION BOOSTERS!

Time: 3:30 PM – 5:30 PM
Room: 3000, Level 3
Event Type: Research Manuscript
Topics Area(s): Design Verification and Validation, EDA

Chair/Co-Chair: Maheshwar Chandrasekar, Synopsys; TBA

This section reflects the latest trends in verification and validation. It introduces state-of-the-art software-level verification methodologies and symbolic execution tools to accelerate bug hunting in high-level hardware generators and transaction-level peripherals. It presents the first formal verification method for modular multipliers. It further illustrates advanced learning-based techniques that extend the envelope of verification and validation in practical applications, including security validation of logic-locked hardware IPs and active learning to accelerate IC yield analysis and optimization. The session finale goes beyond EDA with the introduction of a boosted, neural network-based barrier certificate synthesis method using collaborative learning for cyber-physical system verification.

BRINGING SOURCE-LEVEL DEBUGGING FRAMEWORKS TO HARDWARE GENERATORS

Keyi Zhang, Zain Asgar, Mark Horowitz, Stanford University, Stanford, CA

VERIFYING SYSTEMC TLM PERIPHERALS USING MODERN C++ SYMBOLIC EXECUTION TOOLS

Pascal Pieper, Vladimir Herdt, DFKI, Bremen, Germany; Daniel Grosse, Johannes Kepler University Linz, Linz, Austria; Rolf Drechsler, University of Bremen/DFKI, Bremen, Germany

FORMAL VERIFICATION OF MODULAR MULTIPLIERS USING SYMBOLIC COMPUTER ALGEBRA AND BOOLEAN SATISFIABILITY

Alireza Mahzoon, University of Bremen, Germany; Daniel Grosse, Johannes Kepler University Linz, Linz, Austria; Christoph Scholl, Alexander Konrad, University Freiburg, Germany; Rolf Drechsler, University of Bremen/DFKI, Bremen, Germany

SILICON VALIDATION OF LUT-BASED LOGIC-LOCKED IP CORES

Gaurav Kolhe, Tyler Sheaves, Kevin Immanuel Gubbi, Setareh Rafatirad, Houman Homayoun, University of California, Davis, CA; Tejas Kadale, San Francisco, CA; Sai Manoj Pudukotai Dinakarrao, Avesta Sasan, George Mason University, Fairfax, VA; Hamid Mahmoodi, San Francisco State University, San Francisco, CA

EFFICIENT BAYESIAN YIELD ANALYSIS AND OPTIMIZATION WITH ACTIVE LEARNING

Shuo Yin, Xiang Jin, Linxu Shi, Kang Wang, Wei Xing, Beihang University, Beijing, China

ACCELERATED SYNTHESIS OF NEURAL NETWORK-BASED BARRIER CERTIFICATES USING COLLABORATIVE LEARNING

Jun Xia, Ming Hu Mingsong Chen, East China Normal University, Shanghai, China; Xin Chen, Nanjing University, Nanjing, China

SO YOU WANT A BETTER DESIGN? GO WITH FASTER TIMING AND LOWER POWER PLEASE!

Time: 3:30 PM – 5:30 PM
Room: 3007, Level 3
Event Type: Research Manuscript
Topics Area(s): Timing and Low Power Design, EDA

Chair/Co-Chair: Karthi Duraisamy, Synopsys; Cong (Callie) Hao, Georgia Institute of Technology

This session focuses on how to derive a better design in terms of timing performance and power efficiency. AI/ML methods are continuously being used in the EDA industry and so is the case in this session. Six papers are presented in this session, with half focusing on timing and half focusing on power. The first three papers develop innovative AI/ML methods to improve the timing performance and the last three papers develop AI/ML methods to improve power efficiency.

A TIMING ENGINE INSPIRED GRAPH NEURAL NETWORK MODEL FOR PRE-ROUTING SLACK PREDICTION

Zizheng Guo, Yibo Lin, Peking University, Beijing, China; Mingjie Liu, Jiaqi Gu, Shuhan Zhang, David Z. Pan, The University of Texas at Austin, TX

ACCURATE TIMING PREDICTION AT PLACEMENT STAGE WITH LOOK-AHEAD RC NETWORK

He Xu, Zhiyong Fu, Hunan University, Changsha, China; Yao Wang, Chang Liu, Yang Guo, National University of Defense Technology, Changsha, China

TIMING MACRO MODELING WITH GRAPH NEURAL NETWORKS

Kevin Kai-Chun Chang, Chun-Yao Chiang, Iris Hui-Ru Jiang, National Taiwan University, Taipei, Taiwan; Pei-Yu Lee, Cadence Design Systems, Inc., Hsinchu, Taiwan

WORST-CASE DYNAMIC POWER DISTRIBUTION NETWORK NOISE PREDICTION USING CONVOLUTIONAL NEURAL NETWORK

Xiao Dong, Yufei Chen, Xunzhao Yin, Cheng Zhuo, Zhejiang University, Hangzhou, China

GATSPI: GPU ACCELERATED GATE-LEVEL SIMULATION FOR POWER IMPROVEMENT

Yanqing Zhang, Akshay Sridharan, NVIDIA, Santa Clara, CA; Haoxing Ren, Brucek Khailany, NVIDIA, Austin, TX

PPATUNER: PARETO-DRIVEN TOOL PARAMETER AUTO-TUNING IN PHYSICAL DESIGN VIA GAUSSIAN PROCESS TRANSFER LEARNING

Hao Geng, Tsung-Yi Ho, Bei Yu, The Chinese University of Hong Kong, Hong Kong; Qi Xu, University of Science and Technology of China, Hefei, China

TIMING-CRITICAL DESIGN

Time: 3:30 PM – 5:30 PM
Room: 3004, Level 3
Event Type: Research Manuscript
Topics Area(s): Time-Critical System Design, Embedded Systems

Chair/Co-Chair: Rodolfo Pellizzoni, University of Waterloo; Shahin Golshan, Synopsys

Papers in this session present efficient and yet timing-predictable system designs. They cover the advances of data age analysis for automotive systems, compilation for timing predictability and efficiency, memory architecture for predictable real-time computing, resource sharing, and worst-case execution time (WCET) analysis and optimization.

EFFICIENT MAXIMUM DATA AGE ANALYSIS FOR CAUSE-EFFECT CHAINS IN AUTOMOTIVE SYSTEMS

Ran Bi, Xinbin Liu, Jiankang Ren, Pengfei Wang, Huawei Lv, Guozhen Tan, Dalian University of Technology, Dalian, China

OPTIMIZING PARALLEL PREM COMPILATION OVER NESTED LOOP STRUCTURES

Zhao Gu, Rodolfo Pellizzoni, University of Waterloo, Waterloo, Canada

SCHEDULING AND ANALYSIS OF REAL-TIME TASKS WITH PARALLEL CRITICAL SECTIONS

Yang Wang, Xu Jiang, Dong Ji, Northeastern University, Shenyang, China; Nan Guan, City University of Hong Kong, Hong Kong; Mingsong Lv, The Hong Kong Polytechnic University, Hong Kong; Wang Yi, Uppsala University, Uppsala, Sweden

BLUESCALE: A SCALABLE MEMORY ARCHITECTURE FOR PREDICTABLE REAL-TIME COMPUTING ON HIGHLY INTEGRATED SOCS

Zhe Jiang, Arm Ltd., Sheffield, United Kingdom; Kecheng Yang, Texas State University, San Marcos, TX; Neil Audsley, City University of London, United Kingdom; Nathan Fisher, Weisong Shi, Zheng Dong, Wayne State University, Detroit, MI

PRECISE AND SCALABLE SHARED CACHE CONTENTION ANALYSIS FOR WCET ESTIMATION

Wei Zhang, Lei Ju, Shandong University, Qingdao, China; Mingsong Lv, The Hong Kong Polytechnic University, Hong Kong, Hong Kong; Wanli Chang, University of York, United Kingdom

PREDICTABLE SHARING OF LAST-LEVEL CACHE PARTITIONS FOR MULTI-CORE SAFETY-CRITICAL SYSTEMS

Zhuanhao Wu, Hiren Patel, University of Waterloo, Waterloo, Canada

HETEROGENEOUS 3D OR MONOLITHIC 3D, WHICH DIRECTION TO GO?

Time: 3:30 PM – 5:30 PM
Room: 3001, Level 3
Event Type: Research Panel
Topics Area(s): EDA

Organizer(s): Sung Kyu Lim, Georgia Institute of Technology, Atlanta, GA

Moderator: Max Shulaker, MIT

The term 3D IC has seen two long lasting—and confusing sometimes—definitions, depending on who you ask: advanced packaging vs. advanced circuit. The former is backed by the group that develops the technologies to vertically integrate heterogenous chiplets. The latter believes that there is more work to be done at the "front-end", i.e., IC design houses and foundries. With chips getting larger and costlier to produce, chipletization has become inevitable. But, bumps and pads will not be enough to provide ultra-high density chip-to-chip interconnect needed in future applications. Thus, we ask the questions: will advanced packaging lose steam quickly, or will monolithic 3D IC never happen? If they will co-exist, for what applications? What are the pressing needs in manufacturing, design, and EDA technologies?

Panelists: Subramanian Iyer, University of California, Los Angeles, CA; Sonia Leon, Intel Corporation, San Francisco, CA; Gabriel Loh, Advanced Micro Devices, Inc., Bellevue, WA; Subhasish Mitra, Stanford University, Stanford, CA

SECURITY DURING SYSTEM LEVEL DESIGN : SMALL STEP OR GIANT LEAP?

Time: 3:30 PM – 5:30 PM
Room: 3003, Level 3
Event Type: Special Session (Research)
Topics Area(s): Security

Organizer(s): Christian Pilato, Politecnico di Milano, Milan, Italy

The security of electronic circuits is becoming one of the most critical issues in the semiconductor industry. Malicious actors in the electronic supply chain may be interested in stealing the intellectual property (harming the design houses' businesses) of the user's data (harming the end users' security and privacy). More and more integrated circuits are being designed at the system level to reduce design and verification costs. Working at the system level also broadens the scope of vulnerabilities that can be detected. However, most of the current security solutions are targeting the lower levels of abstraction (especially the gate level). This session aims at presenting the current view on the security challenges for electronic system-level design, where we think these challenges should be targeted all together. This is a timely topic not only for academic research but also for industry, where there is a strong interest for such high-level methods. In this context, the top-notch research groups involved in this special session can offer their viewpoint

SECURE BY CONSTRUCTION: ADDRESSING SECURITY VULNERABILITIES INTRODUCED DURING HIGH-LEVEL SYNTHESIS

Md Rafid Muttaki, Zahin Ibnat, Farimah Farahmandi, University of Florida, Gainesville, FL

HIGH-LEVEL DESIGN METHODS FOR HARDWARE SECURITY: IS IT THE RIGHT CHOICE?

Christian Pilato, Donatella Sciuto, Politecnico di Milano, Milan, Italy; Siddharth Garg, Ramesh Karri, New York University, Brooklyn, NY

TRUSTING THE TRUST ANCHOR: TOWARDS DETECTING CROSS-LAYER VULNERABILITIES WITH HARDWARE FUZZING

Jeyavijayan Rajendran, Rahul Kande, Chen Chen, Aakash Tyagi, Texas A&M University, College Station, TX; Ahmad-Reza Sadeghi, Patrick Jauernig, Pouya Mahmoody, Technische Universität Darmstadt, Germany

AUTOMATING HARDWARE SECURITY PROPERTY GENERATION

Ryan Kastner, Andres Meza, University of California, San Diego, CA; Cynthia Sturton, University of North Carolina, Chapel Hill, NC; Francesco Restuccia, Scuola Superiore Sant'Anna Pisa, Pisa, Italy; Sayak Ray, Intel Corporation, Hillsboro, OR; Jason Fung, Intel Corporation, Santa Clara, CA

ADDITIONAL MEETING INFORMATION

HACK at DAC

Sunday, July 10th at 8:00 am – 6:00 pm
Monday, July 11th at 8:00 am – 6:00 pm
Level 2 Lobby

Young Fellows Program

Sunday, July 10th at 9:00 am – 6:00 pm
Room 3016

Early Career Workshop

Sunday, July 10th at 9:00 am – 5:00 pm
Room 3018

Accellera Luncheon & Panel Discussion

Tuesday, July 12th at 11:30 am – 1:00 pm
Room 3024

IEEE CEDA Distingushed Speaker Luncheon:

In-Memory Computing: From Devices to Applications – A Cross-Layer Perspective
Featuring X. Sharon Hu, University of Notre Dame

Tuesday, July 12th at 12:00 pm – 1:30 pm
Room 3018

PhD Forum and University Demo

Tuesday, July 12th at 7:00 pm – 9:00 pm
Level 3 Lobby

Doulos Lunch and Learn

Wednesday, July 13th at 12:15 pm – 1:15 pm
Room 3018

Young Fellows Program Closing Ceremony

Thursday, July 14th at 3:30 pm – 5:30 pm
Room 3024

Cooley's DAC Troublemaker Panel

Monday, July 11 at 3:00 pm – 4:00 pm

Room 3016

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MONDAY, JULY 11	
10:00 am	**Exhibit Hall Opens**
10:30 – 11:15 am	**Microsoft: Architectural Advantages of AMD Milan-X in Azure HBv3 for Logic Simulation** **Speaker:** Philip Steinke – AMD Fellow
11:30 – 12:15 pm	**Synopsys: Transforming EDA Time-to-Market with Synopsys Cloud** **Speaker:** Vikram Bhatia, Head of Cloud Product Management and GTM Strategy
12:30 – 1:15 pm	**Memverge: Transparent Checkpointing for EDA** **Speaker:** Bernie Wu, Vice President of Strategic Alliances
1:30 – 2:15 pm	**Cadence: From Chips to Systems: The Cloud Imperative** **Speaker:** Mahesh Turaga, VP Business Development, Cloud Team, Cadence
2:30 – 3:15 pm	**Siemens: Practical Cloud Solutions from Siemens EDA** **Speaker:** Craig Johnson, VP, Siemens EDA Cloud Solutions
3:30 – 4:15 pm	**Google: Moving EDA to Cloud, a Story from Google Cloud** **Speaker:** Di Wu, Software Engineer, Google Cloud
4:30 – 5:15 pm	**Pure Storage: Next-Gen Connected Cloud Datacenter with Infrastructure as Code** **Speaker:** Bikash Roy Choudhury, Director of Solutions
TUESDAY, JULY 12	
10:00 am	**Exhibit Hall Opens**
10:30 – 11:15 am	**Anari AI: Message Passing Paradigm can Unite HW and SW Design** **Speaker:** PhD Bogdan Vukobratovic, Co-founder and CTO of ANARI AI
11:30 – 12:15 pm	**Cliosoft: Unleashing Full Analog Design and Simulation Environment on Optimized Cloud** **Speaker:** Richard Paw, Director, Semiconductors & EDA, Microsoft, Teng-Kiat Lee, Technical Marketing Director, Synopsys, and Simon Rance, VP Marketing, Cliosoft
12:30 – 1:15 pm	**Tuple Tech: A Novel DevSecOps Platform For IC/FPGA Design** **Speaker:** Kris Reddy, Head of Business Development, and Vamshi Reddy, President & CEO
2:15 – 5:15 pm	**NetApp: Hands-on Lab: Build a Hybrid Burst to Cloud environment with NetApp "Design Anywhere" Cloud-Bursting EDA Workloads with Bi-Directional Caching of Job Data** **Speaker:** Michael Johnson
6:00 pm	**Exhibit Hall Closes**
WEDNESDAY, JULY 13	
10:00 am	**Exhibit Hall Opens**
10:15 am – 1:15 pm	**Microsoft: How to run EDA tools on the Azure Cloud** **Speaker:** Richard Paw
2:15 – 5:15 pm	**Google: Google Cloud Training** **Speaker:** Peeyush Tugnawat
6:00 pm	**Exhibit Hall Closes**

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MONDAY, JULY 11	
11:30 – 12:15 pm	**Analog IP The Way You Want It** Graham Woods, Agile Analog Ltd.
12:30 – 1:15 pm	**Accelerating Time to Market: Open and Collaborative Innovation in the Hardware Development Ecosystem** Rob Mains, CHIPS Alliance/Linux Foundation
1:30 – 2:15pm	**What's New with FreeRTOS** Richard Barry, Sr. Principal SDE, IoT Device Services
2:30 – 3:15 pm	**Introduction to RISC-V Verification with new open standard RVVI (RISC-V Verification Interface)** Aimee Sutton, Imperas Software
TUESDAY, JULY 12	
10:30 – 11:15am	**RISC-V and HPC** Dr. John Leidel (Founder and Chief Scientist, Tactical Computing Laboratories) Dave Donofrio (Chief Hardware Architect, Tactical Computing Laboratories)
1:30 – 2:15pm	**RISC-V Models for Verification, Software Development and Architectural Exploration** Larry Lapides, Imperas Software
2:30 – 3:15 pm	**CORE-V MCU Devkit Teardown** Rick O'Connor (President & CEO of OpenHW Group) & Griffin Covert (Hardware Engineering Lead of GroupGets)
3:30 – 4:15 pm	**Addressing the challenges of RISC-V adoption – live panel discussion at DAC 2022** Scot Morrison, GM of Embedded Software Solutions; Andy Gothard, Sr. Marketing Manager with Tessent Embedded Analytics; Joe Hupcey III, Verification Product Technologist with Questa Design & Verification Technologies
4:30 – 5:15 pm	**CORE-V MCU DevKit Fleet Sensors in AWS IoT Cloud** Rick O'Connor, President and CEO, OpenHW Group
WEDNESDAY, JULY 13	
10:30 – 11:15 am	**SiliconCompiler: Automating translation from code to silicon** Zero ASIC
11:30 – 12:15 pm	**CORE-V MCU DevKit Fleet Sensors in AWS IoT Cloud** Rick O'Connor, President and CEO, OpenHW Group
2:30 – 3:15 pm	**RiVAI RVV Vector Processor Solution** Yi Zeng, Vice President, RiVAI Technology

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